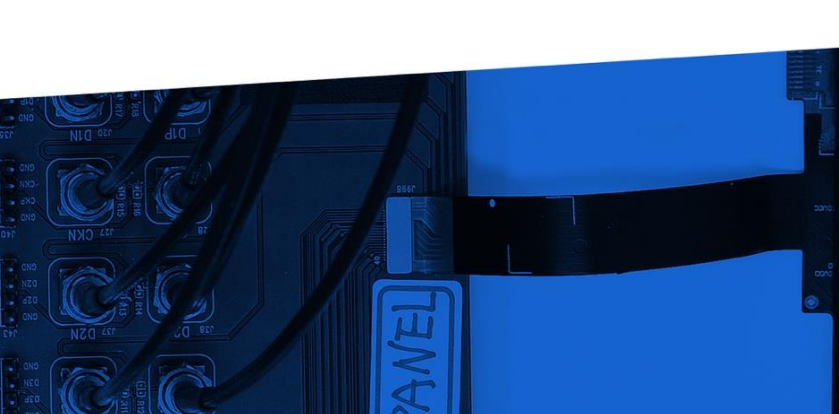
DATA SHEET

SV4E-DPRX

MIPI D-PHY Analyzer

E SERIES



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Introduction

OVERVIEW

The **SV4E-DPRX MIPI D-PHY Analyzer** is a highly integrated packet and protocol analyzer that facilitates the rapid validation of MIPI® Alliance enabled devices. Such devices include display panels or driver ICs, high-resolution image sensors and advanced image signal processors used in mobile or IoT applications. The SV4E-DPRX's unique analog front-end technology for the MIPI Alliance D-PHY℠ physical layer means that users can achieve high-confidence device validation without worrying about physical attachment issues. The Introspect ESP Software provided with the unit includes a full suite of tools for CSI-2 and DSI-2 packet and frame analysis for system level validation.

KEY FEATURES

- **D-PHY Physical Layer Receiver**: monolithic receiver with integrated LP/HS signaling and support for symbol rates up to 2.5 Gbps
- **D-PHY Protocols**: fully supports CSI-2 and DSI-2 pixel formats and DSI-2 DSC and V-DCM decompression
- **Diagnostics**: full packet and image frame analysis with built-in CRC and error detection
- **I2C Master**: built-in I2C controller for programming sensors and providing true host-emulation capability integrated within the Introspect ESP Software
- **Programmable Power Supplies**: six built-in power supplies for devices under test, with control and monitoring functions integrated within the Introspect ESP Software

KEY BENEFITS

- **Self-Contained**: an all-in-one system enables the simplest bench environment for protocol validation applications
- **Automated**: leverages the full power of Python and the award-winning Introspect ESP Software. Scripting capability is ideal for debug tasks and full-fledged production screening of devices and system modules
- **Future Proof**: protect your investment by adopting a high-performance tool for multiple product applications and across a large span of data rates

ORDERING INFORMATION

TABLE 1 ITEM NUMBERS FOR THE SV4E-DPRX ANALYZER

PART NUMBER	NAME	KEY DIFFERENTIATORS
5665	SV4E-DPRX MIPI D-PHY Analyzer (includes Introspect ESP SW license)	Low cost packet analyzer for D-PHY links

Feature Description

COMPLETE D-PHY RECEIVER IMPLEMENTATION

The SV4E-DPRX MIPI D-PHY Analyzer is a complete, integrated, 4-lane D-PHY receiver providing the analog front-end circuitry for D-PHY as well as a complete protocol back-end. As shown in Figure 1, each lane contains low power (LP) programmable threshold voltage detectors, dynamically controlled termination resistors, and fully differential high-speed (HS) receivers. The real-time behavior of the DPRX enables broad acquisition capabilities for physical-layer and protocol-layer testing.

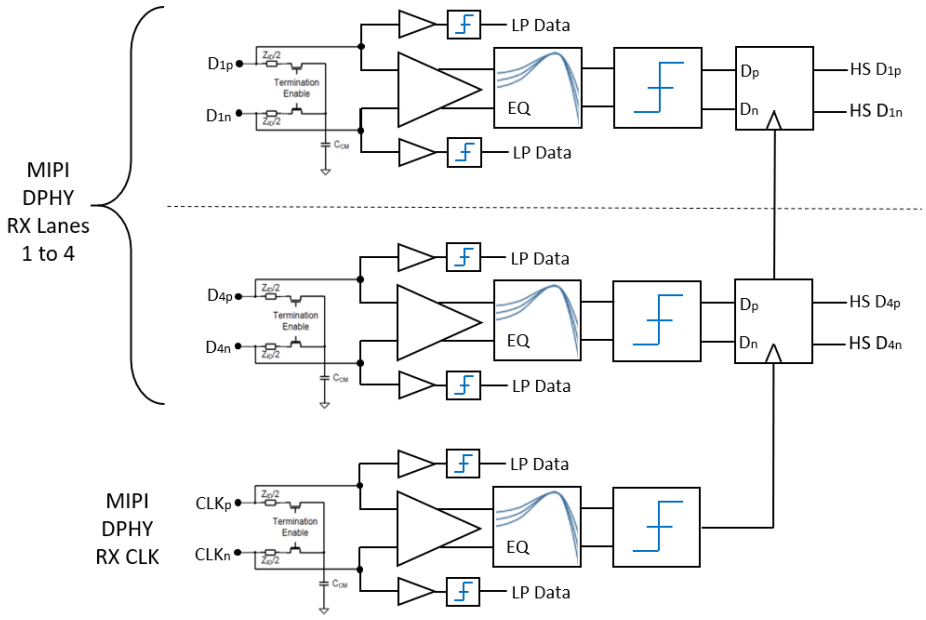

Figure 1: SV4E-DPRX receiver detail illustrating LP detection and HS receivers for Data and Clock lanes

PROTOCOL ANALYSIS

The SV4E-DPRX MIPI D-PHY Analyzer is a complete protocol analyzer for both camera and display serial interfaces. The analyzer adjusts its viewer displays based on the protocol being measured. Figure 2 below shows analysis features available in the Introspect ESP software, including viewers for:

- CSI/DSI Packets: merged traffic from all lanes may be viewed as unique packets, headers are decoded for easy, high-level viewing, and errors (header ECC, payload CRC) are automatically highlighted
- Frames: images are automatically reconstructed and saved, even if incomplete, with details such as pixel format, virtual channel, and image dimensions shown in the viewer

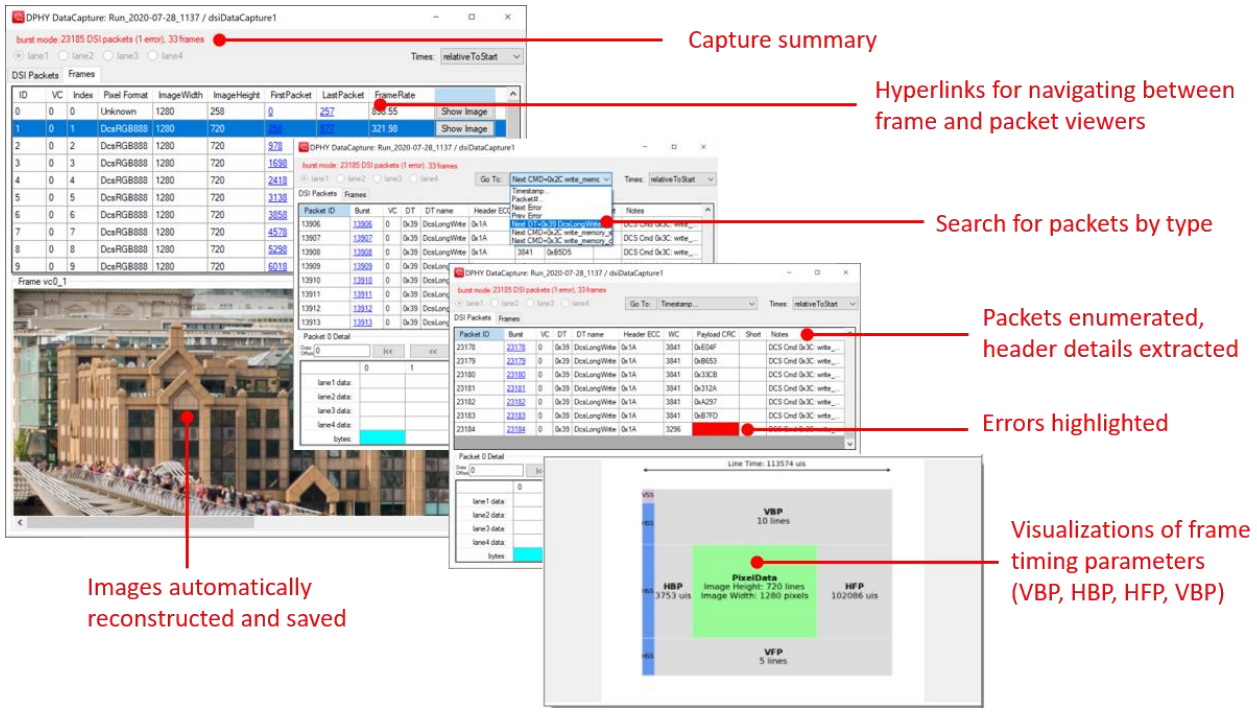

Figure 2: Packet and frame viewers in the Introspect ESP Software

HARDWARE CRC CHECKING AND PACKET ERROR RATE TESTING

A fundamental feature of the SV4E-DPRX MIPI D-PHY Analyzer is hardware-based packet error-rate test (PERT) capability. Similar to the traditional BER test, the PERT enables the measurements of real D-PHY transmissions from CSI or DSI generators. As illustrated in Figure 3, the Analyzer detects and filters all signal waveforms and compares only the packet data transmitted between SOT and EOT, registering errors after the data has been merged between lanes, thereby comparing errors in packets rather than bits.

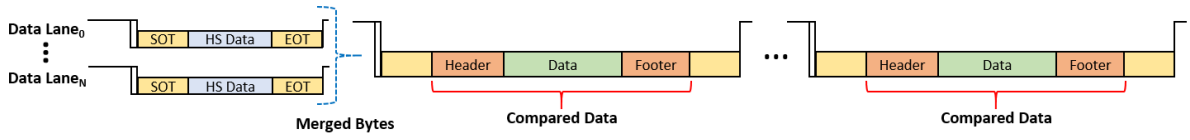

Figure 3: Illustration of packet error rate testing

ADVANCED TRIGGER MODES

Figure 4 shows the Introspect ESP Software user interface for defining the trigger mechanisms within the analyzer. At the highest level, the analyzer can be programmed to perform immediate captures (in which all data is measured irrespective of LP transitions) or triggered captures. Both are as illustrated in Figure 5.

In triggered capture modes, the D-PHY analyzer automatically handles LP and HS received signals and resistor termination. The analyzer waits for a valid LP to HS entry sequence before enabling a capture, and when a valid HS-entry transition is detected, the capture starts immediately. If no valid HS-entry transition is detected, the capture returns an empty array.

Table 2 provides a list of trigger conditions that are available in the Analyzer. The duration of data captured previous to the trigger condition is specified in software by “preTriggerDuration” settings. The duration of data captured after the trigger condition is specified in software by “postTriggerDuration” settings. The specification of post trigger duration is described in the following section.

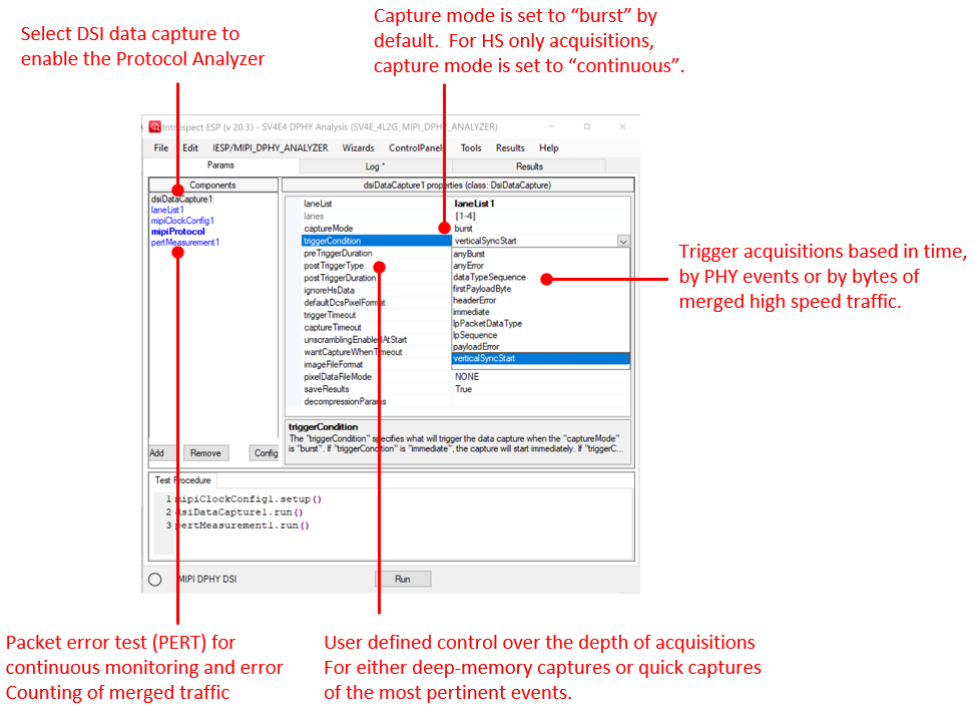

Figure 4: Introspect ESP GUI for the SV4E-DPRX. Top left: Components window, showing selected CSI, DSI and PHY data acquisition methods. Top right: Properties window, showing DSI Data Capture. Bottom: Test Procedure window, with Python code calling components.

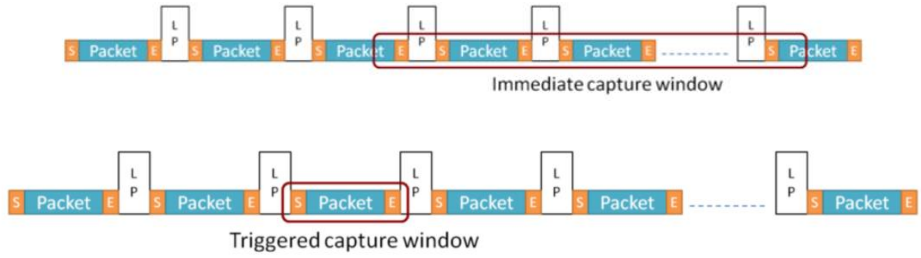

Figure 5: Illustration of multi-packet, per lane PHY-level capture (top) and triggered packet capture (bottom)

TABLE 2: TRIGGER CONDITIONS

TRIGGER CONDITION NAME	TYPE OF EVENT	TRIGGER DESCRIPTION
immediate	Time-Based	time-base acquisition, beginning immediately
anyBurst	PHY	the first high-speed burst recorded on any data lane
lpSequence	PHY	user-defined sequence of LP states, e.g. “111,001,000” reflects a proper LP-HS entry sequence
anyError	CSI, DSI	the first error is registered: header, CRC or payload
dataTypeSequence	CSI, DSI	user-defined integer value to be identified in a packet header
headerError	CSI, DSI	protocol layer, the first error recognized in a packet header
payloadError	CSI, DSI	protocol layer, the first error recognized in a packet header
firstPayloadByte	CSI, DSI	user-defined byte to be identified in the payload
lpPacketDataType	CSI, DSI	user-defined integer value to identified in LP packet
frameStart	CSI	CSI-only, any packet with header data type 0x00 indicating the beginning of a frame
verticalSyncStart	DSI	DSI-only, any packet with header data type 0x01 indicating the beginning of a frame

SPECIFYING THE ACQUISITION DURATION

The acquisition duration is determined according to the “postTriggerType”, and may be specified in terms of time, in terms of PHY events, or in terms of bytes of merged high-speed traffic. Figure 6 illustrates two methods of determining acquisition length in terms of PHY events. In Figure 6 (top), an acquisition begins on the first high-speed burst observed and completes after a user-defined number of bursts are recorded. In Figure 6 (bottom), an acquisition begins and the analyzer records for a user-defined period of N nanoseconds.

Figure 7 illustrates three examples of triggering acquisitions on merged, high-speed data. The acquisition start condition is user-defined as either: (a) an error within a packet header, (b) a variable data type identifier, here chosen as 0x01 and (c) a frame start packet (CSI only). The duration of the acquisition for each is chosen according to the number of N received: (d) bursts, (e) bytes and (f) frame end packets. Table 3 provides a list of conditions for determining the acquisition duration.

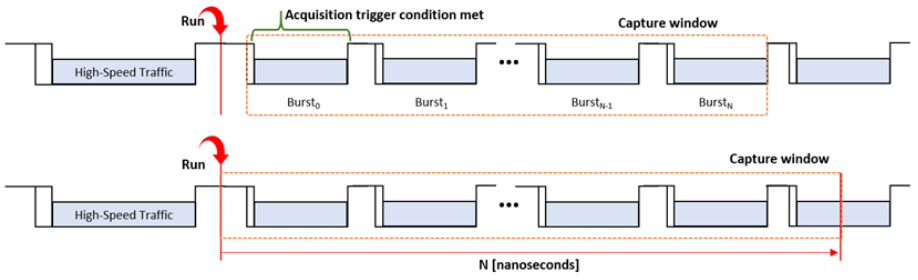

Figure 6: Illustration of two event-based acquisitions. Above, acquisition is triggered on the first observed burst and the duration is determined by a user-defined number of N bursts. Below, acquisition begins immediately, and the duration is for a user-defined period of N nanoseconds.

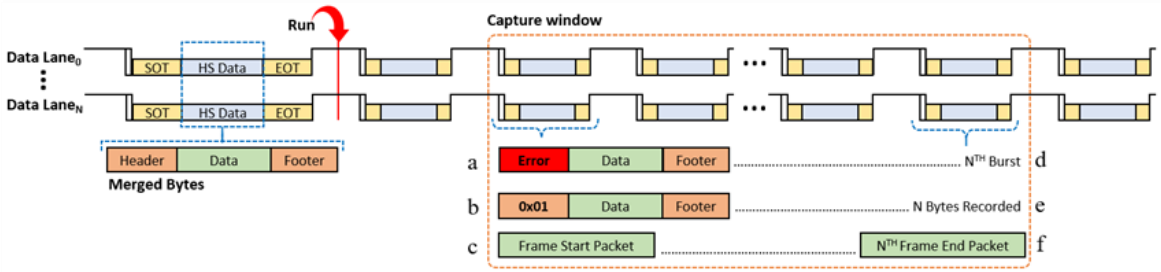

Figure 7: Illustration of three acquisitions triggered on merged high-speed traffic events: (a) a header error, (b) a user-defined data type identifier and (c) a frame start packet. Three conditions for specifying the acquisition duration are shown: (d) a user-defined number of N bursts, (e) a number of bytes, and (f) a number of frames

TABLE 3: SPECIFICATION OF ACQUISITION DURATION

SPECIFICATION OF ACQUISITION DURATION	TYPE OF EVENT	TRIGGER DESCRIPTION
durationInNs	Time-Based	time-base acquisition, defined in nanoseconds
numberOfBursts	PHY	the total number of unique bursts acquired, across all data lanes
numberOfBytes	PHY	the total number of bytes recorded between SOT and EOT of all bursts
numberOfLpCommands	PHY	the number of LP commands acquired
numberOfLpStates	PHY	The number of unique LP states, e.g. "111,001,000" would be 3
numberOfFrameEnds	CSI	protocol layer, the number of frame-end packets recorded
numberOfVerticalSyncStarts	DSI	protocol layer, the number of packets with data type identifier 0x01

PHYSICAL CONNECTIONS

Photographs showing the ports and connectors on the SV4E-DPRX Analyzer are shown in Figure 8(a) and (b). The physical connection of a typical Device Adapter Board (DAB) is shown in Figure 8(c). The DAB provides the connection to the desired customer device (eg: a sensor or display driver) under test.

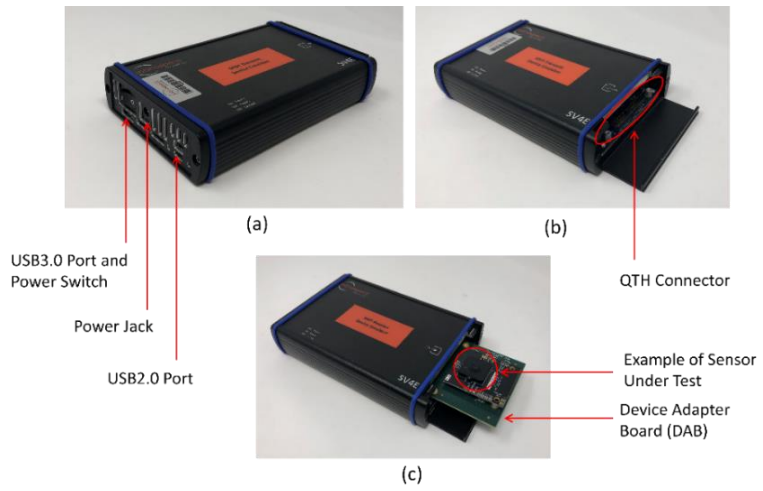

Figure 8: SV4E-DPRX Analyzer connectors: (a) Left Side (b) Right Side (c) Typical DAB Connection

QTH / QSH CONNECTOR

The SV4E-DPRX has an 80 pin, high speed connector for all inputs and outputs, with part number Samtec QTH-040-01-L-D-DP-A.

https://www.samtec.com/products/qth-dp

This part is designed to mate to a high speed connector on the customer adapter board, using the following part number: Samtec QSH-040-01-L-D-DP-A

https://www.samtec.com/products/qsh-dp

For information on QTH signals and connections, please refer directly to the SV4E-DPRX Device Adapter Board Reference Design Guide, as listed in "Additional Documentation" below.

ADDTIONAL DOCUMENTATION

SV4E-DPRX Quick Start Manual

- EN-G036E-E-19219 - SV4E-DPRX Quick Start Manual

Step-by-step guide to getting started with the SV4E-DPRX module. Includes hardware and software installation

SV4E-DPRX Device Adapter Board (DAB) Reference Design Guide

- EN-G046E-E-20085 SV4E-DPRX Device Adapter Board (DAB) Reference Design Guide

Reference document for QTH / QSH pinout and general board design guidelines.

SV4E-DPRX DAB Design Files.zip

- Includes reference schematic, layout and CAD files for an example DAB. Please contact Introspect Technology.

Specifications

TABLE 4: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol			
Physical Layer Interface	D-PHY		
MIPI Protocol	CSI, DSI		CSI-2 v1.3, CSI-2 v2.0, DSI-2 v1.1
LS/HS Handling	Automatic		
Ports			
Number of DPHY Lanes	4		4 data lanes plus 1 clock
Number of GPIO pins	16		
Pre-Defined GPIO pins	5		SV4E RESET (input) I2C Bus (SCL, SDA, master only) FRAME_START (output) LINE_START (output)
User-Defined GPIO	11		Configurable, input or output, for use as triggers or flags
Programmable On-Board Power Supplies	6		
Connections to PC for Introspect ESP Software Control	2		USB2 and USB3
Power Consumption			
DC Input Voltage	12	V	
Maximum Current Draw	1.5	A	
Symbol Rates / Frame Rates			
Minimum Data Rate	40	Mbps	Per Lane
Maximum Data Rate	2.5	Gbps	Per Lane
Minimum LP Toggle Rate	0	MHz	
Maximum LP Toggle Rate	20	MHz	

TABLE 5: CPHY RECEIVER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Coupling			
Input Impedance	50	ohm	HS transmission
	Hi-Z		LP transmission
HS / LP Voltage			
Minimum $\|V_{OD}\|$	140	mV	Measured at SV4E module connector
Maximum $\|V_{OD}\|$	300	mV	Measured at SV4E module connector
Minimum Programmable LP Threshold	0	mV	
Maximum Programmable LP Threshold	1200	mV	
Timing			
Minimum T_{LPX}	50 ns		
Minimum $T_{HS\text{-}PREPARE}$	40 ns + 4 UI		
Minimum $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$	145 ns + 10 UI		
Minimum $T_{HS\text{-}TRAIL}$	Larger of: (60 ns + 4 UI) or 8 UI		
Minimum $T_{CLK\text{-}PREPARE}$	38 ns		
Minimum $T_{CLK\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$	300 ns		
Minimum $T_{CLK\text{-}PRE}$	8 UI		
Minimum $T_{CLK\text{-}POST}$	60 ns + 52 UI		
Minimum $T_{CLK\text{-}TRAIL}$	60 ns		

TABLE 6: PATTERN HANDLING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Features			
Supported Pixel Formats (CSI)	RAW, RGB, YUV		RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20, RGB444, RGB555, RGB565, RGB666, RGB888, YUV420, YUV422
Supported Pixel Formats (DSI)	RGB YCbCr		RGB101010, RGB121212, RGB332, RGB565, RGB666, RGB888, YCbCr420_12bit, YCbCr422_16bit, YCbCr422_20bit, YCbCr422_24bit
Decompression Support (DSI)	Yes		DSC, V-DCM
Display Command Set (DSI) Support	Yes		
Memory Depth	1	GByte	For received packet data

TABLE 7: PACKET AND FRAME ANALYSIS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Features			
HS Data Rate Detection	Yes		Automatic
CSI / DSI Packet Analysis	Yes		Header, Payload, ECC extraction Data type detection Virtual channel support
Frame Analysis	Yes		Image width / height detection Pixel format detection Frame rate detection
CRC and ECC Analysis	Yes		Payload error detection Header error detection Packet error statistics
Trigger Conditions for Data Capture	Yes		Refer to Table 2
Specification of Data Acquisition Duration	Yes		Refer to Table 3

TABLE 8: PROGRAMMABLE POWER SUPPLY SPECIFICATION

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
General Performance			
Number of Programmable Power Supplies	6		Each supply programmed independently
Minimum Voltage	1000	mV	
Maximum Voltage	5000	mV	
Voltage Programming Resolution	1	mV	
Maximum Output Current	3.0	A	Per supply
Current Measurement Capability	Yes		Independent measurement provided on each programmable supply
Minimum Current Measurement	50	mA	
Current Measurement Resolution	4	mA	

TABLE 9: I2C BUS AND GENERAL GPIO CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Voltage			
Voltage Level	2.5	V	All GPIOs operate at 2.5 V LVCMOS
V_{IL} minimum	-0.3	V	
V_{IL} maximum	0.7	V	
V_{IH} minimum	1.7	V	
V_{IH} maximum	3.3	V	
V_{OL} maximum	0.4	V	
V_{OH} minimum	2.0	V	

Revision Number	History	Date
1.0	Document Release	September 22, 2020

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