GRL USB Type-C Power Delivery and Alt Mode Test Method of Implementation (MOI) and User Guide

for GRL Power Deliver Compliance Test Software and USB Type-C Test Controller

(GRL-USB-PD, GRL-USB-PD-C1)

This material is provided as a reference to install Rev 1.2 of Granite River Labs (GRL) USB-PD Power Delivery Compliance Test Software.

For software support, contact support@graniteriverlabs.com.

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Revision Record

Version	Revision Date	Description of Changes	Author(s)
1.2.0	1/2/2015	GRL-USB-PD Rev1.2 SW Release	mikeen@graniteriverlabs.com
1.2.1	4/11/2016	Add firmware & FPGA updating	baltmann@graniteriverlabs.com
1.2.2	6/03/2016	Update for Rev 1.2.2 Software	mikeen@graniteriverlabs.com
1.2.3	9/12/2016	Update for Rev 1.2.3 Software	sky@graniteriverlabs.com mikeen@graniteriverlabs.com
1.2.4	9/28/2016	Update for Rev 1.2.3.12 Software	sky@graniteriverlabs.com
1.2.4.4_03	1/04/2017	Update for Rev 1.2.3.4 Software	sky@graniteriverlabs.com mikeen@graniteriverlabs.com
1.2.4.5_1	04/06/2017	Update for Rev 1.2.4.5 Software	sky@graniteriverlabs.com
1.2.4.5_2	08/08/2017	Update for USB PD Compliance MOI version 1.06	sky@graniteriverlabs.com

1 Reference Documents

The test methods outlined in this document are tests required by various technology adoptions of the USB Type-C Connector. Specifications that have adopted the USB Type-C Connector and may be referenced in this document include, but are not limited to, the following specification versions.

Note: In order to have access to all specifications, it may be required that you are a member of an industry group and have attained the proper permissions.

1.1 USB-IF

All of the following specifications are part of the USB3.1 Specification download at:

http://www.usb.org/developers/docs/

Type-C Cable and Connector Specification

USB Power Delivery Specification Rev2 Version 1.2

USB-PD Compliance Test Plan Rev 1.0, Version 2.0, June 2016

USB-C_Source_Power_Test_Specification_2017_03_03, version 0.71

PD Communications Engine USB PD Compliance MOI March 24 2017, Version 1.06

1.2 VESA and Display Port

Download the Display Port document from the VESA web site:

http://www.vesa.org/join-vesamemberships/member-downloads/?action=stamp&fileid=3033

Display Port Alt Mode on USB Type-C Standard, Ver.1.0a, August 5th, 2015

2 Scope of this MOI and Quick Start Guide

This MOI (Method of Implementation) and Quick Start Guide serves as the primary user documentation for GRL-USB-PD Compliance Test Software and GRL-USB-C1 USB Type-C Test Controller Hardware. It also provides the technical implementation detail for testing to the various specifications. The subsequent sections provide step-by-step test procedures for specific tests in Test Plans and Compliance Test Specifications for USB Type-C technologies.

The Appendices provide additional technical information and user guidance that falls outside the general flow of testing to the test specifications.

3 Getting Started with GRL-USB-PD Test Solution

This section describes in detail how to get started with the GRL-USB-PD test solution for USB-PD compliance testing. Whether you are installing for the first time or doing an upgrade, please make sure to follow all the steps in this section to verify your setup prior to testing a DUT. The procedure is as follows:

1. Install the latest version of GRL-USB-PD SW.
2. Activate the license if necessary (if needed).
3. Update the GRL-USB-PD-C1 Controller Firmware. Refer to section 3.3
4. Setup Oscilloscope VISA Communication with GRL-USB-PD Software. Refer to section15
5. Setup Electronic Load VISA Communication with GRL-USB-PD Software. Refer to section15
6. Calibrate the Noise Source Board. Refer to section **Error! Reference source not found.**
7. In case the signal is not captured in the oscilloscope run Verify Test Setup, Refer to section 4.9
8. Perform a test on the 25cm GRL EMark Cable. Refer to section 5.2If this procedure is followed and any issues arise, please contact support@graniteriverlabs.com.

3.1 Install GRL-USB-PD Software

1) Download the GRL-USB-PD Software from the **Trials and Licenses** tab at http://graniteriverlabs.com/usb-pd/ from Support Tab.
2) On the Win7 (or above) Oscilloscope to be used for testing, create a folder with an executable of the software.

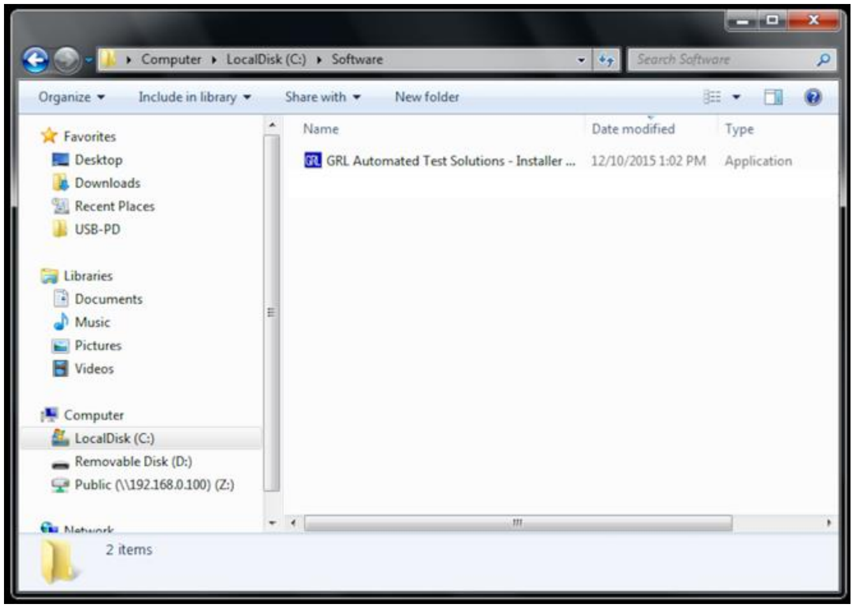
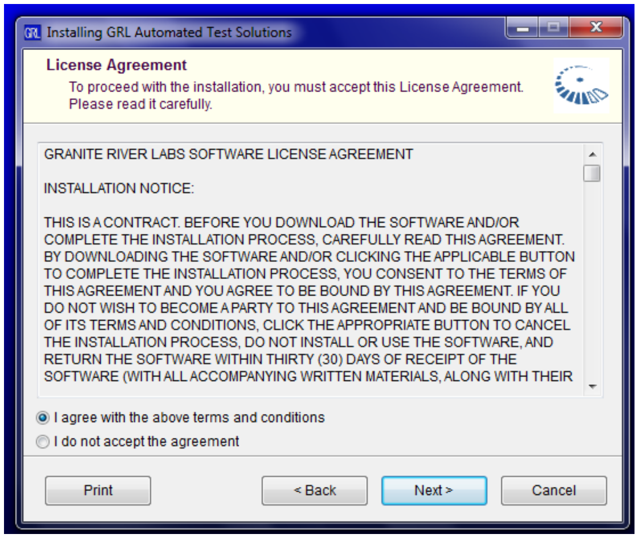


FIGURE 1: INSTALLING GRL-USB-PD SOFTWARE

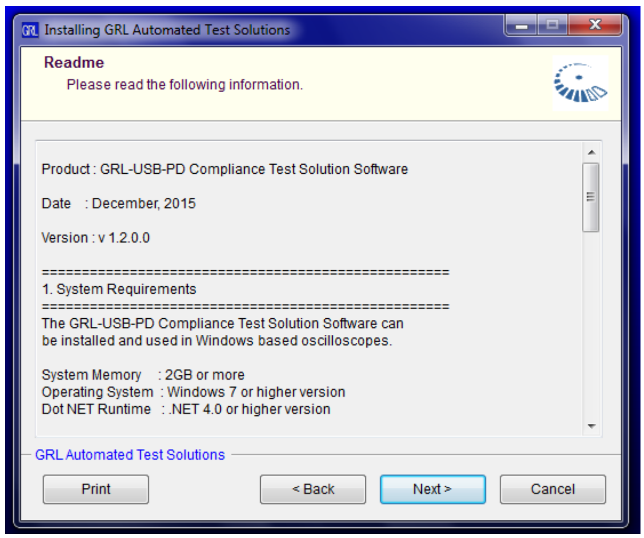
3) Run the Executable to Install the Software. You will see the following screens during installation:

1. Welcome to GRL Automated Test Solutions Software:

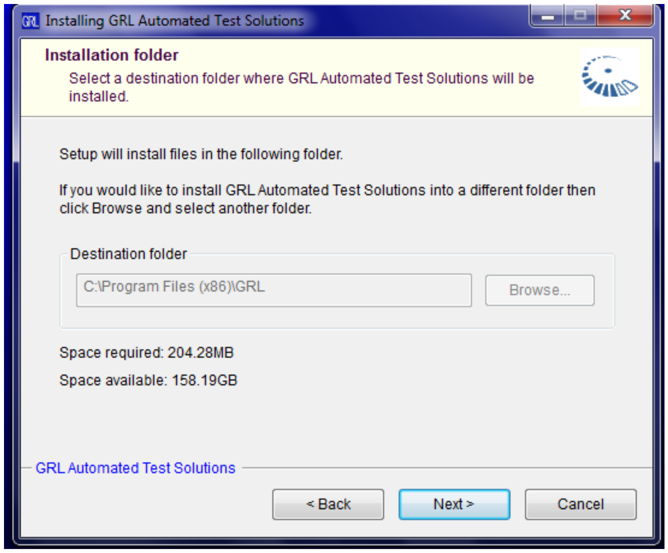
2. License Agreement:



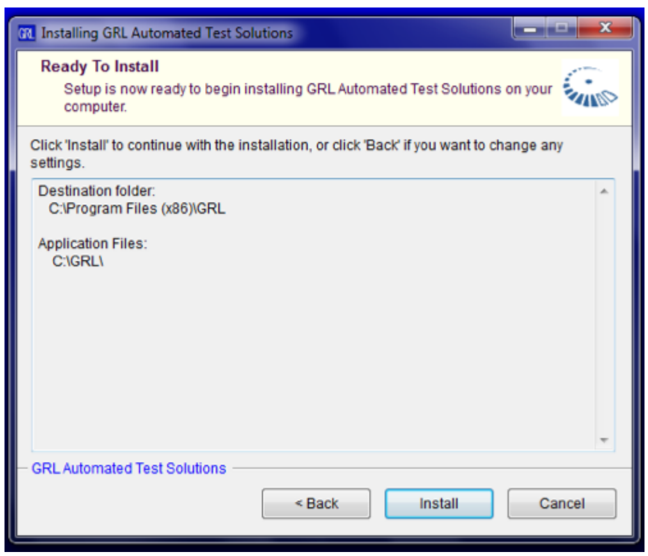
3. Readme:



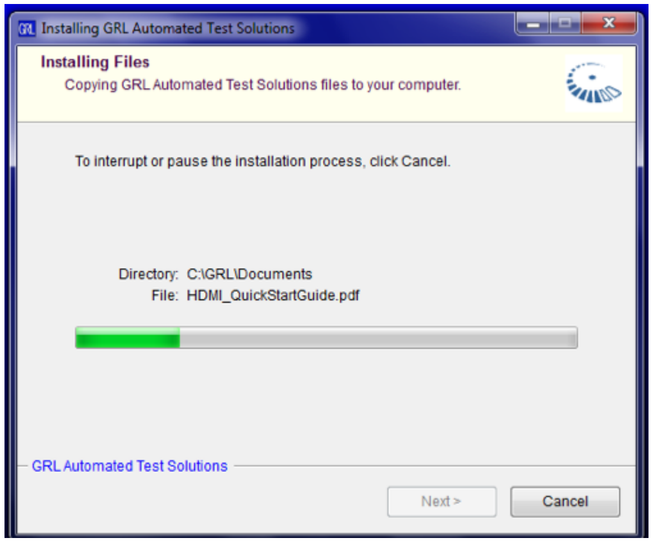
4. Installation Location:



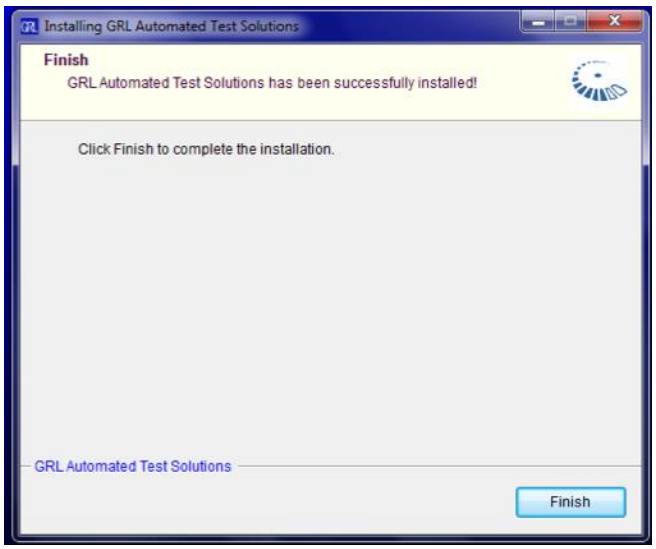
5. Ready to Install:



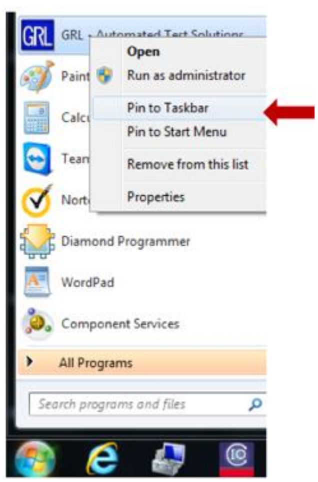
6. Installing:



7. Finish:



4) In Windows, Pin GRL Software to Task Bar for easy access.

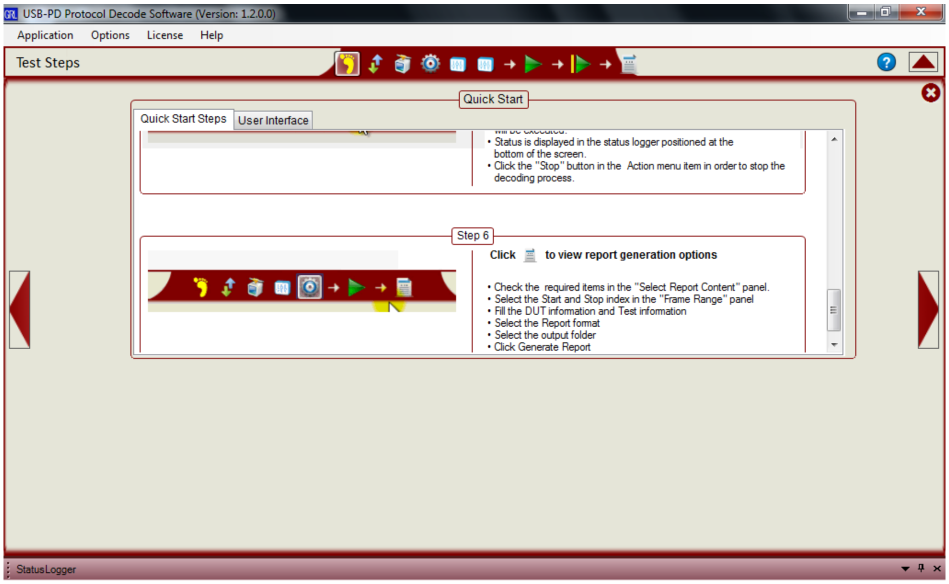


3.1.1 GRL-USB-PD Software Navigation

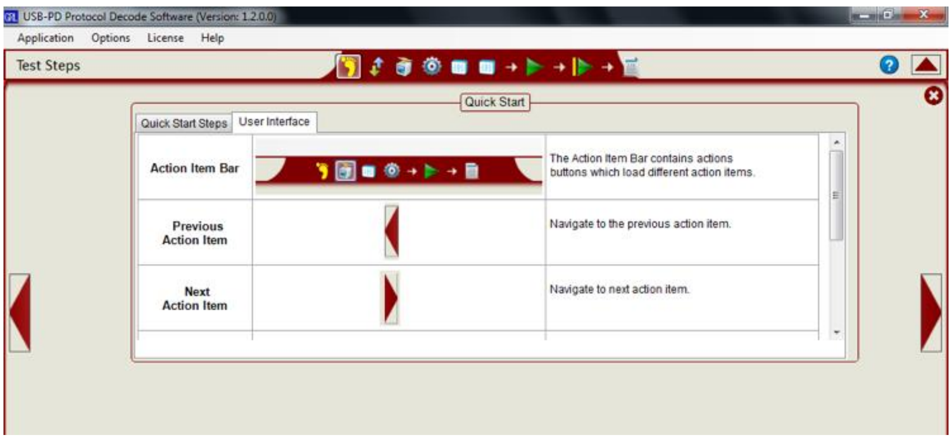
5) Launch the SW by choosing the GRL Icon on the Windows Task Bar.

6) Once SW launches, the **Test Steps** menu will appear.

1. **Quick Start Steps** - This menu gives a tutorial on the test steps navigation buttons that appear across the top of the application.



2. **User Interface** - This menu shows how to navigate the GRL-USB-PD SW. You can navigate left to right on the top menu or use the Previous and Next buttons on each side of the application to navigate to the left and right.



3.2 GRL-USB-PD Software License Activation (if needed)

There are two Licensing options for GRL-USB-PD. Option (1) is a 'node locked license' that is assigned to the host Oscilloscope's MAC Address through an encrypted key; in this case the software can only be used on the host oscilloscope. Option (2) is a USB Dongle HW 'single user license'; in this case the software license can be moved from oscilloscope to oscilloscope in the lab for testing, or can be used on a separate PC for post-processing saved waveforms.

7) For Option (1) – Node Locked License, follow this procedure to activate either a Permanent License or a Demo License.

   - Permanent License – Available to customers who have purchased the SW from GRL or Instrument Vendor.

   - Demo License – Time Limited license available from GRL for customer evaluation or Sales demo purposes.

1. Go to the License > License Details.

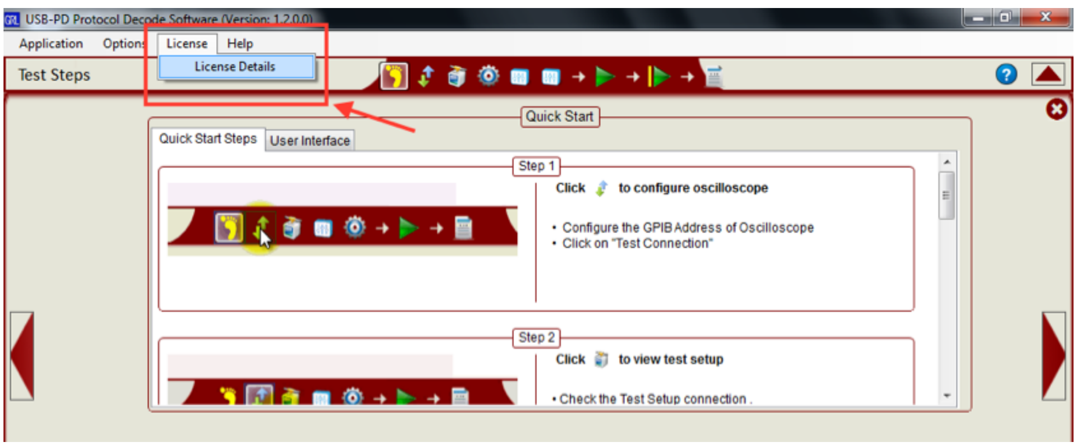
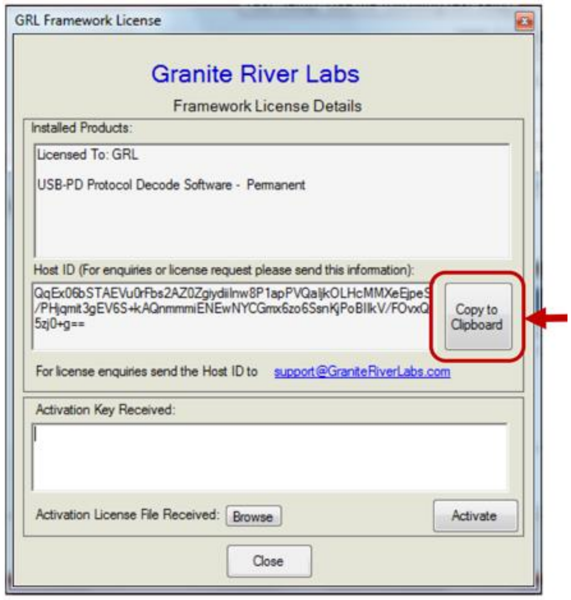


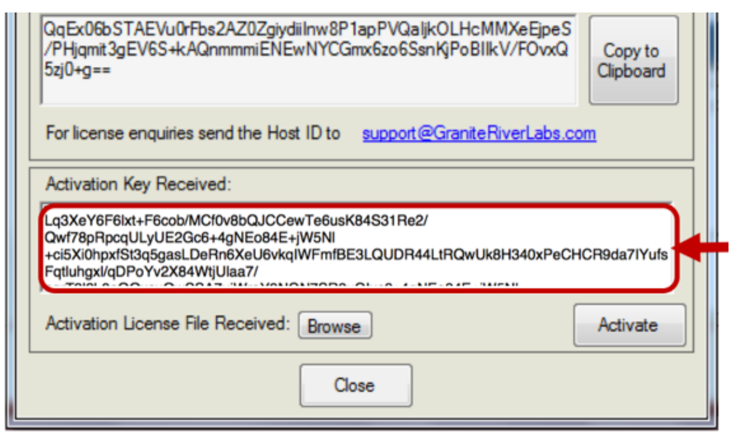
FIGURE 2: ACTIVATING GRL-USB-PD SOFTWARE LICENSE

2. In the GRL Framework License Window:
   i) Copy the existing Host ID to the PC's Clipboard using **Copy to Clipboard**.

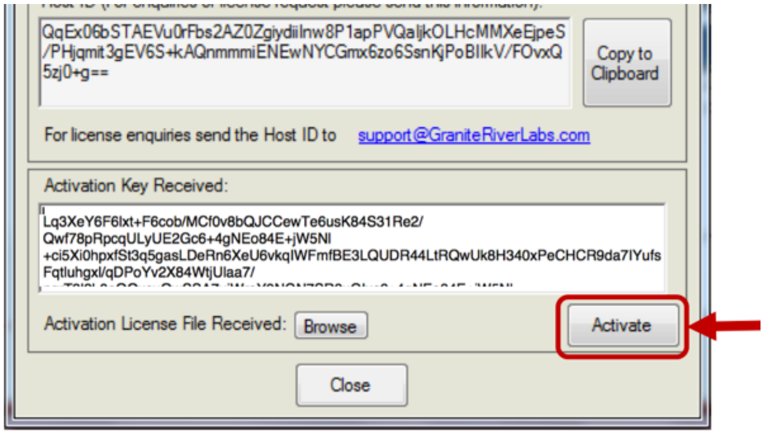


   ii) Click on the support@GraniteRiverLabs.com link to open your PC's email.

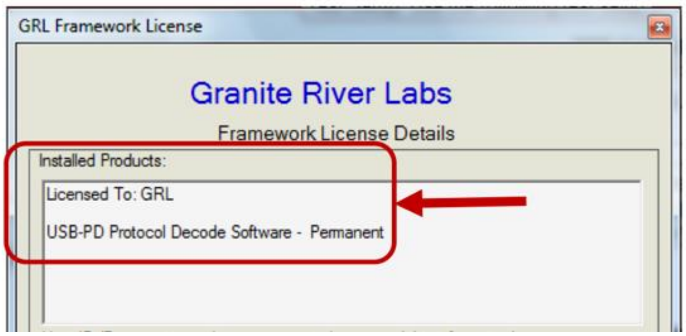
   iii) Paste the Host ID into the email body.
   iv) Send the email to GRL.
   v) You will receive an email response with and updated Host ID string.
   vi) Copy and Paste the new Host ID string into the **Activation Key Received** field in the application.



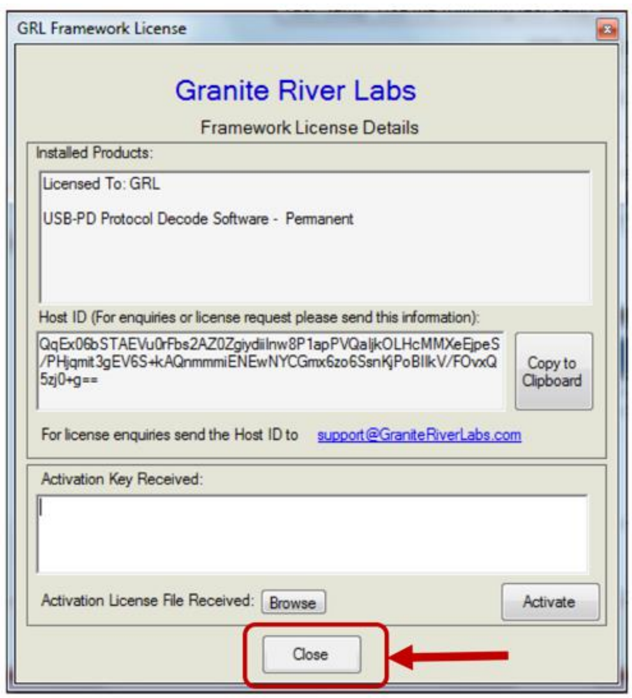
vii) Click on the **Activate** Button.



viii) Activation Status will appear under the Installed Products field.



ix) Click the **Close** button to begin using the Licensed application.



8) For Option (2) – Single User USB Dongle License, it is not necessary to contact GRL for a license.

1. Download and install the software.
2. Insert the USB dongle in any one of the Scope's USB ports.
3. Open the application and start using it.

3.3 Update GRL-USB-PD-C1 Firmware and FPGA

Along with each GRL-USB-PD software revision, a new version of FW and FPGA code is provided. Use the following procedure to update the controller's firmware and FPGA code.

1) Install the latest USB-PD Compliance Test Solution software.
2) Launch the application and Click "Update Firmware" button in "Scope Connection Setup" Menu as shown.

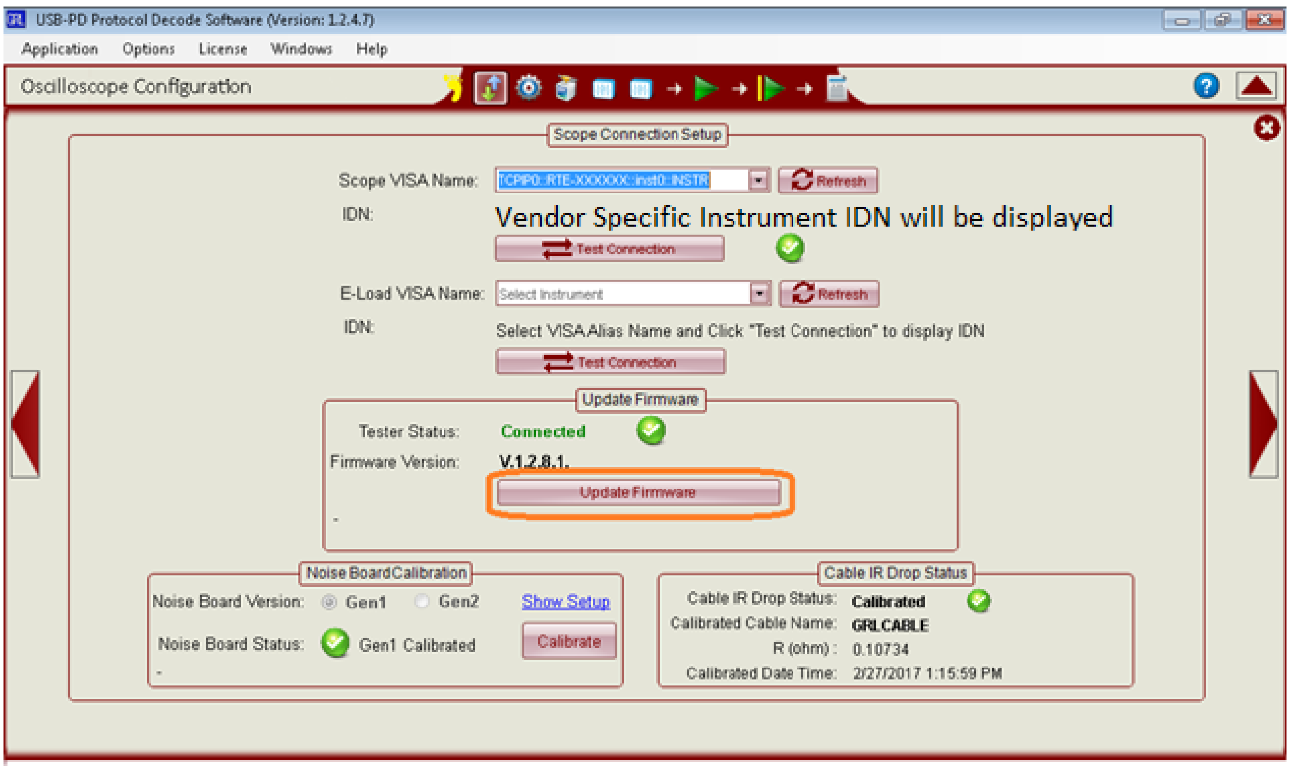
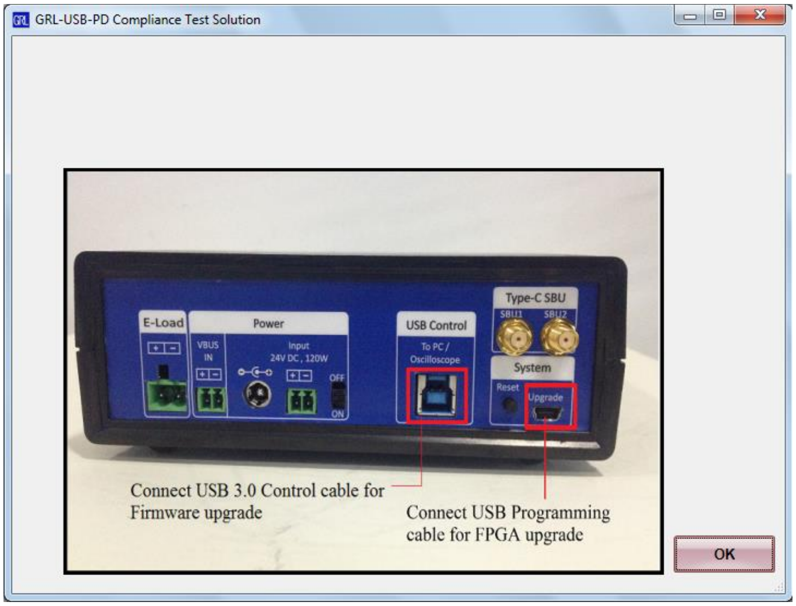
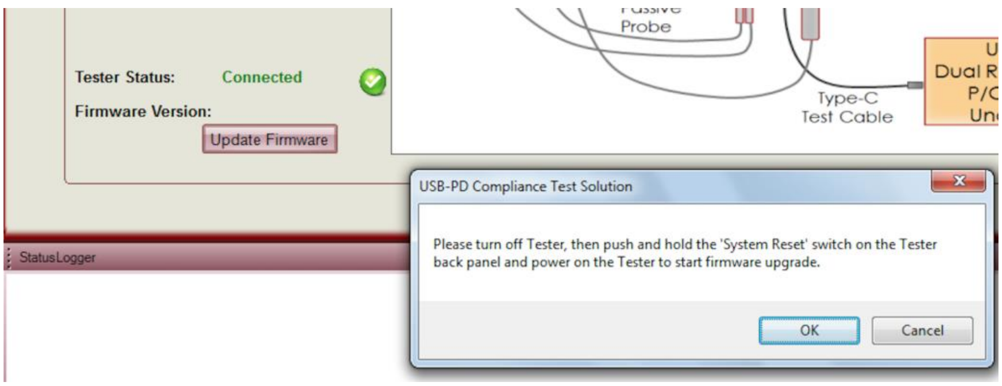


Figure 3: Oscilloscope Configuration Window for Updating the Firmware

3) Pop up appears; ensure that the USB 3.0 Cable is connected to the Scopes **USB3.0** or **USB2.0** Port. Ensure that the mini-USB Cable provided with the GRL-USB-PD-C1 controller is connected to a **USB2.0** port on the Scope.

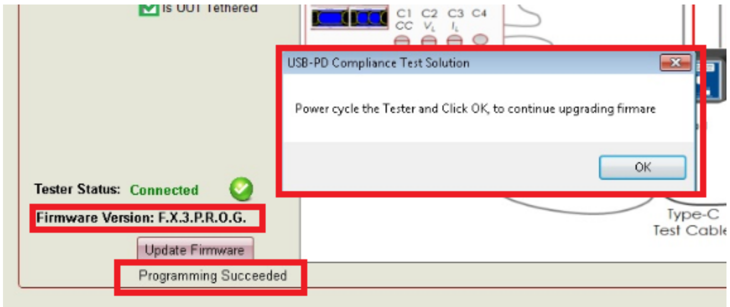


4) Pop up appears as shown below. Turn off the Controller (Tester) using "On/Off" switch, hold "Reset" button down in the rear panel on the controller and power on the Tester. Verify Tester Status is 'Connected' and press OK.

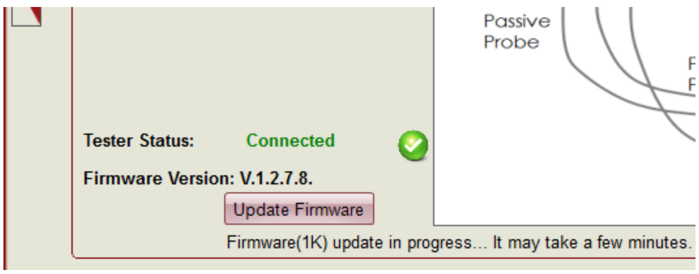


5) Observe "CC Line" LED of the front Panel, starts blinking to ensure Application Processor entered in to Boot Mode, Firmware version will appear as "F.X.3.P.R.O.G". As shown in **Error! Reference source not found.**. While updating firmware status appears a s "Firmware update in progress".

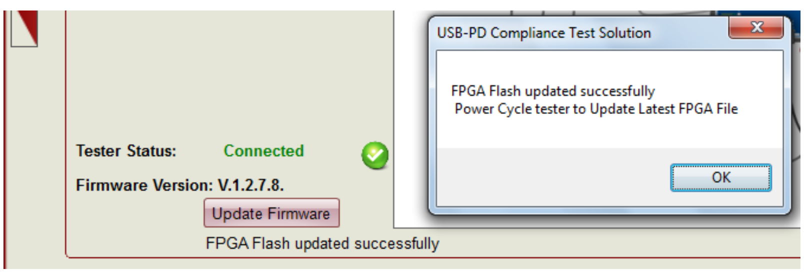
6) Application Processor Firmware completes as shown below. To perform FPGA update Application must not be in Boot mode, a popup appears as shown below, **Turn Off** and **Turn On (without holding Reset switch)** the tester and press OK.



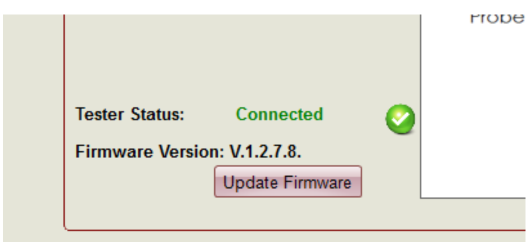
7) FPGA update starts with the status as shown below. During this step, two FPGA's such as 1K and 8K will be updated. Observe status message for both the devices.



8) Once FPGA Flash is completed, you will get a Pop-Up as follows. Press OK.



9) Reset Controller by Toggling the On/Off button one last time. Then Controller is updated and ready for use.



3.4 Calibration of the BMC-RX Noise Source Generator

The procedure to calibrate the voltage reference of the Noise board is required when the Controller is used for the first time or replaced with a different one. The calibrated Voltage reference value and Amplitude of the connected Controller will be retained in the software. Upon changing the Controller, the user has to calibrate the new Controller again. The Trigger Channel is checked and set to CH4 as shown in Figure 13. Make sure that the Controller is Reset before starting the Noise Calibration.

Note: Noise calibration for Gen2 is under development. This feature would be supported in future release.

Step 1: Remove the DUT or cable and make sure nothing connected on Port A as shown below and power cycle the controller once. Make sure to Connect Controller USB cable to USB 2.0 port of scope.

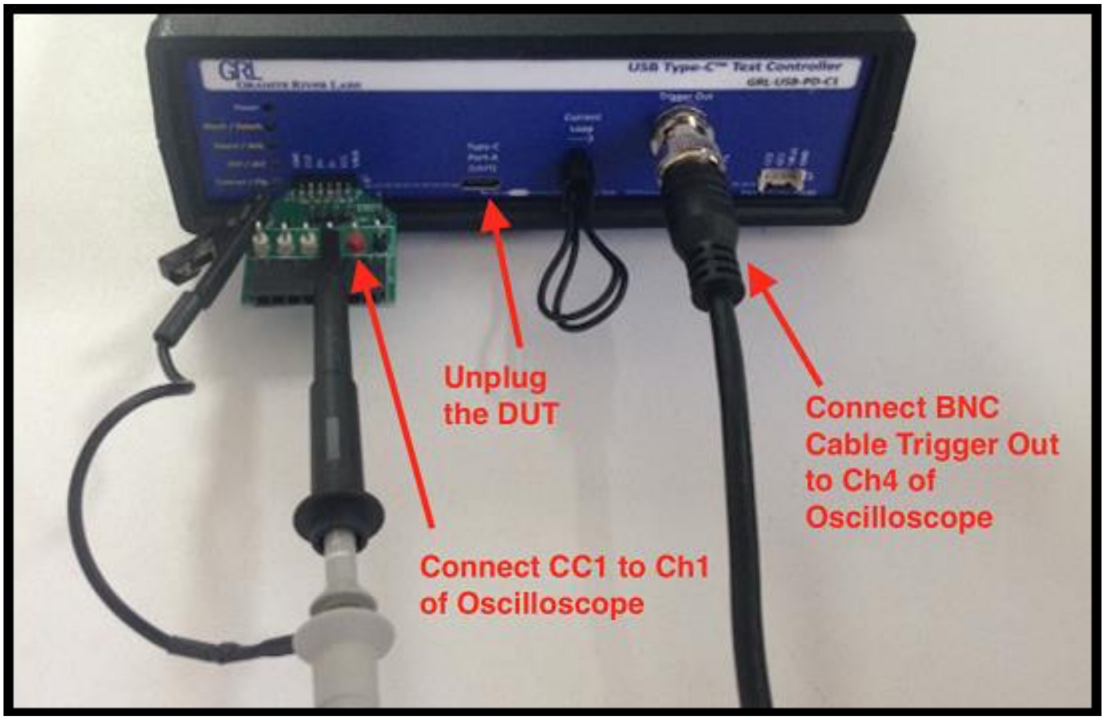
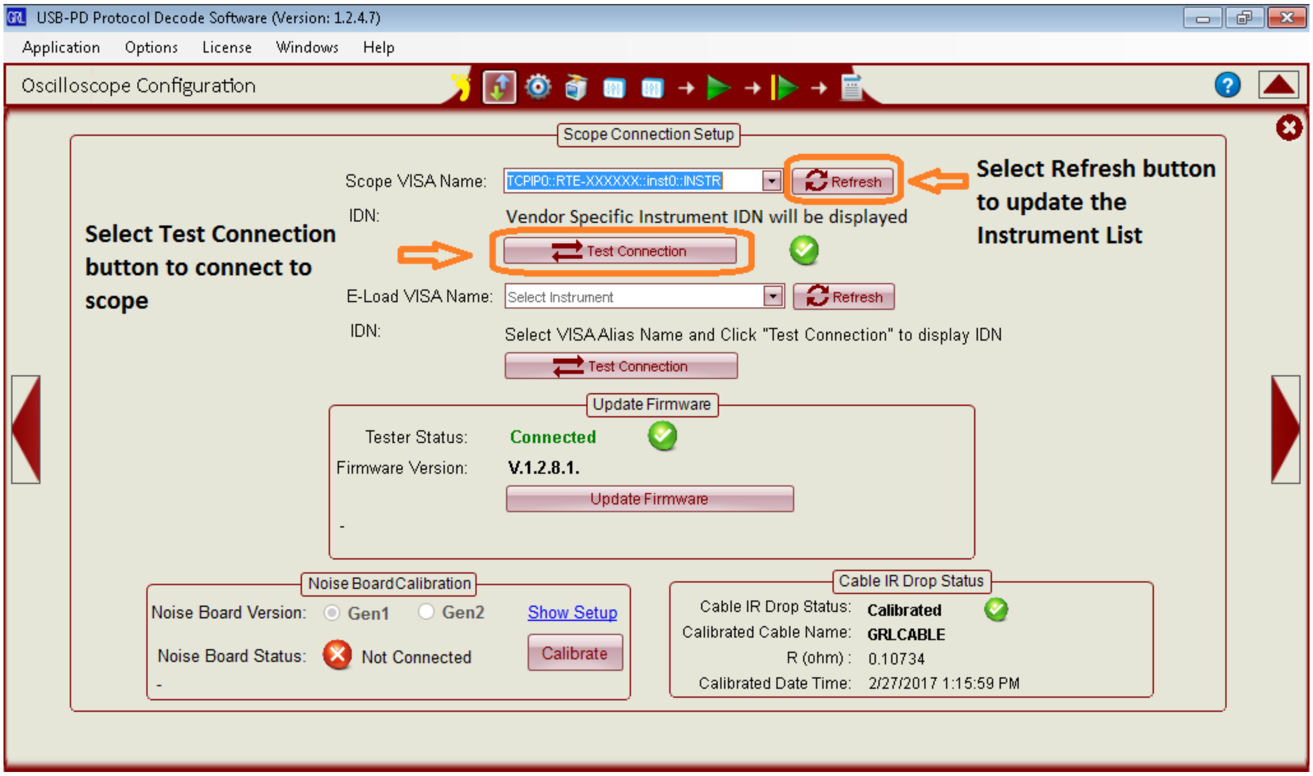
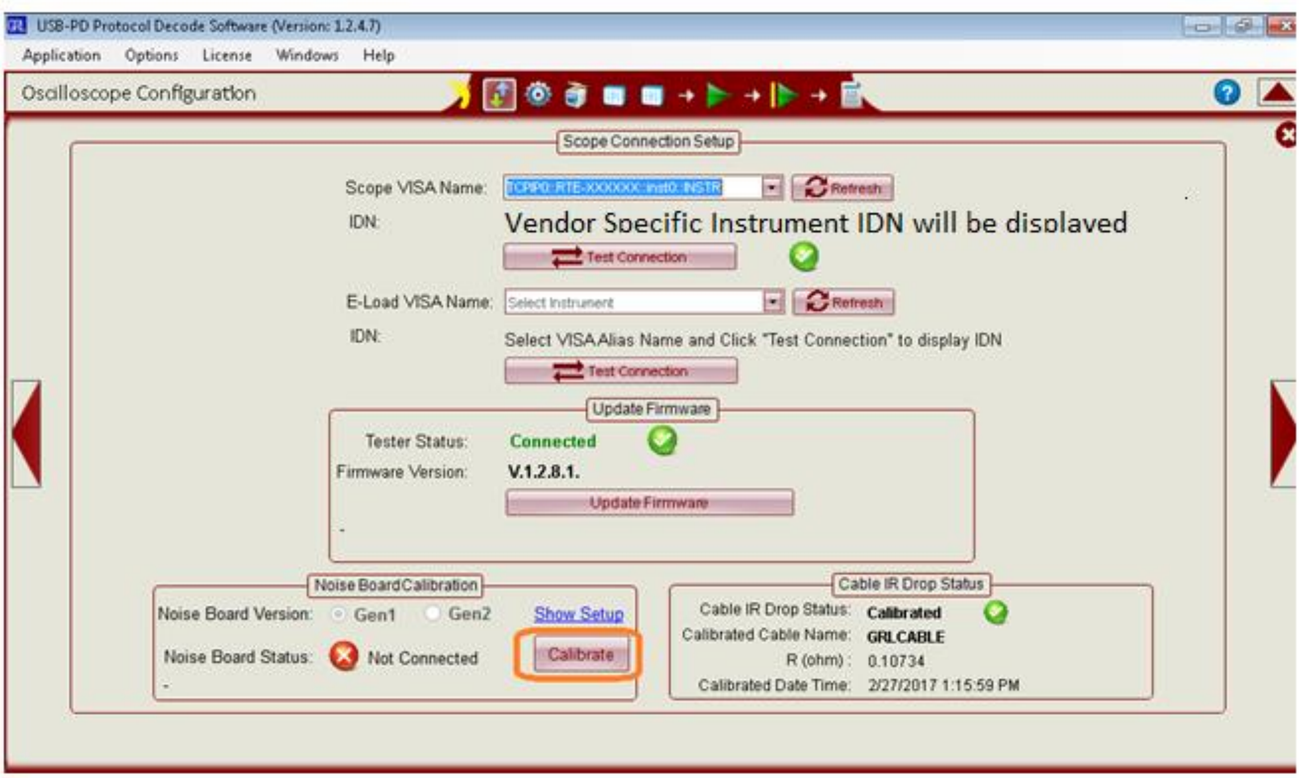


FIGURE 4: RECEIVER NOISE SOURCE CALIBRATION SETUP

Step 2: Open GRL Application and Click Refresh button in Oscilloscope Configuration panel and connect scope as shown in below figure.

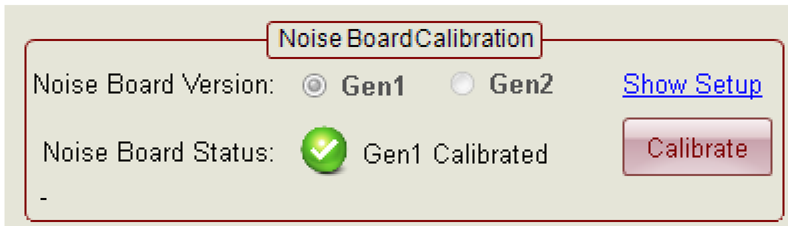


Step 3: Click on Calibration button as shown below

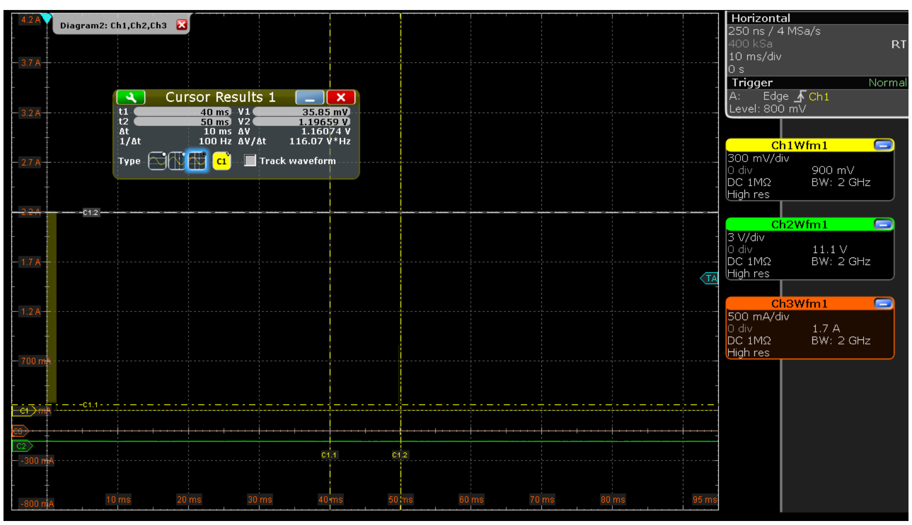


Step4: Group Noise calibration would start first followed by BUSIDLE Calibration .This process could take some time. Message box showing “Noise Calibration Succeeded” would appear.

Step 5: Once the BUSIDLE calibration completes, Noise Board status updates as Gen1 calibrated as shown below



Step 6: The following figure is the snapshot of the oscilloscope showing the voltage levels after the completion of Calibration. The Peak to Peak Noise Source Amplitude should be in the range of 1.04V to 1.20V for the Calibration to succeed.



In case of Failure Please Contact support@graniteriverlabs.com for further support.

4 Connection and Setup of Hardware

Figure 6 shows an example setup for testing a USB-PD Provider/Consumer or Dual Role Device.

The GRL-USB-PD Software, which is loaded on a Win7 (or higher) oscilloscope’s operating system, uses the oscilloscope’s instruments VISA (Virtual Instrument Software Architecture) to automate the following equipment for testing using GPIB (General Purpose Interface Bus) commands. Below is a procedure for connecting HW and verifying proper HW connections.

1) Connect Power Supply to Controller.
2) Connect the GRL-USB-PD-C1 Controller using physical USB connection to the Scope.
3) Setup the Oscilloscope and Electronic Load (eLoad) using its internal GPIB/VISA connection.
4) Verify the Controller's USB drivers are properly installed on the Scope's OS.

Note: Automation of Power Supply switching in the GRL-USB-PD-C1 is handled internally to the controller unit. Thus, there is no USB or GPIB connection attached to the Power Supply.

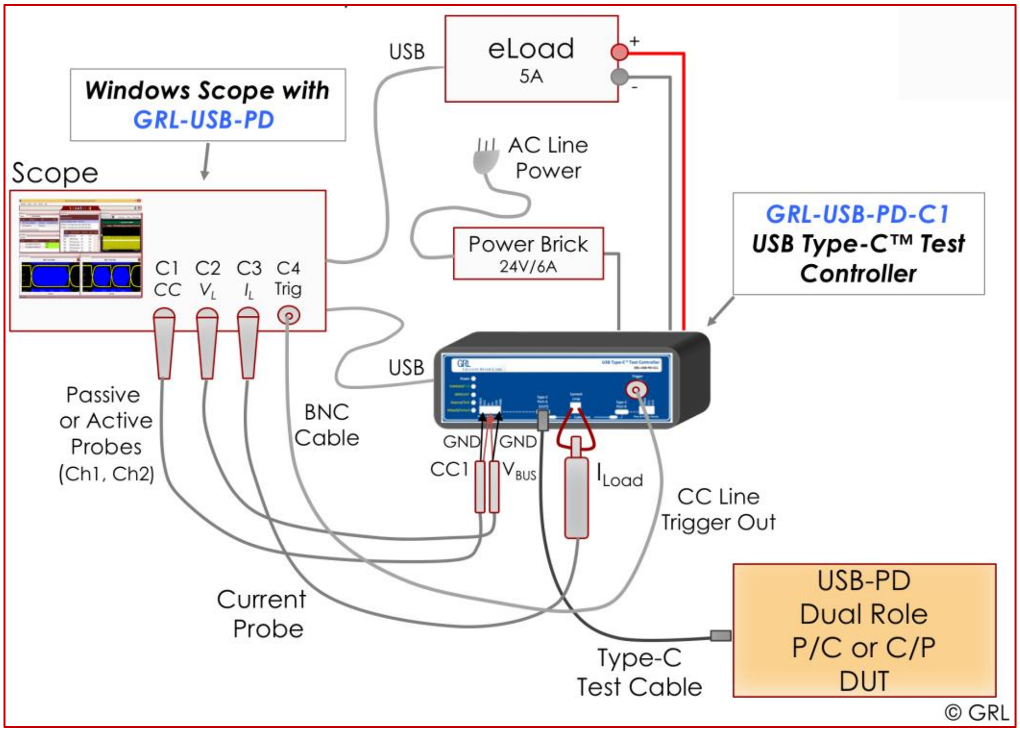


FIGURE 5: HARDWARE SETUP FOR PROVIDER/CONSUMER OR DUAL ROLE DEVICE

4.1 Connect Power Supply to Controller

To setup the GRL-USB-PD-C1 Test Controller, do the following:

1) Connect the GRL-USB-PD-C1 Power Interface using one of three methods:

1. Using the 24V, 120W Power Brick included with the controller (recommended for most applications),
2. Using a Lab Power Supply (24V, 120W) to connect to the '+' and '-' terminals of the controller, or
3. Using a Lab Power Supply to connect Vbus directly to the '+' and '-' terminals of the controller.

GRL-USB-PD-C1 Rear Panel

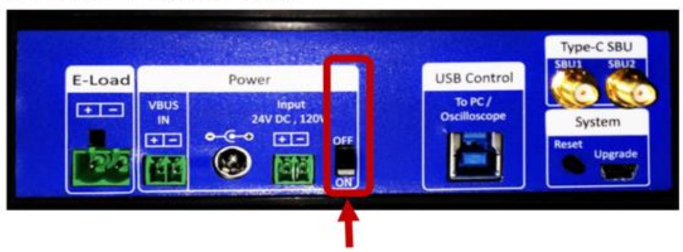
4.2 Connect USB Cable and Turn On Controller

2) Connect the GRL-USB-PD-C1 Device (Type-B) connector to one of the oscilloscope's USB Host (Type-A) connector using a USB2.0 or USB3.0 Cable.

GRL-USB-PD-C1 Rear Panel

3) Turn on the GRL-USB-PD-C1 controller using the On/Off button.

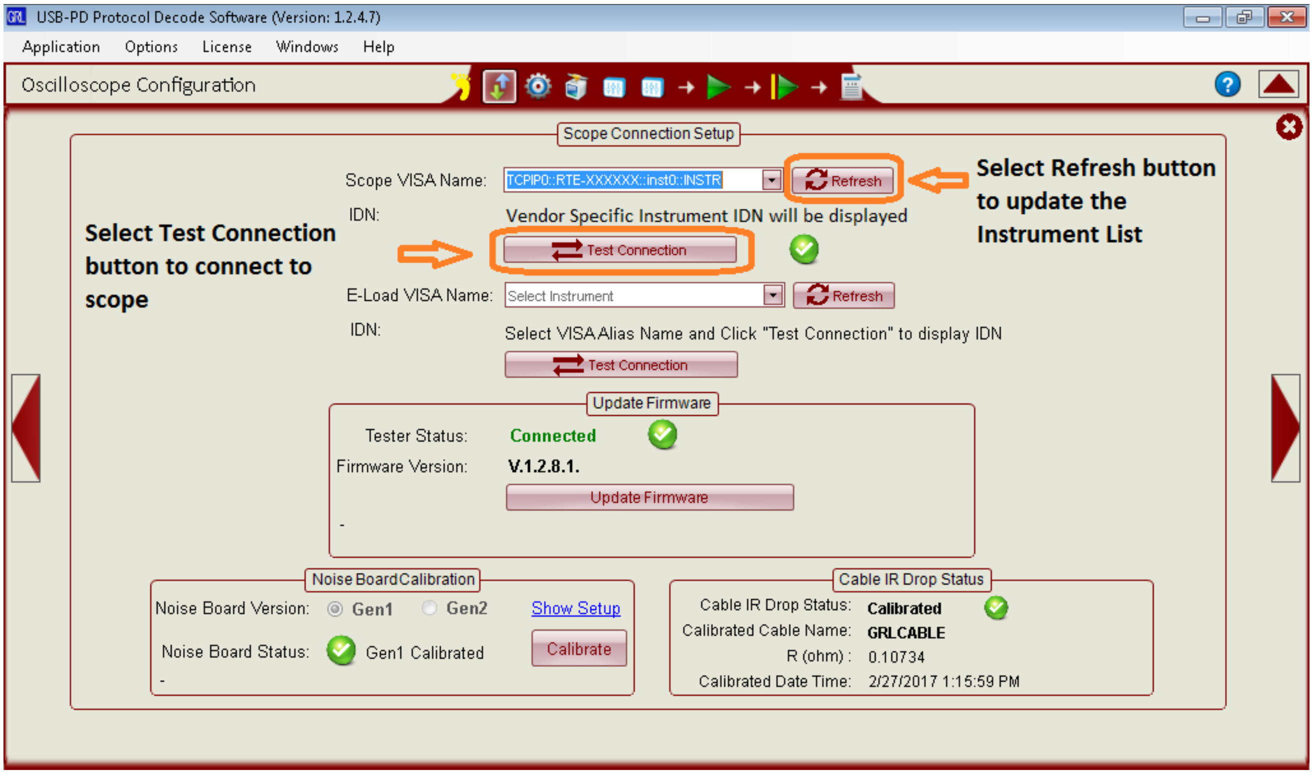
GRL-USB-PD-C1 Rear Panel



4.3 Oscilloscope and eLoad Connection Setup

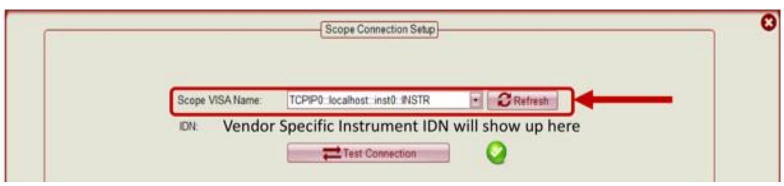
To setup the Oscilloscope do the following:

4) Select the **Scope Connection** Setup menu (second icon from the left).

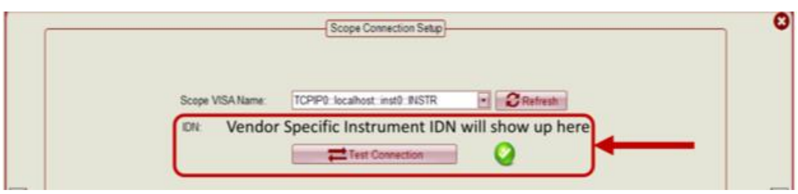


5) Press the **Refresh Button** next to the **Scope VISA Name** to refresh the connected instruments.

6) If there are multiple VISA Instruments connected, select the **TCPIP0: localhost** from the pull down menu, which is the Internal GPIB connection to the oscilloscope.



7) Press the **Test Connection Button** to verify the connection. The **green icon** will show up when it is verified.

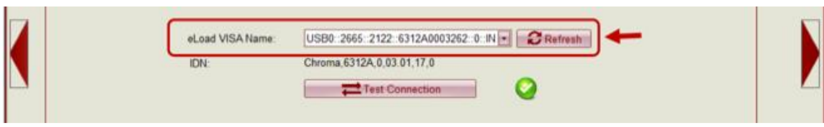


The Oscilloscope is now setup.

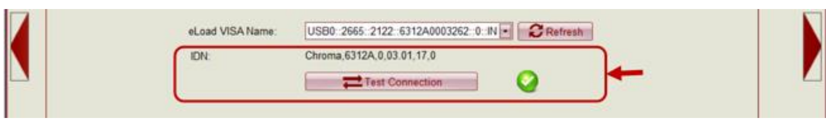
To setup the eLoad do the following:

8) As in the above diagram, connect the '+' and '-'Terminals of the eLoad to the eLoad terminals on the rear panel of the GRL-USB-PD-C1 controller. Refer to the readme.txt file for supported electronic loads.

9) Connect the eLoad's USB Device (Type-B) connector to one of the oscilloscope's USB Host (Type-A) connector using a USB2.0 Cable.
10) Make sure the USB driver for the eLoad being used is installed on the oscilloscope's OS.
11) In the GRL-USB-PD Software, Press the **Refresh Button** next to the **eLoad VISA Name** to refresh the connected instruments.



12) Press the **Test Connection Button** to verify the connection. The **green icon** will show up when it is verified.



4.4 Verifying GRL-USB-PD-C1 Windows Driver Installation

The USB drivers for the GRL-USB-PD-C1 Controller are automatically installed to the oscilloscopes OS with the GRL-USB-PD software installation.

When the USB connection is made between the Oscilloscope and the Controller unit using the blue USB3.0 cable, the drivers will be automatically updated. It may take some time for the Windows OS to update the drivers the first time the controller is connected.

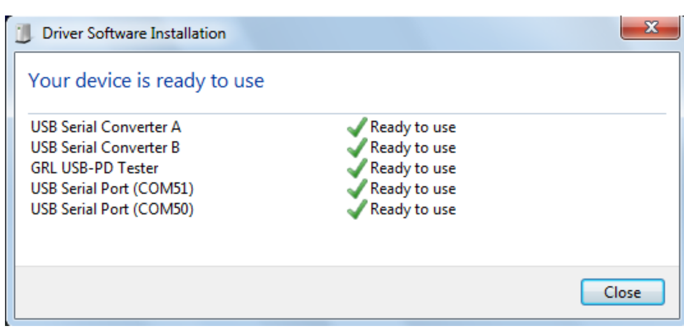


FIGURE 6: INSTALLATION OF USB DRIVERS WHEN INITIALLY CONNECTED

Before proceeding with the HW setup, it is recommended that you verify in the oscilloscope's device manager that there are no unrecognized USB connections. This is an indication that all drivers have been properly installed and connected.

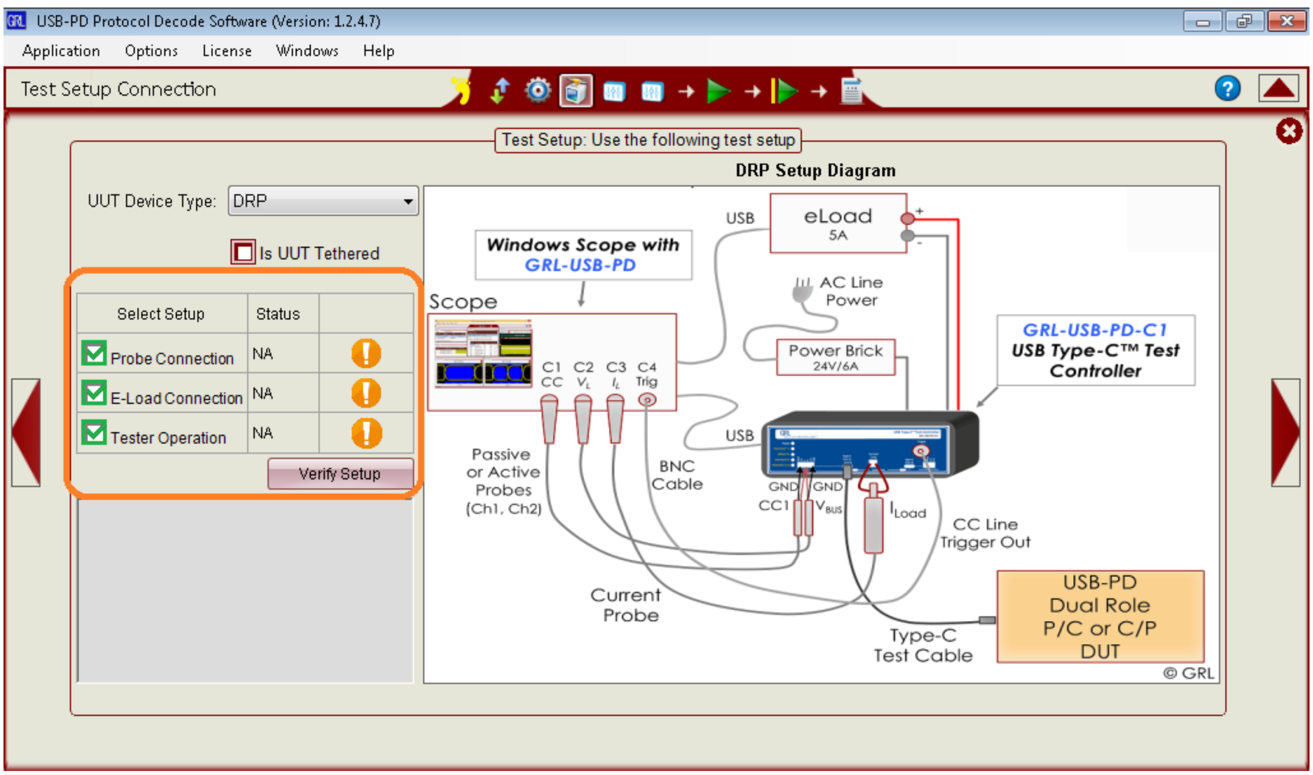
The GRL-USB-PD-C1 controller is now setup and ready for use.

Before running any tests, it is recommended that you verify all connections are communicating using the procedure in this Section. Sometimes communication errors occur between equipment.

If a connection is lost and cannot be restored to its 'green state', close the GRL-USB-PD SW application and re-start it. No work will be lost if the application is closed and re-started.

4.5 Verify Test Setup

To verify the Test Setup navigate to Test Setup Window and click Verify Setup Button as shown below. This feature checks if the Probe, E-Load and Controller Connections are correct. In case of any connection error message showing the reason for failure is shown.



4.6 Cable IR Drop Calibration Procedure

This Procedure is to remove the IR drop in the USB-C Test Cable during Power Load testing. This procedure is required before the compliance testing.

Step 1: Make the setup as shown below for Cable IR drop measurement

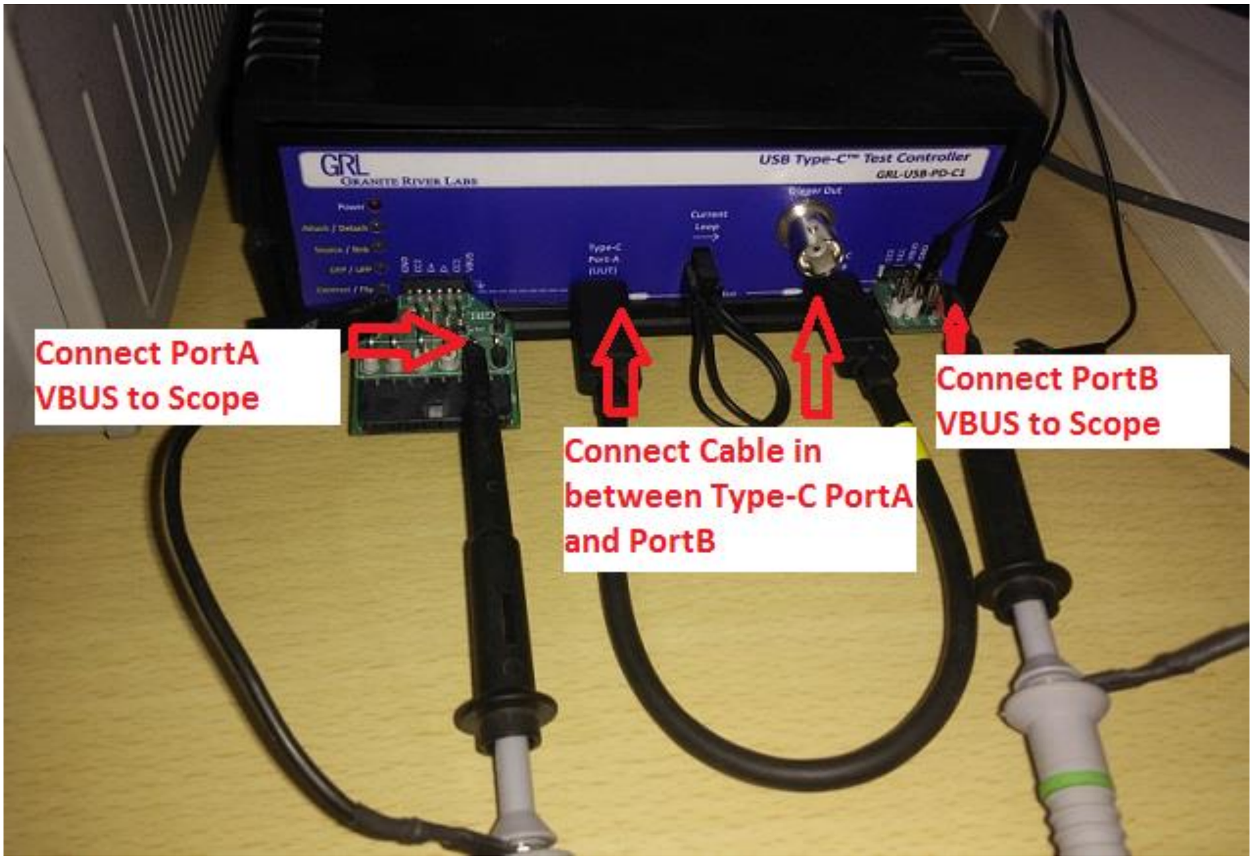
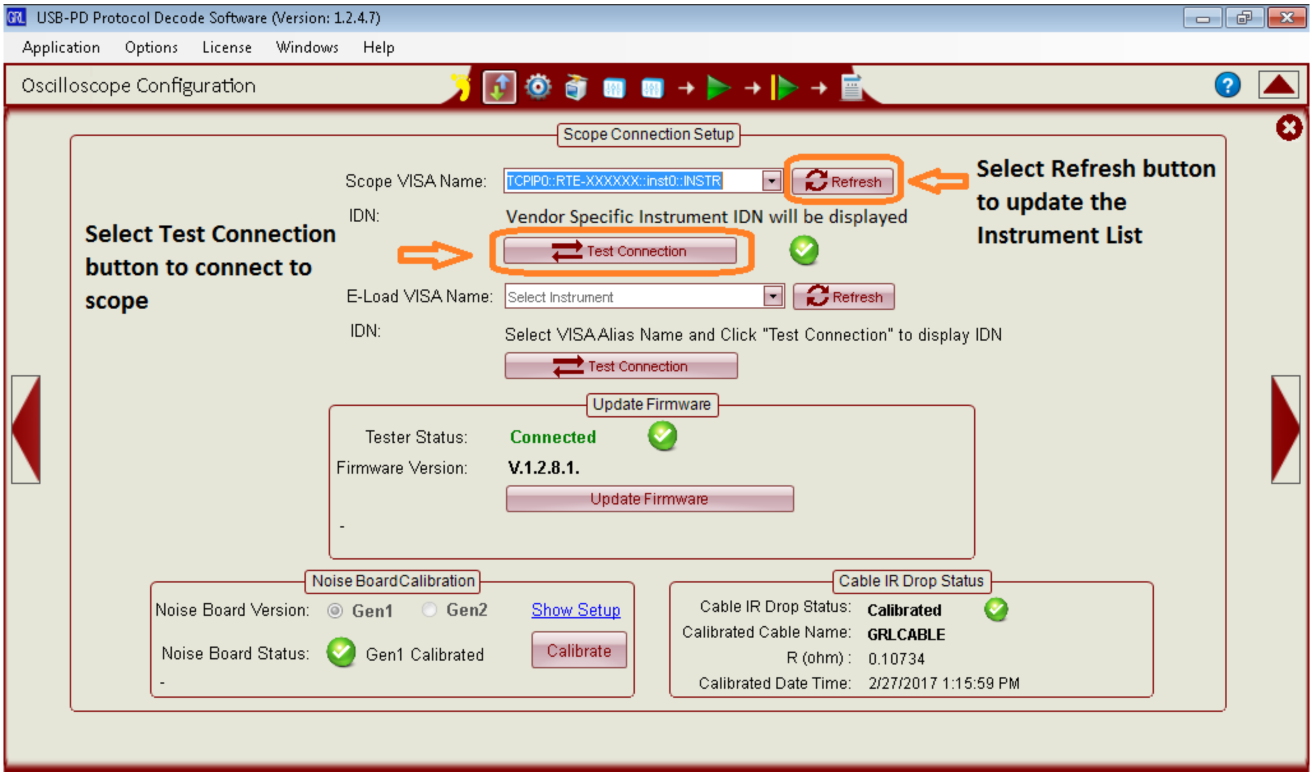
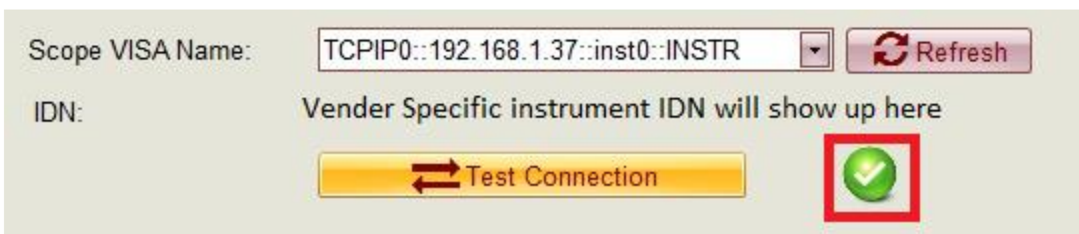


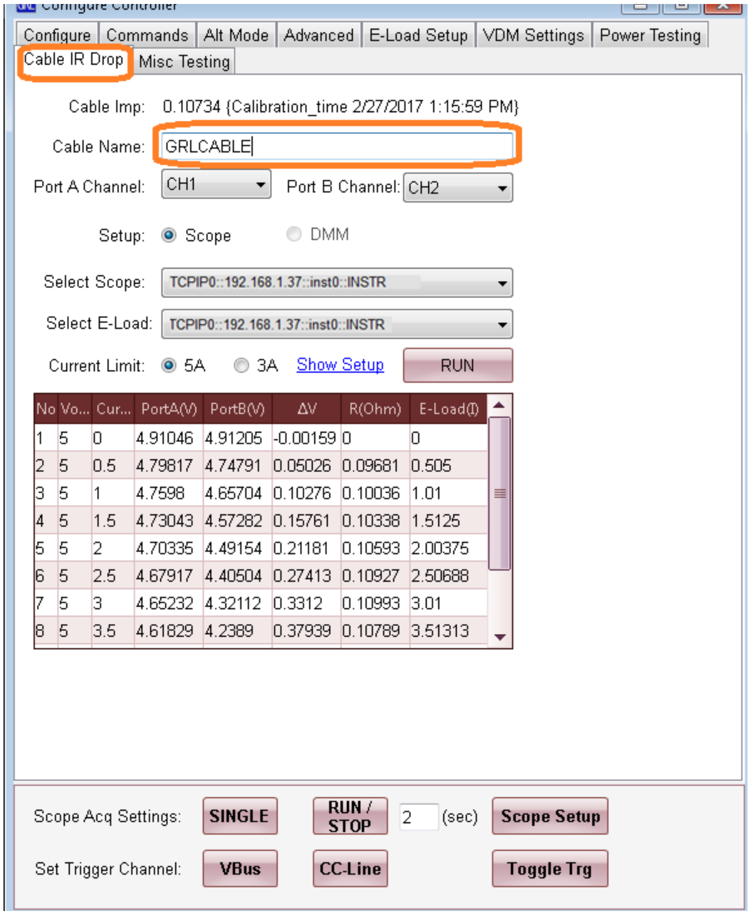
FIGURE 7: TEST CABLE IR DROP CALIBRATION SETUP

Step2: Click Refresh button in Oscilloscope Configuration panel and connect scope as shown in below figure.

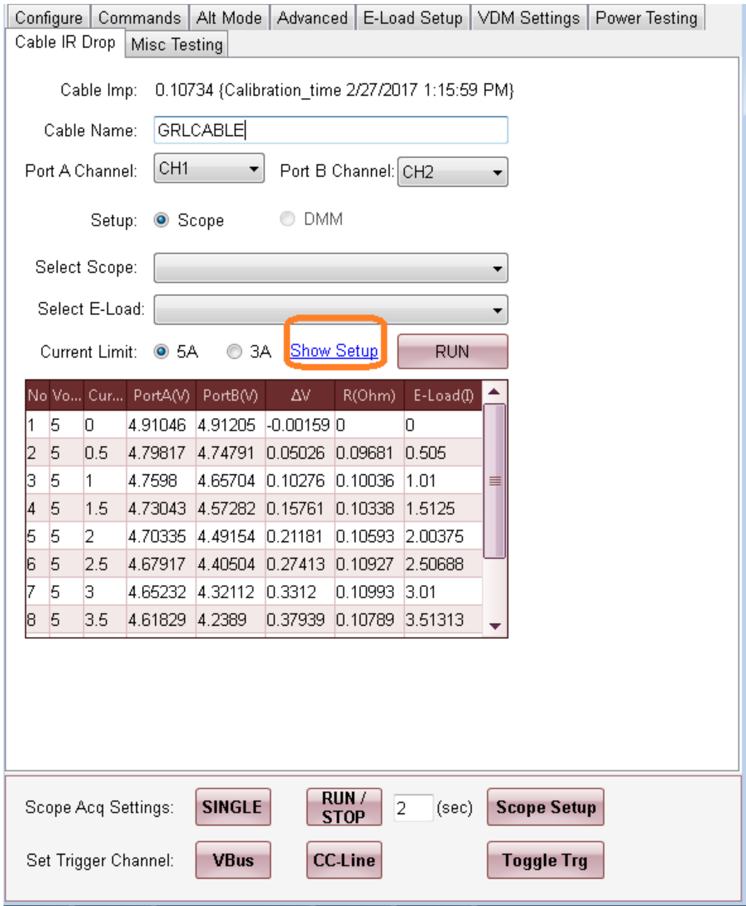




Step 3: Move to Decoder Configuration Tab, Open Config Controller Window and click on Cable IR Drop Tab mention the Cable Name as shown below.

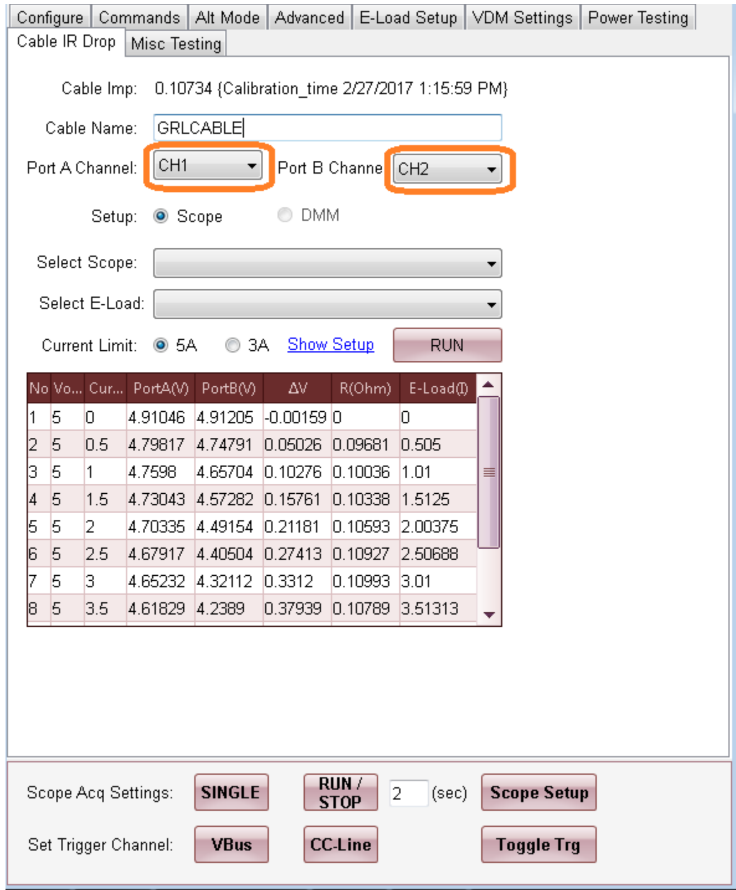


Step 4: To View setup connection click on Show Setup label as shown below, the setup image will pop up.

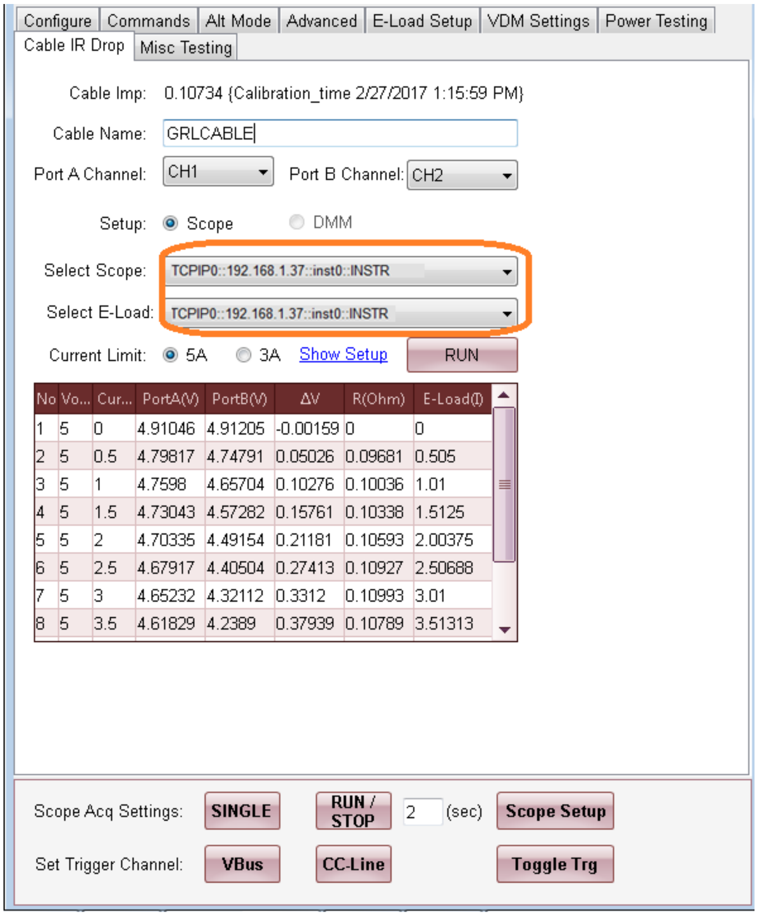


No	Vo...	Cur...	PortA(V)	PortB(V)	ΔV	R(Ohm)	E-Load(I)
1	5	0	4.91046	4.91205	-0.00159	0	0
2	5	0.5	4.79817	4.74791	0.05026	0.09681	0.505
3	5	1	4.7598	4.65704	0.10276	0.10036	1.01
4	5	1.5	4.73043	4.57282	0.15761	0.10338	1.5125
5	5	2	4.70335	4.49154	0.21181	0.10593	2.00375
6	5	2.5	4.67917	4.40504	0.27413	0.10927	2.50688
7	5	3	4.65232	4.32112	0.3312	0.10993	3.01
8	5	3.5	4.61829	4.2389	0.37939	0.10789	3.51313

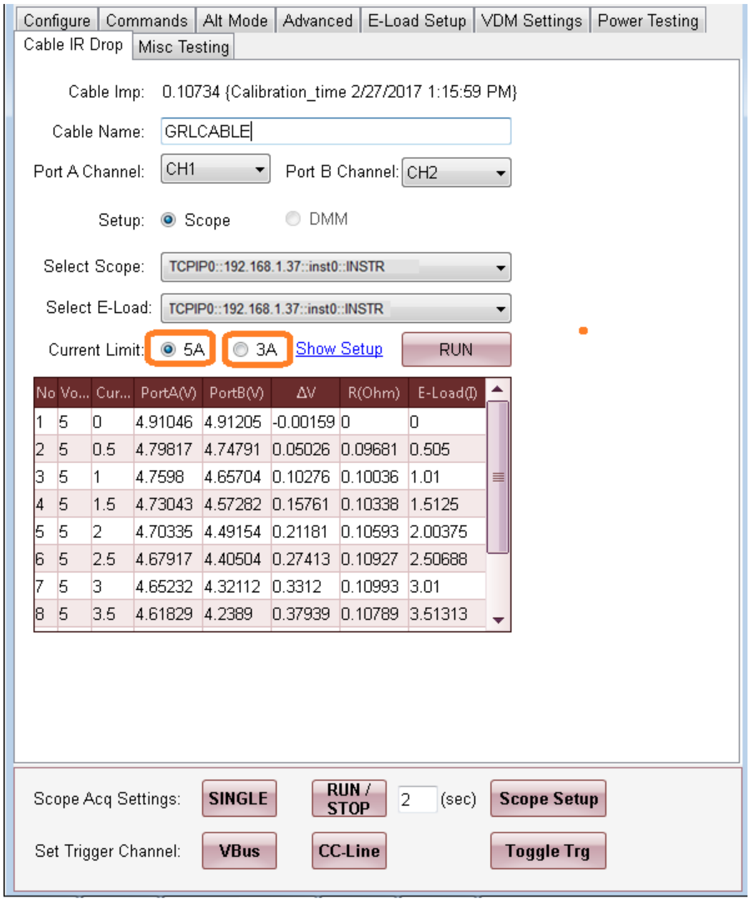
Step 5: Select 'Port –A' in Port A Channel drop down list and select the Scope 'Port-B' in Port B channel drop down list as shown below.



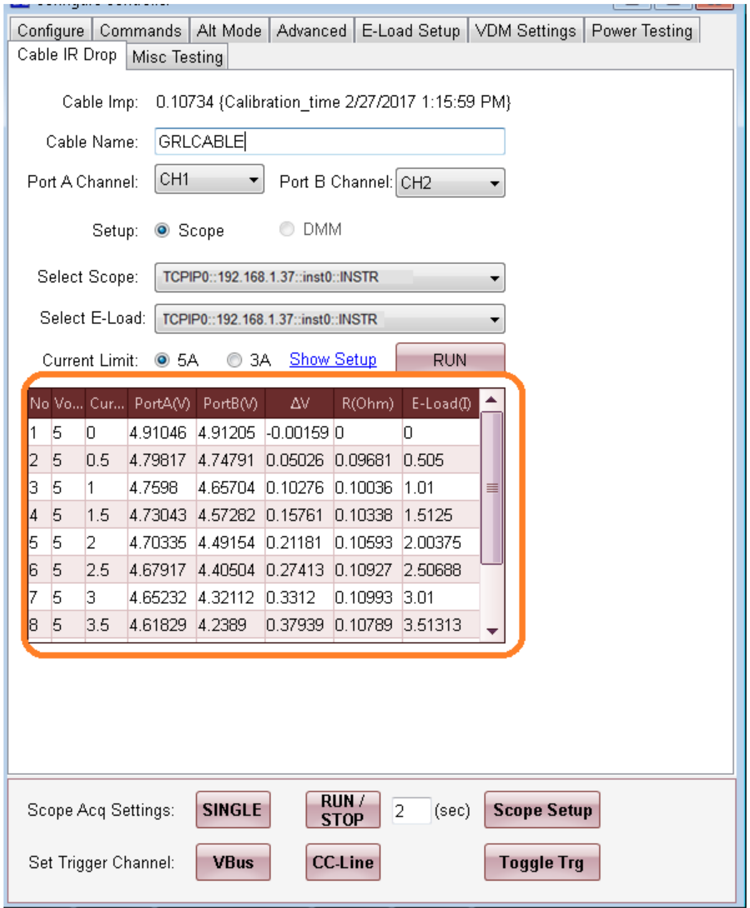
Step 6: Select scope and eLoad VISA identifiers in the respective drop down list as shown below.



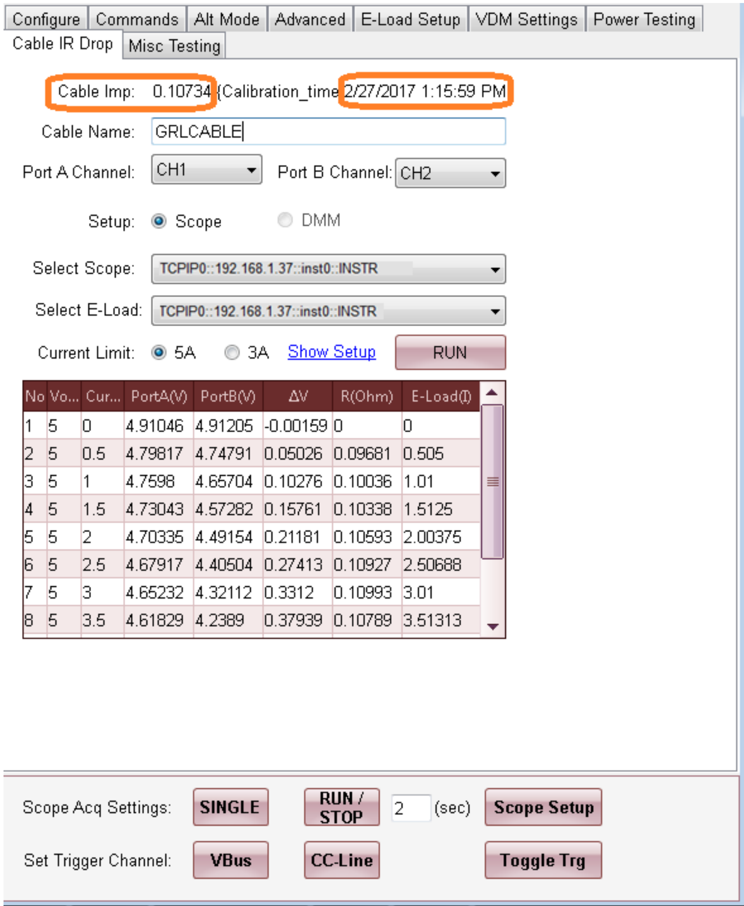
Step 7: Set Current limit as 3A or 5A. 5A is the default value. Based on the current limit set the Grid values will be populated.



Step 8: Click on Run button. The port-A voltage, Port-B voltage, difference in voltage, impedance and measured current values are as displayed.

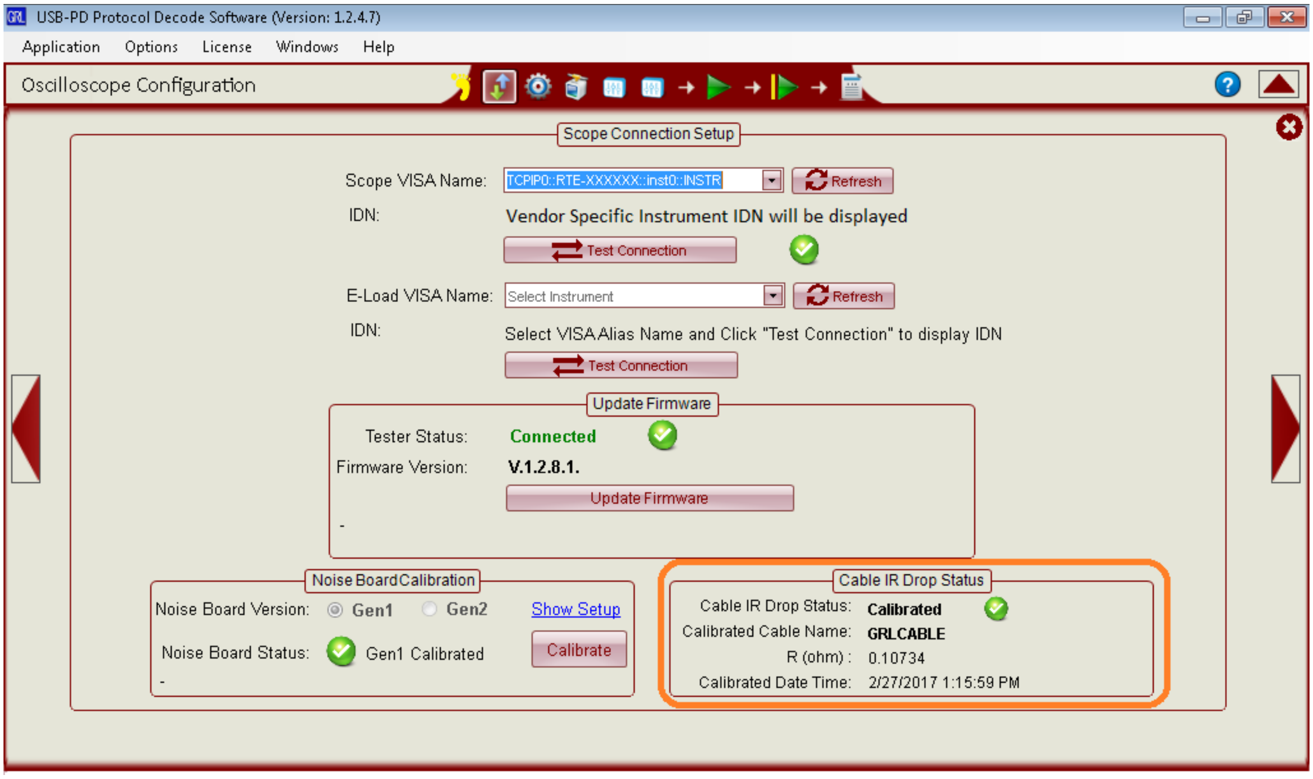


Step 9: After completing the IR calibration check the Cable impedance, time and date of calibration are as shown below



Step 10: In the case when IR drop calibration is already done on the cable, the values in Cable IR Drop Tab will updated based on previous calibrated values including the date and time.

Step 11: Navigate to the Oscilloscope Configuration Window. The IR Drop status would be displayed as shown below.



4.7 Run Test on GRL eMarker Cable to verify update

To verify the update, it is recommended that you run a test on the GRL 'eMarker' cable that is included with the GRL-USB-PD-C1 controller. Follow the procedure in Section 5.10 for the test procedure. Once completed the eMark cable test should show all Pass when testing the GRL eMarker cable.

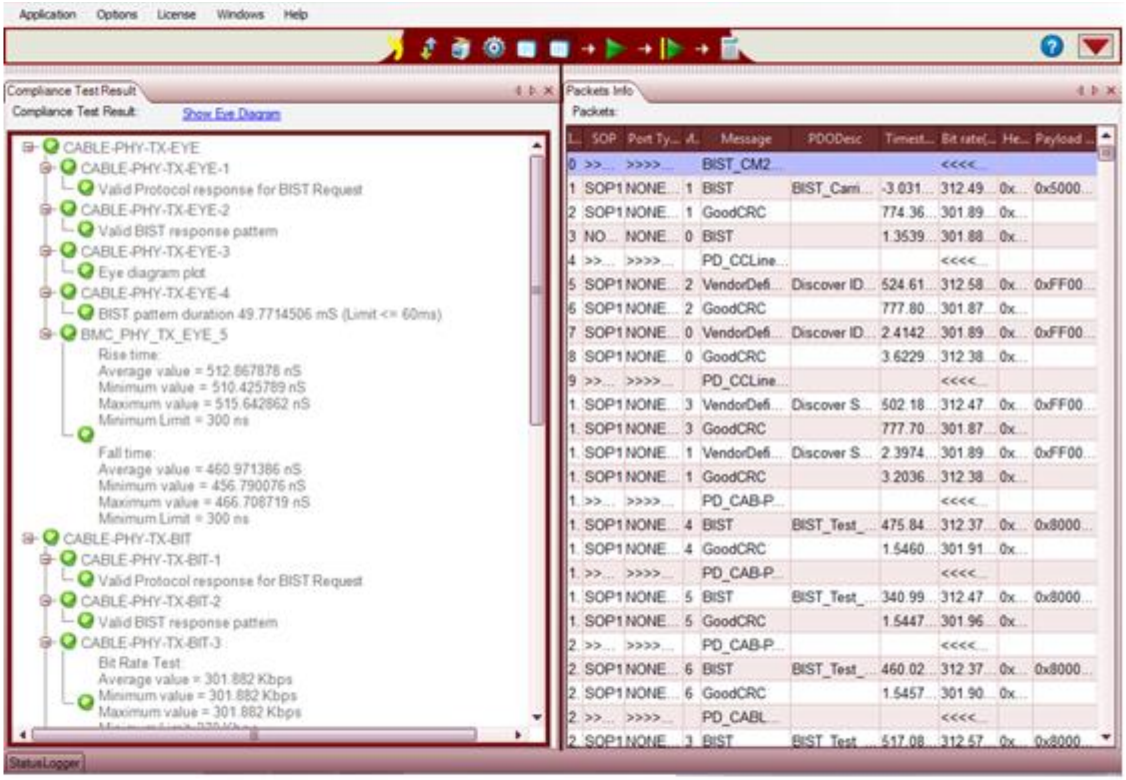


FIGURE 8: EMARK CABLE TEST RESULT ON GRL TEST CABLE

5 USB Power Delivery (USB-PD) Compliance Testing

5.1 Test Plan Overview

The *USB-IF USB Power Delivery Test Plan* is developed by the USB-IF's Power Delivery Working Group.

Chapter 12, MOI Assertion, of the Test Plan provides the listing of required tests for Certification.

Based on the Test Plan, device types include:

- **Electronic Mark 'E-Mark' Cable** – A USB Type-C Cable that has a USB-PD electronic marking chip which indicates through USB-PD messaging its capabilities and vendor information.
- **Dual Role Port** - A Consumer/Provider or Provider/Consumer capable port that is a port capable of operating as either a Source or a Sink.
- **Power Provider** – A device with a PD Port (typically a Host, Hub, or Wall Wart DFP) which is able to source power over the power conductor (e.g. Vbus).
- **Power Consumer** – A device with a PD Port (typically a Device's upstream port) which is able to sink power from the power conductor (e.g. Vbus).
- **Consumer/Provider** - A Power Consumer which can also act as a Power Provider.
- **Provider/Consumer** - A Power Provider which can also act as a Power Consumer.

The following sections include summaries of Primary and Secondary tests that must be run on each USB-PD Device type. Primary tests are required tests. Secondary tests are tests that must be run on specific PD messages when they occur.

The ‘Test Name’ in the following tables can be cross-referenced with the table in Chapter 12 of the test plan, to identify the test assertions covered by each test. The ‘Test Ref #’ is used to organize the tests between the Primary and Secondary test suites, and to provide logical grouping for the test report.

5.2 Electronic Mark 'E-Mark' Cable Tests

5.2.1 Primary eMark Cable Tests

Test Ref #	Test Name	Test Description
	Cable Physical Layer Tests - Transmit	
TDA.1.1.1.1.1	CAB-PHY-TX-EYE	Cable Transmitter Eye Diagram (SOP Prime)
TDA.1.1.1.1.2	CAB-DP-PHY-TX-EYE	Cable Transmitter Eye Diagram (SOP Double Prime)
TDA.1.1.1.2.1	CAB-PHY-TX-BIT	Cable Transmit Bit Rate and Bit Rate Drift (SOP Prime)
TDA.1.1.1.2.2	CAB-DP-PHY-TX-BIT	Cable Transmit Bit Rate & Bit Rate Drift (SOP Double Prime)
	Cable Physical Layer Tests - Receive	
TDA.1.1.2.1.1	CAB-PHY-RX-BUSIDL	Cable Bus Idle Detection (SOP Prime)
TDA.1.1.2.1.2	CAB-DP-PHY-RX-BUSIDL	Cable Bus Idle Detection (SOP Double Prime)
TDA.1.1.2.2.1	CAB-PHY-RX-INT-REJ	Cable Receive Interference Rejection (SOP Prime)
TDA.1.1.2.2.2	CAB-DP-PHY-RX-INT-REJ	Cable Receive Interference Rejection (SOP Double Prime)
	Cable Physical Layer Tests - Miscellaneous	
TDA.1.1.3.1.1	CAB-PHY-TERM	Cable Termination Impedance (SOP Prime)
TDA.1.1.3.1.2	CAB-DP-PHY-TERM	Cable Termination Impedance (SOP Double Prime)
TDA.1.1.3.2.1	CAB-PHY-MSG	Cable PHY Level Message Test (SOP Prime)
TDA.1.1.3.2.2	CAB-DP-PHY-MSG	Cable PHY Level Message Test (SOP Double Prime)
	Cable Protocol-Specific Tests	
TDA.1.2.1	CAB-PROT-DISCOV	Cable ID Checks

5.2.2 Secondary eMark Cable Tests

5.2.2.1 Secondary Message Checks

Test Ref #	Test Name	Test Description
TDB.1.1.1	PHY-MSG-GEN	PHY Level General Message (SOP*)
TDB.2.1.2.1	PROT-MSG-HDR	Message Header Checks – except GoodCRC
TDB.2.1.2.2	PROT-MSG-HDR-GCRC	Message Header Checks – GoodCRC
TDB.2.1.3	PROT-MSG-CTRL	Control Message Checks
TDB.2.1.4.3	PROT-MSG-DATA-VEND	Vendor Defined Message Checks
TDB.2.1.4.4.1.2	PROT-MSG-DATA-VDM-ID-ACK	Discover ID ACK Message Checks
TDB.2.1.4.4.2.2	PROT-MSG-DATA-VDM-SVID-ACK	Discover SVIDs ACK Message Checks
TDB.2.1.4.4.3.2	PROT-MSG-DATA-VDM-MODE-ACK	Discover Modes ACK Message Check
TDB.2.1.4.4.4	PROT-MSG-DATA-VDM-ENTER-MODE	Enter Mode Message Check
TDB.2.1.4.4.5	PROT-MSG-DATA-VDM-EXIT-MODE	Exit Mode Message Check

5.2.2.2 Secondary Procedure Checks

Test Ref #	Test Name	Test Description
TDB.2.2.1.1	PROT-PROC-AMS_1	Atomic Message Sequence
TDB.2.2.2.1	PROT-PROC-GOODCRC-TSTR	GoodCRC sent by Tester
TDB.2.2.2.2	PROT-PROC-GOODCRC-DUT	GoodCRC sent by Unit Under Test (DUT)
TDB.2.2.12.1	PROT-PROC-SR-TSTR	Tester Originated Soft Reset
TDB.2.2.12.2	PROT-PROC-SR-DUT	DUT Originated Soft Reset
TDB.2.2.13.1	PROT-PROC-HR-TSTR	Tester Originated Hard Reset
TDB.2.2.13.2	PROT-PROC-HR-DUT	DUT Originated Hard Reset
TDB.2.2.14	PROT-PROC-BIST-TSTR	Tester Originated BIST

5.3 Dual-Role Port (DRP) Tests

5.3.1 Primary DRP Tests

Note that test BMC-PROT-BIST-NOT-5V-SRC is required only for devices which support greater than 5 volts.

Test Ref #	Test Name	Test Description
	Power Rules Tests	
PDSPEC10.10.2	SOURCE-POWER-RULES	Provider Power Rules Test
PDSPEC10.10.3	SINK-POWER-RULES	Consumer Power Rules Test
	BMC Physical Layer Tests - Transmit	
TDA.2.1.1.1	BMC-PHY-TX-EYE	BMC Transmitter Eye Diagram
TDA.2.1.1.2	BMC-PHY-TX-BIT	BMC Transmit Bit Rate and Bit Drift Rate
	BMC Physical Layer Tests - Receive	
TDA.2.1.2.1	BMC-PHY-RX-BUSIDL	BMC Bus Idle Detection
TDA.2.1.2.2	CAB-DP-PHY-RX-BUSIDL	BMC Receive Interference Rejection
	BMC Physical Layer Tests - Miscellaneous	
TDA.2.1.3.1	BMC-PHY-TERM	BMC Termination Impedance
TDA.2.1.3.2	BMC-PHY-MSG	BMC PHY Level Message
	Protocol-Specific Message Check Tests	
TDA.2.2.1	BMC-PROT-SEQ-GETCAPS	Get_Source_Cap and Get_Sink_Cap
TDA.2.2.2.1	BMC-PROT-SEQ-CHKCAP-P-PC	Check Capabilities (3A Marked)
TDA.2.2.2.2	BMC-PROT-SEQ-CHKCAP-NOMRK-P-PC	Check Capabilities (Unmarked)
TDA.2.2.2.3	BMC-PROT-SEQ-CHKCAP-CP-ACC	Check Capabilities (3A Marked) – After PR Swap
TDA.2.2.2.4	BMC-PROT-SEQ-CHKCAP-NOMRK-CP-ACC	Check Capabilities (Unmarked) – After PR Swap
TDA.2.2.3	BMC-PROT-SEQ-DRSWAP	Dual Role Swap
TDA.2.2.4	BMC-PROT-SEQ-VCSWAP	Vconn Swap
TDA.2.2.5	BMC-PROT-DISCOV	ID Check
TDA.2.2.6	BMC-SEQ-SWAP-REJ	Reject Swap – Consumer / Provider
TDA.2.2.7	BMC-PROT-BIST-NOT-5V-SRC	BIST Functionality at Above 5V
TDA.2.2.8	BMC-PROT-REV-NUM	Revision Number
TDA.2.2.9	BMC-PROT-GSC-REC	Get_Source_Cap Received Test
	Power Source/Sink Tests	
TDA.2.3.1.1	BMC-POW-SRC-LOAD-P-PC	Source Dynamic Load – Provider or Provider/Consumer
TDA.2.3.1.2	BMC-POW-SRC-LOAD-CP-ACC	Source Dynamic Load – Consumer/Provider Accepting Swap
TDA.2.3.2.1	BMC-POW-SRC-TRANS-P-PC	PDO Transition – Source, Provider or Provider/Consumer
TDA.2.3.2.2	BMC-POW-SRC-TRANS-CP-ACC	PDO Transition – Source, Consumer/Provider Accepting Swap
TDA.2.3.3.1	BMC-POW-SNK-TRANS-C-CP	PDO Transition – Current Draw and Suspend – Sink, Consumer
TDA.2.3.3.2	BMC-POW-SNK-TRANS-PC	PDO Transition – Current Draw and Suspend – Sink, Provider/Consumer

5.3.2 Secondary DRP Tests

5.3.2.1 Secondary Message Checks

Test Ref #	Test Name	Test Description
TDB.1.1.1	PHY-MSG-GEN	PHY Level General Message (SOP*)
TDB.2.1.2.1	PROT-MSG-HDR	Message Header Checks – except GoodCRC
TDB.2.1.2.2	PROT-MSG-HDR-GCRC	Message Header Checks – GoodCRC
TDB.2.1.3	PROT-MSG-CTRL	Control Message Checks
TDB.2.1.3.1	PROT-MSG-CTRL-PING	Ping Checks
TDB.2.1.4.1.1	PROT-MSG-DATA-SRC-CAP	Source Capability Message Checks
TDB.2.1.4.1.2	PROT-MSG-DATA-SNK-CAP	Sink Capability Message Checks
TDB.2.1.4.2	PROT-MSG-DATA-REQ	Request Message Checks
TDB.2.1.4.3	PROT-MSG-DATA-VEND	Vendor Defined Message Checks
TDB.2.1.4.4.1.1	PROT-MSG-DATA-VDM-ID-INIT	Discover ID Initiator Message Checks
TDB.2.1.4.4.1.2	PROT-MSG-DATA-VDM-ID-ACK	Discover ID ACK Message Checks
TDB.2.1.4.4.2.1	PROT-MSG-DATA-VDM-SVID-INIT	Discover SVIDs Initiator Message Checks
TDB.2.1.4.4.2.2	PROT-MSG-DATA-VDM-SVID-ACK	Discover SVIDs ACK Message Checks
TDB.2.1.4.4.3.1	PROT-MSG-DATA-VDM-MODE-INIT	Discover Modes Initiator Message Check
TDB.2.1.4.4.3.2	PROT-MSG-DATA-VDM-MODE-ACK	Discover Modes ACK Message Check
TDB.2.1.4.4.4	PROT-MSG-DATA-VDM-ENTER-MODE	Enter Mode Message Check
TDB.2.1.4.4.5	PROT-MSG-DATA-VDM-EXIT-MODE	Exit Mode Message Check
TDB.2.1.4.4.6	PROT-MSG-DATA-VDM-ATT	Attention Message Check

5.3.2.2 Secondary Procedure Checks

Test Ref #	Test Name	Test Description
TDB.2.2.1.1	PROT-PROC-AMS_1	Atomic Message Sequence
TDB.2.2.2.1	PROT-PROC-GOODCRC-TSTR	GoodCRC sent by Tester
TDB.2.2.2.2	PROT-PROC-GOODCRC-DUT	GoodCRC sent by Unit Under Test (DUT)
TDB.2.2.3.1.1	PROT-PROC-SWAP-TSTR-SNK	Tester (Sink) Originated Swap
TDB.2.2.3.1.2	PROT-PROC-SWAP-TSTR-SRC	Tester (Source) Originated Swap
TDB.2.2.3.2.1	PROT-PROC-SWAP-DUT-SNK	DUT (Sink) Originated Swap
TDB.2.2.3.2.2	PROT-PROC-SWAP-DUT-SRC	DUT (Source) Originated Swap
TDB.2.2.4	PROT-PROC-PSSOURCEOFFTIMER	Test PSSourceOffTimer when not Swapped
TDB.2.2.5	PROT-PROC-PSSOURCEONTIMER	Test PSSourceOnTimer when not Swapped
TDB.2.2.6	PROT-PROC-PING	Send Ping from Tester
TDB.2.2.7.1	PROT-PROC-REQ-TSTR	Tester Originated Request
TDB.2.2.7.2	PROT-PROC-REQ-UUR	DUT Originated Request
TDB.2.2.8.1	PROT-PROC-SRCCAPS-TSTR	Tester Originated Source Capabilities
TDB.2.2.8.2	PROT-PROC-SRCCAPS-DUT	DUT Originated Source Capabilities
TDB.2.2.9.1	PROT-PROC-GETSRCCAPS-TSTR	Tester Originated Get_Source_Cap
TDB.2.2.9.2	PROT-PROC-GETSRCCAPS-DUT	DUT Originated Get_Source_Cap
TDB.2.2.10.1	PROT-PROC-GETSNKCAPS-TSTR	Tester Originated Get_Sink_Cap
TDB.2.2.10.2	PROT-PROC-GETSNKCAPS-DUT	DUT Originated Get_Sink_Cap
TDB.2.2.11.1	PROT-PROC-GOTOMIN-TSTR	Tester Originated GoToMin
TDB.2.2.11.2	PROT-PROC-GOTOMIN-DUT	DUT Originated GoToMin
TDB.2.2.12.1	PROT-PROC-SR-TSTR	Tester Originated Soft Reset
TDB.2.2.12.2	PROT-PROC-SR-DUT	DUT Originated Soft Reset
TDB.2.2.13.1	PROT-PROC-HR-TSTR	Tester Originated Hard Reset
TDB.2.2.13.2	PROT-PROC-HR-DUT	DUT Originated Hard Reset
TDB.2.2.14	PROT-PROC-BIST-TSTR	Tester Originated BIST

5.4 Provider-Only Tests

5.4.1 Primary Provider-Only Tests

Note that test BMC-PROT-BIST-NOT-5V-SRC is required only for devices which support greater than 5 volts.

Test Ref #	Test Name	Test Description
	Power Rules Tests	
PDSPEC10.10.2	SOURCE-POWER-RULES	Provider Power Rules Test
	BMC Physical Layer Tests - Transmit	
TDA.2.1.1.1	BMC-PHY-TX-EYE	BMC Transmitter Eye Diagram
TDA.2.1.1.2	BMC-PHY-TX-BIT	BMC Transmit Bit Rate and Bit Drift Rate
	BMC Physical Layer Tests - Receive	
TDA.2.1.2.1	BMC-PHY-RX-BUSIDL	BMC Bus Idle Detection
TDA.2.1.2.2	CAB-DP-PHY-RX-BUSIDL	BMC Receive Interference Rejection
	BMC Physical Layer Tests - Miscellaneous	
TDA.2.1.3.1	BMC-PHY-TERM	BMC Termination Impedance
TDA.2.1.3.2	BMC-PHY-MSG	BMC PHY Level Message
	Protocol-Specific Message Check Tests	
TDA.2.2.1	BMC-PROT-SEQ-GETCAPS	Get_Source_Cap and Get_Sink_Cap
TDA.2.2.2.1	BMC-PROT-SEQ-CHKCAP-P-PC	Check Capabilities (3A Marked)
TDA.2.2.2.2	BMC-PROT-SEQ-CHKCAP-NOMRK-P-PC	Check Capabilities (Unmarked)
TDA.2.2.3	BMC-PROT-SEQ-DRSWAP	Dual Role Swap
TDA.2.2.6	BMC-SEQ-SWAP-REJ	Reject Swap – Consumer / Provider
TDA.2.2.7	BMC-PROT-BIST-NOT-5V-SRC	BIST Functionality at Above 5V
TDA.2.2.8	BMC-PROT-REV-NUM	Revision Number
	Power Source/Sink Tests	
TDA.2.3.1.1	BMC-POW-SRC-LOAD-P-PC	Source Dynamic Load – Provider or Provider/Consumer
TDA.2.3.2.1	BMC-POW-SRC-TRANS-P-PC	PDO Transition – Source, Provider or Provider/Consumer

5.4.2 Secondary Provider-Only Tests

5.4.2.1 Secondary Message Checks

Test Ref #	Test Name	Test Description
TDB.1.1.1	PHY-MSG-GEN	PHY Level General Message (SOP*)
TDB.2.1.2.1	PROT-MSG-HDR	Message Header Checks – except GoodCRC
TDB.2.1.2.2	PROT-MSG-HDR-GCRC	Message Header Checks – GoodCRC
TDB.2.1.3	PROT-MSG-CTRL	Control Message Checks
TDB.2.1.3.1	PROT-MSG-CTRL-PING	Ping Checks
TDB.2.1.4.1.1	PROT-MSG-DATA-SRC-CAP	Source Capability Message Checks
TDB.2.1.4.3	PROT-MSG-DATA-VEND	Vendor Defined Message Checks
TDB.2.1.4.4.1.1	PROT-MSG-DATA-VDM-ID-INIT	Discover ID Initiator Message Checks
TDB.2.1.4.4.1.2	PROT-MSG-DATA-VDM-ID-ACK	Discover ID ACK Message Checks
TDB.2.1.4.4.2.1	PROT-MSG-DATA-VDM-SVID-INIT	Discover SVIDs Initiator Message Checks
TDB.2.1.4.4.2.2	PROT-MSG-DATA-VDM-SVID-ACK	Discover SVIDs ACK Message Checks
TDB.2.1.4.4.3.1	PROT-MSG-DATA-VDM-MODE-INIT	Discover Modes Initiator Message Check
TDB.2.1.4.4.3.2	PROT-MSG-DATA-VDM-MODE-ACK	Discover Modes ACK Message Check
TDB.2.1.4.4.4	PROT-MSG-DATA-VDM-ENTER-MODE	Enter Mode Message Check
TDB.2.1.4.4.5	PROT-MSG-DATA-VDM-EXIT-MODE	Exit Mode Message Check
TDB.2.1.4.4.6	PROT-MSG-DATA-VDM-ATT	Attention Message Check

5.4.2.2 Secondary Procedure Checks

Test Ref #	Test Name	Test Description
TDB.2.2.1.1	PROT-PROC-AMS_1	Atomic Message Sequence
TDB.2.2.2.1	PROT-PROC-GOODCRC-TSTR	GoodCRC sent by Tester
TDB.2.2.2.2	PROT-PROC-GOODCRC-DUT	GoodCRC sent by Unit Under Test (DUT)
TDB.2.2.6	PROT-PROC-PING	Send Ping from Tester
TDB.2.2.7.1	PROT-PROC-REQ-TSTR	Tester Originated Request
TDB.2.2.8.2	PROT-PROC-SRCCAPS-DUT	DUT Originated Source Capabilities
TDB.2.2.9.1	PROT-PROC-GETSRCCAPS-TSTR	Tester Originated Get_Source_Cap
TDB.2.2.9.2	PROT-PROC-GETSRCCAPS-DUT	DUT Originated Get_Source_Cap
TDB.2.2.10.1	PROT-PROC-GETSNKCAPS-TSTR	Tester Originated Get_Sink_Cap
TDB.2.2.10.2	PROT-PROC-GETSNKCAPS-DUT	DUT Originated Get_Sink_Cap
TDB.2.2.11.2	PROT-PROC-GOTOMIN-DUT	DUT Originated GoToMin
TDB.2.2.12.1	PROT-PROC-SR-TSTR	Tester Originated Soft Reset
TDB.2.2.12.2	PROT-PROC-SR-DUT	DUT Originated Soft Reset
TDB.2.2.13.1	PROT-PROC-HR-TSTR	Tester Originated Hard Reset
TDB.2.2.13.2	PROT-PROC-HR-DUT	DUT Originated Hard Reset
TDB.2.2.14	PROT-PROC-BIST-TSTR	Tester Originated BIST

5.5 Consumer-Only Tests

5.5.1 Primary Consumer-Only Tests

Test Ref #	Test Name	Test Description
	Power Rules Tests	
PDSPEC10.10.3	SINK-POWER-RULES	Consumer Power Rules Test
	BMC Physical Layer Tests - Transmit	
TDA.2.1.1.1	BMC-PHY-TX-EYE	BMC Transmitter Eye Diagram
TDA.2.1.1.2	BMC-PHY-TX-BIT	BMC Transmit Bit Rate and Bit Drift Rate
	BMC Physical Layer Tests - Receive	
TDA.2.1.2.1	BMC-PHY-RX-BUSIDL	BMC Bus Idle Detection
TDA.2.1.2.2	CAB-DP-PHY-RX-BUSIDL	BMC Receive Interference Rejection
	BMC Physical Layer Tests - Miscellaneous	
TDA.2.1.3.1	BMC-PHY-TERM	BMC Termination Impedance
TDA.2.1.3.2	BMC-PHY-MSG	BMC PHY Level Message
	Protocol-Specific Message Check Tests	
TDA.2.2.1	BMC-PROT-SEQ-GETCAPS	Get_Source_Cap and Get_Sink_Cap
TDA.2.2.3	BMC-PROT-SEQ-DRSWAP	Dual Role Swap
TDA.2.2.4	BMC-PROT-SEQ-VCSWAP	Vconn Swap
TDA.2.2.5	BMC-PROT-DISCOV	ID Check
TDA.2.2.8	BMC-PROT-REV-NUM	Revision Number
	Power Source/Sink Tests	
TDA.2.3.3.1	BMC-POW-SNK-TRANS-C-CP	PDO Transition – Current Draw and Suspend – Sink, Consumer

5.5.2 Secondary Consumer-Only Tests

5.5.2.1 Secondary Message Checks

Test Ref #	Test Name	Test Description
TDB.1.1.1	PHY-MSG-GEN	PHY Level General Message (SOP*)
TDB.2.1.2.1	PROT-MSG-HDR	Message Header Checks – except GoodCRC
TDB.2.1.2.2	PROT-MSG-HDR-GCRC	Message Header Checks – GoodCRC
TDB.2.1.3	PROT-MSG-CTRL	Control Message Checks
TDB.2.1.4.1.2	PROT-MSG-DATA-SNK-CAP	Sink Capability Message Checks
TDB.2.1.4.2	PROT-MSG-DATA-REQ	Request Message Checks
TDB.2.1.4.3	PROT-MSG-DATA-VEND	Vendor Defined Message Checks
TDB.2.1.4.4.1.1	PROT-MSG-DATA-VDM-ID-INIT	Discover ID Initiator Message Checks
TDB.2.1.4.4.1.2	PROT-MSG-DATA-VDM-ID-ACK	Discover ID ACK Message Checks
TDB.2.1.4.4.2.1	PROT-MSG-DATA-VDM-SVID-INIT	Discover SVIDs Initiator Message Checks
TDB.2.1.4.4.2.2	PROT-MSG-DATA-VDM-SVID-ACK	Discover SVIDs ACK Message Checks
TDB.2.1.4.4.3.1	PROT-MSG-DATA-VDM-MODE-INIT	Discover Modes Initiator Message Check
TDB.2.1.4.4.3.2	PROT-MSG-DATA-VDM-MODE-ACK	Discover Modes ACK Message Check
TDB.2.1.4.4.4	PROT-MSG-DATA-VDM-ENTER-MODE	Enter Mode Message Check
TDB.2.1.4.4.5	PROT-MSG-DATA-VDM-EXIT-MODE	Exit Mode Message Check
TDB.2.1.4.4.6	PROT-MSG-DATA-VDM-ATT	Attention Message Check

5.5.2.2 Secondary Procedure Checks

Test Ref #	Test Name	Test Description
TDB.2.2.1.1	PROT-PROC-AMS_1	Atomic Message Sequence
TDB.2.2.2.1	PROT-PROC-GOODCRC-TSTR	GoodCRC sent by Tester
TDB.2.2.2.2	PROT-PROC-GOODCRC-DUT	GoodCRC sent by Unit Under Test (DUT)
TDB.2.2.6	PROT-PROC-PING	Send Ping from Tester
TDB.2.2.7.2	PROT-PROC-REQ-UUR	DUT Originated Request
TDB.2.2.8.1	PROT-PROC-SRCCAPS-TSTR	Tester Originated Source Capabilities
TDB.2.2.9.1	PROT-PROC-GETSRCCAPS-TSTR	Tester Originated Get_Source_Cap
TDB.2.2.9.2	PROT-PROC-GETSRCCAPS-DUT	DUT Originated Get_Source_Cap
TDB.2.2.10.1	PROT-PROC-GETSNKCAPS-TSTR	Tester Originated Get_Sink_Cap
TDB.2.2.10.2	PROT-PROC-GETSNKCAPS-DUT	DUT Originated Get_Sink_Cap
TDB.2.2.11.1	PROT-PROC-GOTOMIN-TSTR	Tester Originated GoToMin
TDB.2.2.12.1	PROT-PROC-SR-TSTR	Tester Originated Soft Reset
TDB.2.2.12.2	PROT-PROC-SR-DUT	DUT Originated Soft Reset
TDB.2.2.13.1	PROT-PROC-HR-TSTR	Tester Originated Hard Reset
TDB.2.2.13.2	PROT-PROC-HR-DUT	DUT Originated Hard Reset
TDB.2.2.14	PROT-PROC-BIST-TSTR	Tester Originated BIST

5.6 Dual-Role Device – Consumer/Provider Tests

5.6.1 Primary Dual-Role Device – Consumer/Provider Tests

Test Ref #	Test Name	Test Description
	Power Rule Tests	
PDSPEC10.10.2	SOURCE-POWER-RULES	Provider Power Rules Test
PDSPEC10.10.3	SINK-POWER-RULES	Consumer Power Rules Test
	BMC Physical Layer Tests - Transmit	
TDA.2.1.1.1	BMC-PHY-TX-EYE	BMC Transmitter Eye Diagram
TDA.2.1.1.2	BMC-PHY-TX-BIT	BMC Transmit Bit Rate and Bit Drift Rate
	BMC Physical Layer Tests - Receive	
TDA.2.1.2.1	BMC-PHY-RX-BUSIDL	BMC Bus Idle Detection
TDA.2.1.2.2	CAB-DP-PHY-RX-BUSIDL	BMC Receive Interference Rejection
	BMC Physical Layer Tests - Miscellaneous	
TDA.2.1.3.1	BMC-PHY-TERM	BMC Termination Impedance
TDA.2.1.3.2	BMC-PHY-MSG	BMC PHY Level Message
	Protocol-Specific Message Check Tests	
TDA.2.2.1	BMC-PROT-SEQ-GETCAPS	Get_Source_Cap and Get_Sink_Cap
TDA.2.2.2.3	BMC-PROT-SEQ-CHKCAP-CP-ACC	Check Capabilities (3A Marked) – After PR Swap
TDA.2.2.2.4	BMC-PROT-SEQ-CHKCAP-NOMRK-CP-ACC	Check Capabilities (Unmarked) – After PR Swap
TDA.2.2.3	BMC-PROT-SEQ-DRSWAP	Dual Role Swap
TDA.2.2.4	BMC-PROT-SEQ-VCSWAP	Vconn Swap
TDA.2.2.5	BMC-PROT-DISCOV	ID Check
TDA.2.2.8	BMC-PROT-REV-NUM	Revision Number
	Power Source/Sink Tests	
TDA.2.3.1.2	BMC-POW-SRC-LOAD-CP-ACC	Source Dynamic Load – Consumer/Provider Accepting Swap
TDA.2.3.2.2	BMC-POW-SRC-TRANS-CP-ACC	PDO Transition – Source, Consumer/Provider Accepting Swap
TDA.2.3.3.1	BMC-POW-SNK-TRANS-C-CP	PDO Transition – Current Draw and Suspend – Sink, Consumer

5.6.2 Secondary Dual-Role Device – Consumer/Provider Tests

5.6.2.1 Secondary Message Checks

Test Ref #	Test Name	Test Description
TDB.1.1.1	PHY-MSG-GEN	PHY Level General Message (SOP*)
TDB.2.1.2.1	PROT-MSG-HDR	Message Header Checks – except GoodCRC
TDB.2.1.2.2	PROT-MSG-HDR-GCRC	Message Header Checks – GoodCRC
TDB.2.1.3	PROT-MSG-CTRL	Control Message Checks
TDB.2.1.3.1	PROT-MSG-CTRL-PING	Ping Checks
TDB.2.1.4.1.1	PROT-MSG-DATA-SRC-CAP	Source Capability Message Checks
TDB.2.1.4.1.2	PROT-MSG-DATA-SNK-CAP	Sink Capability Message Checks
TDB.2.1.4.2	PROT-MSG-DATA-REQ	Request Message Checks
TDB.2.1.4.3	PROT-MSG-DATA-VEND	Vendor Defined Message Checks
TDB.2.1.4.4.1.1	PROT-MSG-DATA-VDM-ID-INIT	Discover ID Initiator Message Checks
TDB.2.1.4.4.1.2	PROT-MSG-DATA-VDM-ID-ACK	Discover ID ACK Message Checks
TDB.2.1.4.4.2.1	PROT-MSG-DATA-VDM-SVID-INIT	Discover SVIDs Initiator Message Checks
TDB.2.1.4.4.2.2	PROT-MSG-DATA-VDM-SVID-ACK	Discover SVIDs ACK Message Checks
TDB.2.1.4.4.3.1	PROT-MSG-DATA-VDM-MODE-INIT	Discover Modes Initiator Message Check
TDB.2.1.4.4.3.2	PROT-MSG-DATA-VDM-MODE-ACK	Discover Modes ACK Message Check
TDB.2.1.4.4.4	PROT-MSG-DATA-VDM-ENTER-MODE	Enter Mode Message Check
TDB.2.1.4.4.5	PROT-MSG-DATA-VDM-EXIT-MODE	Exit Mode Message Check
TDB.2.1.4.4.6	PROT-MSG-DATA-VDM-ATT	Attention Message Check

5.6.2.2 Secondary Procedure Checks

Test Ref #	Test Name	Test Description
TDB.2.2.1.1	PROT-PROC-AMS_1	Atomic Message Sequence
TDB.2.2.2.1	PROT-PROC-GOODCRC-TSTR	GoodCRC sent by Tester
TDB.2.2.2.2	PROT-PROC-GOODCRC-DUT	GoodCRC sent by Unit Under Test (DUT)
TDB.2.2.3.1.1	PROT-PROC-SWAP-TSTR-SNK	Tester (Sink) Originated Swap
TDB.2.2.3.1.2	PROT-PROC-SWAP-TSTR-SRC	Tester (Source) Originated Swap
TDB.2.2.3.2.1	PROT-PROC-SWAP-DUT-SNK	DUT (Sink) Originated Swap
TDB.2.2.3.2.2	PROT-PROC-SWAP-DUT-SRC	DUT (Source) Originated Swap
TDB.2.2.4	PROT-PROC-PSSOURCEOFFTIMER	Test PSSourceOffTimer when not Swapped
TDB.2.2.5	PROT-PROC-PSSOURCEONTIMER	Test PSSourceOnTimer when not Swapped
TDB.2.2.6	PROT-PROC-PING	Send Ping from Tester
TDB.2.2.7.1	PROT-PROC-REQ-TSTR	Tester Originated Request
TDB.2.2.7.2	PROT-PROC-REQ-UUR	DUT Originated Request
TDB.2.2.8.1	PROT-PROC-SRCCAPS-TSTR	Tester Originated Source Capabilities
TDB.2.2.8.2	PROT-PROC-SRCCAPS-DUT	DUT Originated Source Capabilities
TDB.2.2.9.1	PROT-PROC-GETSRCCAPS-TSTR	Tester Originated Get_Source_Cap
TDB.2.2.9.2	PROT-PROC-GETSRCCAPS-DUT	DUT Originated Get_Source_Cap
TDB.2.2.10.1	PROT-PROC-GETSNKCAPS-TSTR	Tester Originated Get_Sink_Cap
TDB.2.2.10.2	PROT-PROC-GETSNKCAPS-DUT	DUT Originated Get_Sink_Cap
TDB.2.2.11.1	PROT-PROC-GOTOMIN-TSTR	Tester Originated GoToMin
TDB.2.2.11.2	PROT-PROC-GOTOMIN-DUT	DUT Originated GoToMin
TDB.2.2.12.1	PROT-PROC-SR-TSTR	Tester Originated Soft Reset
TDB.2.2.12.2	PROT-PROC-SR-DUT	DUT Originated Soft Reset
TDB.2.2.13.1	PROT-PROC-HR-TSTR	Tester Originated Hard Reset
TDB.2.2.13.2	PROT-PROC-HR-DUT	DUT Originated Hard Reset
TDB.2.2.14	PROT-PROC-BIST-TSTR	Tester Originated BIST

5.7 Dual-Role Device – Provider/Consumer Tests

5.7.1 Primary Dual Role Device – Provider/Consumer Tests

Note that test BMC-PROT-BIST-NOT-5V-SRC is required only for devices which support greater than 5 volts.

Test Ref #	Test Name	Test Description
	Power Rules Tests	
PDSPEC10.10.2	SOURCE-POWER-RULES	Provider Power Rules Test
PDSPEC10.10.3	SINK-POWER-RULES	Consumer Power Rules Test
	BMC Physical Layer Tests - Transmit	
TDA.2.1.1.1	BMC-PHY-TX-EYE	BMC Transmitter Eye Diagram
TDA.2.1.1.2	BMC-PHY-TX-BIT	BMC Transmit Bit Rate and Bit Drift Rate
	BMC Physical Layer Tests - Receive	
TDA.2.1.2.1	BMC-PHY-RX-BUSIDL	BMC Bus Idle Detection
TDA.2.1.2.2	CAB-DP-PHY-RX-BUSIDL	BMC Receive Interference Rejection
	BMC Physical Layer Tests - Miscellaneous	
TDA.2.1.3.1	BMC-PHY-TERM	BMC Termination Impedance
TDA.2.1.3.2	BMC-PHY-MSG	BMC PHY Level Message
	Protocol-Specific Message Check Tests	
TDA.2.2.1	BMC-PROT-SEQ-GETCAPS	Get_Source_Cap and Get_Sink_Cap
TDA.2.2.2.1	BMC-PROT-SEQ-CHKCAP-P-PC	Check Capabilities (3A Marked)
TDA.2.2.2.2	BMC-PROT-SEQ-CHKCAP-NOMRK-P-PC	Check Capabilities (Unmarked)
TDA.2.2.3	BMC-PROT-SEQ-DRSWAP	Dual Role Swap
TDA.2.2.4	BMC-PROT-SEQ-VCSWAP	Vconn Swap
TDA.2.2.6	BMC-SEQ-PRSWAP	Reject Swap – Consumer / Provider
TDA.2.2.7	BMC-PROT-BIST-NOT-5V-SRC	BIST Functionality at Above 5V
TDA.2.2.8	BMC-PROT-REV-NUM	Revision Number
	Power Source/Sink Tests	
TDA.2.3.1.1	BMC-POW-SRC-LOAD-P-PC	Source Dynamic Load – Provider or Provider/Consumer
TDA.2.3.2.1	BMC-POW-SRC-TRANS-P-PC	PDO Transition – Source, Provider or Provider/Consumer
TDA.2.3.3.2	BMC-POW-SNK-TRANS-PC	PDO Transition – Current Draw and Suspend – Sink, Provider/Consumer

5.7.2 Secondary Dual-Role Device – Provider/Consumer Tests

5.7.2.1 Secondary Message Check Tests

Each of the following tests is performed whenever the message named in the Test Description is used.

Test Ref #	Test Name	Test Description
TDB.1.1.1	PHY-MSG-GEN	PHY Level General Message (SOP*)
TDB.2.1.2.1	PROT-MSG-HDR	Message Header Checks – except GoodCRC
TDB.2.1.2.2	PROT-MSG-HDR-GCRC	Message Header Checks – GoodCRC
TDB.2.1.3	PROT-MSG-CTRL	Control Message Checks
TDB.2.1.3.1	PROT-MSG-CTRL-PING	Ping Checks
TDB.2.1.4.1.1	PROT-MSG-DATA-SRC-CAP	Source Capability Message Checks

Test Ref #	Test Name	Test Description
TDB.2.1.4.1.2	PROT-MSG-DATA-SNK-CAP	Sink Capability Message Checks
TDB.2.1.4.2	PROT-MSG-DATA-REQ	Request Message Checks
TDB.2.1.4.3	PROT-MSG-DATA-VEND	Vendor Defined Message Checks
TDB.2.1.4.4.1.1	PROT-MSG-DATA-VDM-ID-INIT	Discover ID Initiator Message Checks
TDB.2.1.4.4.1.2	PROT-MSG-DATA-VDM-ID-ACK	Discover ID ACK Message Checks
TDB.2.1.4.4.2.1	PROT-MSG-DATA-VDM-SVID-INIT	Discover SVIDs Initiator Message Checks
TDB.2.1.4.4.2.2	PROT-MSG-DATA-VDM-SVID-ACK	Discover SVIDs ACK Message Checks
TDB.2.1.4.4.3.1	PROT-MSG-DATA-VDM-MODE-INIT	Discover Modes Initiator Message Check
TDB.2.1.4.4.3.2	PROT-MSG-DATA-VDM-MODE-ACK	Discover Modes ACK Message Check
TDB.2.1.4.4.4	PROT-MSG-DATA-VDM-ENTER-MODE	Enter Mode Message Check
TDB.2.1.4.4.5	PROT-MSG-DATA-VDM-EXIT-MODE	Exit Mode Message Check
TDB.2.1.4.4.6	PROT-MSG-DATA-VDM-ATT	Attention Message Check

5.7.2.2 Secondary Procedure Check Tests

Each of the following tests is performed whenever the message named in the Test Description is used.

Test Ref #	Test Name	Test Description
TDB.2.2.1.1	PROT-PROC-AMS_1	Atomic Message Sequence
TDB.2.2.2.1	PROT-PROC-GOODCRC-TSTR	GoodCRC sent by Tester
TDB.2.2.2.2	PROT-PROC-GOODCRC-DUT	GoodCRC sent by Unit Under Test (DUT)
TDB.2.2.3.1.1	PROT-PROC-SWAP-TSTR-SNK	Tester (Sink) Originated Swap
TDB.2.2.3.1.2	PROT-PROC-SWAP-TSTR-SRC	Tester (Source) Originated Swap
TDB.2.2.3.2.1	PROT-PROC-SWAP-DUT-SNK	DUT (Sink) Originated Swap
TDB.2.2.3.2.2	PROT-PROC-SWAP-DUT-SRC	DUT (Source) Originated Swap
TDB.2.2.4	PROT-PROC-PSSOURCEOFFTIMER	Test PSSourceOffTimer when not Swapped
TDB.2.2.5	PROT-PROC-PSSOURCEONTIMER	Test PSSourceOnTimer when not Swapped
TDB.2.2.6	PROT-PROC-PING	Send Ping from Tester
TDB.2.2.7.1	PROT-PROC-REQ-TSTR	Tester Originated Request
TDB.2.2.7.2	PROT-PROC-REQ-UUR	DUT Originated Request
TDB.2.2.8.1	PROT-PROC-SRCCAPS-TSTR	Tester Originated Source Capabilities
TDB.2.2.8.2	PROT-PROC-SRCCAPS-DUT	DUT Originated Source Capabilities
TDB.2.2.9.1	PROT-PROC-GETSRCCAPS-TSTR	Tester Originated Get_Source_Cap
TDB.2.2.9.2	PROT-PROC-GETSRCCAPS-DUT	DUT Originated Get_Source_Cap
TDB.2.2.10.1	PROT-PROC-GETSNKCAPS-TSTR	Tester Originated Get_Sink_Cap
TDB.2.2.10.2	PROT-PROC-GETSNKCAPS-DUT	DUT Originated Get_Sink_Cap
TDB.2.2.11.1	PROT-PROC-GOTOMIN-TSTR	Tester Originated GoToMin
TDB.2.2.11.2	PROT-PROC-GOTOMIN-DUT	DUT Originated GoToMin
TDB.2.2.12.1	PROT-PROC-SR-TSTR	Tester Originated Soft Reset
TDB.2.2.12.2	PROT-PROC-SR-DUT	DUT Originated Soft Reset
TDB.2.2.13.1	PROT-PROC-HR-TSTR	Tester Originated Hard Reset
TDB.2.2.13.2	PROT-PROC-HR-DUT	DUT Originated Hard Reset
TDB.2.2.14	PROT-PROC-BIST-TSTR	Tester Originated BIST

Chapter 13 of the Test Plan describes in detail the test steps for each of the tests in the overview. Detailed description of each test goes beyond the scope of this MOI. Please refer to the test plan for detailed understanding of the tests.

5.8 Granite River Labs USB-PD Test Methodology

GRL's test solutions provide automated testing. GRL Power Delivery Compliance Test Software (GRL-USB-PD0) Rev.1.2 and higher is used in conjunction with GRL USB Type-C Test Controller (GRL-USB-PD-C1) to automate the tests in the USB Power Delivery Test Plan. GRL USB Power Delivery Software is run on a Win7 (or higher) oscilloscope. Three channels of the oscilloscope are used to capture the signals needed for testing. Channel 1 captures the active CC Line, Channel 2 captures Vbus, and Channel 3 captures the load current on Vbus.

5.9 Required Test Equipment

The required equipment needed to test USB Type-C components, reference designs, and end products is shown in the following table. The equipment referenced is based on each of the subsequent sections of this MOI.

For testing of all devices that support USB-PD:

- 1 ea. Win7 (or higher) Oscilloscope
- 1 ea. GRL's USB Power Delivery Compliance Software (GRL-USB-PD) installed on the oscilloscope's operating system
- 1 ea. GRL's USB Type-C Test Controller (GRL-USB-PD-C1) with external Power Supply
- 2 ea. Voltage Probes (see probe requirements below)

If device is a Power Consumer, Provider or DRP.

- Add 1 ea. Current Probe

If device is a Provider or DRP.

- Add 1 ea. Electronic Load (E-Load)

5.9.1 Oscilloscope, Probes, and Electronic Load

GRL-USB-PD Software supports multiple oscilloscope and electronic load platforms for testing. Refer to the vendor specific data sheets at http://graniteriverlabs.com/usb-pd/ for recommended oscilloscope, passive probes, current probes and electronic loads.

The oscilloscope should provide, at least:

Bandwidth of 500MHz or higher
Channel depth of 10-M samples is required for each Channel in high resolution mode. All the four channels have to be enabled.
Windows 7 OS, for running the GRL-USB-PD application
Adobe Reader, for viewing PDF files
Picture Viewer, for viewing waveform files
HighRes acquisition mode to average out sample-to-sample noise in the acquisition

The probes should provide at least:

For Oscilloscopes with 1 megohm input impedance:

- For CC probing use passive probes with low input capacitance
- For Vbus probing use passive probes with low input capacitance

For High Performance Oscilloscopes with 50Ohm input impedance:

- For CC probing use active probes for lowest noise performance
- For Vbus probing use passive probe with high impedance adapter

For Current measurement use Hall Effect current probe measurement to 5 Amps

The electronic Load should provide at least:

20 Volts

5 Amps – adjustable slew rate to 150mA/us, as defined in Chapter 7 of the USB-PD Specification

5.9.2 USB Power Delivery Compliance Software (GRL-USB-PD)

GRL's USB Power Delivery (GRL-USB-PD) Compliance Test Software is an oscilloscope-based software tool designed for testing to the USB Power Delivery (USB-PD) specification. GRL-USB-PD software, when used 'stand-alone' on any Windows-based oscilloscope, provides a simple and efficient way to perform USB-PD electrical parametric and protocol measurements. GRL-USB-PD provides waveform visibility and protocol analysis, making it ideal for design and debug of USB Type-C Power Delivery silicon and end products.

5.9.3 USB Type-C Test Controller (GRL-USB-PD-C1)

GRL's USB Type-C Test Controller Hardware (GRL-USB-PD-C1) works with GRL-USB-PD to perform compliance tests on USB Power Delivery or Type-C designs, supporting USB Power Delivery Protocol, Compliance, Decode, and Debug along with Electrical Measurements.

- Bi-Phase Mark Coded (BMC)
- Physical layer (BMC-PHY) tests - Chapter 5 of the USB-PD Specification
- Protocol layer (BMC-PROT) tests – Chapter 6 of the USB-PD Specification
- Power state (BMC-POW) tests – Chapter 7 of the USB-PD Specification

GRL-USB-PD-C1 automates testing through user-selected test suites.

5.10 Compliance Test Work Flow and Test Procedure

Figure 9 shows the work flow for USB-PD Compliance testing with GRL-USB-P test solutions.

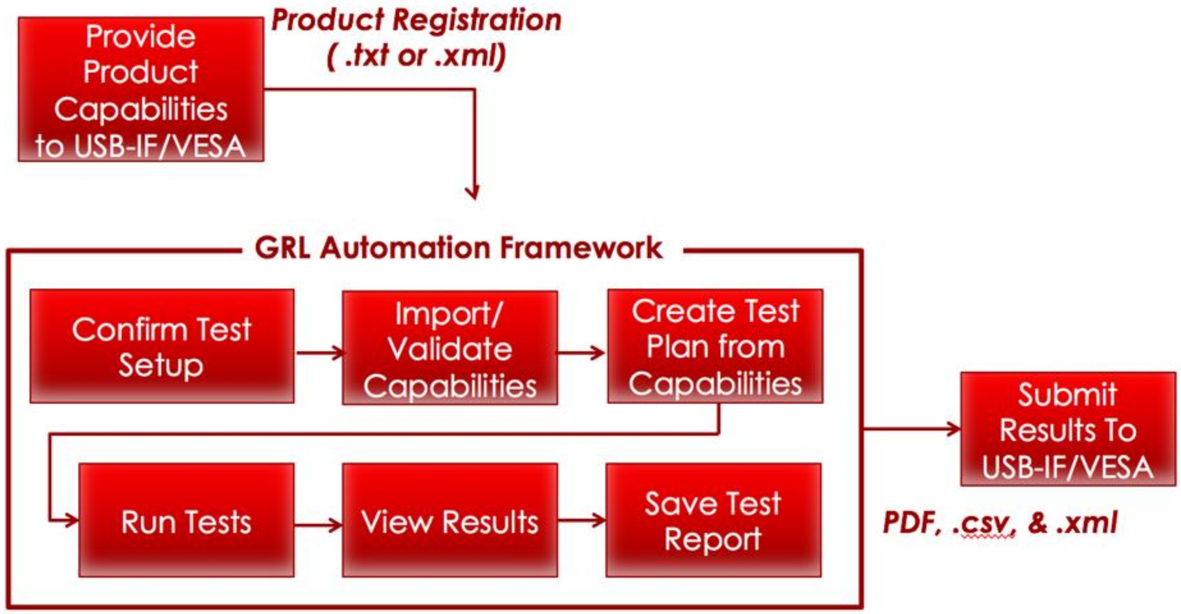


FIGURE 9: TEST WORK FLOW DIAGRAM

5.10.1 Providing Product Capabilities for Testing

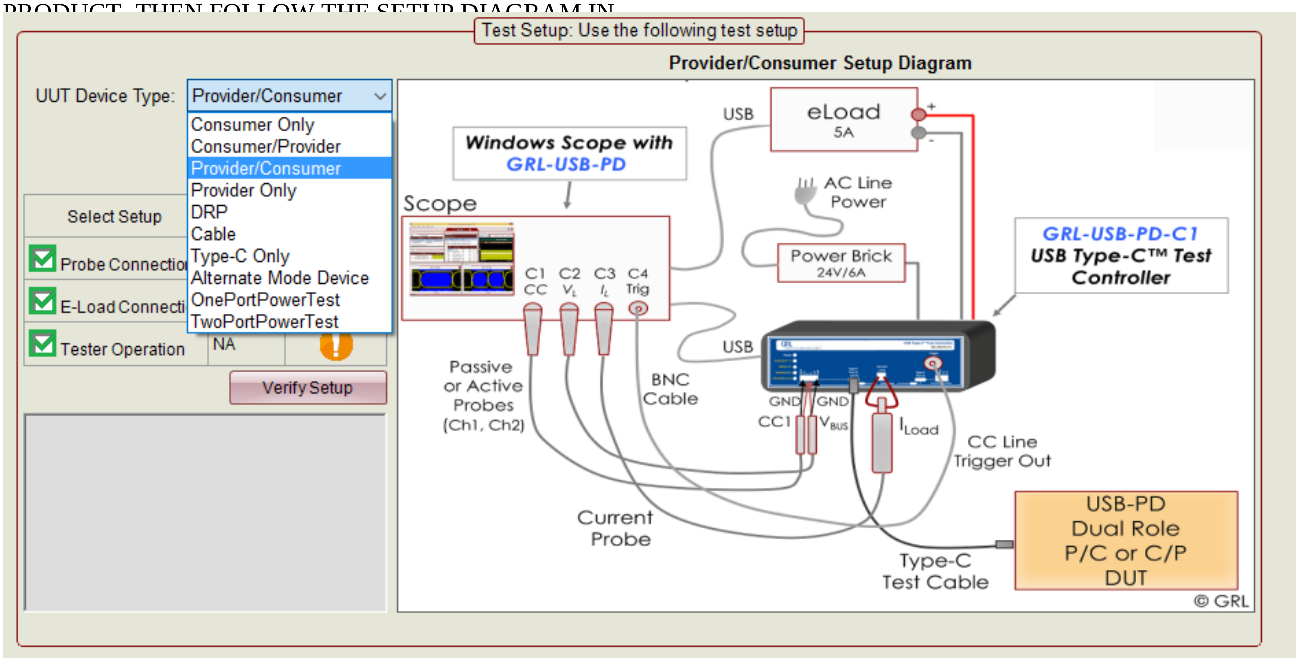
Before testing can begin, a device vendor text file must be created. This file is created using the ***USB PD Vendor Info File Generator*** available for download at the USB-IF website at: http://www.usb.org/developers/tools/PDVendorInfoFileGenerator_1.0.0.1.exe

5.10.2 Confirm the Test Setup for the Device Under Test

1) Follow Procedures in Appendix A, B, and C for initial Software, Hardware and Controller Setup.
2) Go to the GRL-USB-PD Software **Test Setup Connection** menu, select the DUT Device Type and make the oscilloscope probe connections shown in the **Setup Diagram** appropriate for the device type.

1. If the device is a tethered device (Type-C Cable permanently attached to the DUT), then select the **DUT Tethered** checkbox. This applies the Rx Mask when performing the BMC Eye testing. Otherwise, use the 25cm (10 inch) test cable for testing, and the Tx Mask will be applied.The RX Mask testing is done with no load on Vbus.

If the device is a **DRP**, **Consumer/Provider**, **Provider/Consumer**, or **Provider** product, then follow the setup diagram in



3) Figure 10,

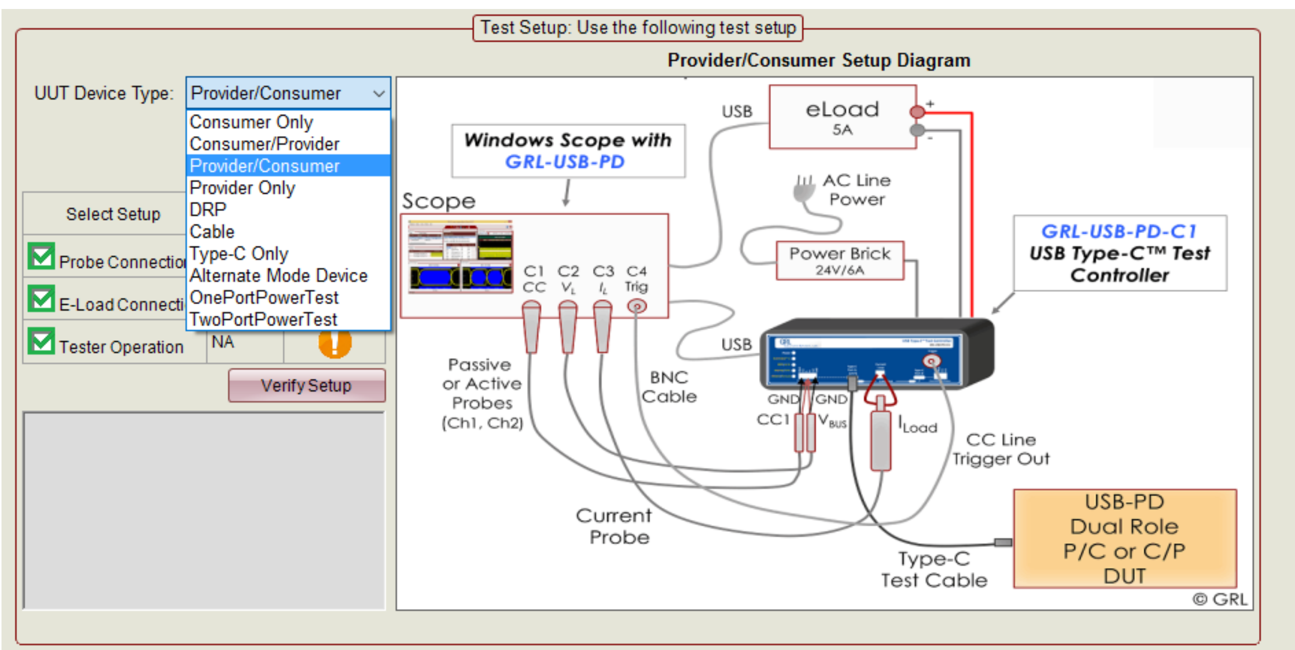


Figure 10: DUT Test Setup Diagram #1

1. Connect **Ch1** Passive Probe to **CC1-GND** at **Port-A Probing Points** input of GRL-USB-PD-C1 using the **Probe-Ext1** board.

Note: CC1 and CC2 signals may be swapped depending on the 'flip orientation' of the test cable. If CC1 does not appear on Ch1 on initial test, then either flip the test cable or change the probe to CC2.

2. Connect **Ch2** Passive Probe to **Vbus** and **GND** at **Port-A Probing Points** input.

   Note: Before testing, follow the vendor-specific procedures for compensating the passive probes being used for voltage measurement. This may include automatic and/or manual adjustments.

3. Connect **Ch3** Current Probe to the **Current Loop** input of GRL-USB-PD-C1 using the **Current Loop** connector.

   Note: When testing, the software will prompt you for which direction to orient the current flow direct on the current probe, referenced to the Current Loop direction on the front panel.

   Note: Follow the oscilloscope vendor's procedures for setting up the current probe for proper measurement Units and Offset, and for proper Degauss of the current probe.

4. Connect **Ch4** to **Trigger Output connector** using BNC cable.
5. Connect the **Type-C Test Cable** connected to the DUT to the **Type-C Port A** Connection on GRL-USB-PD-C1.
6. Confirm that the setup appears as shown in Figure 11 and Figure 12.

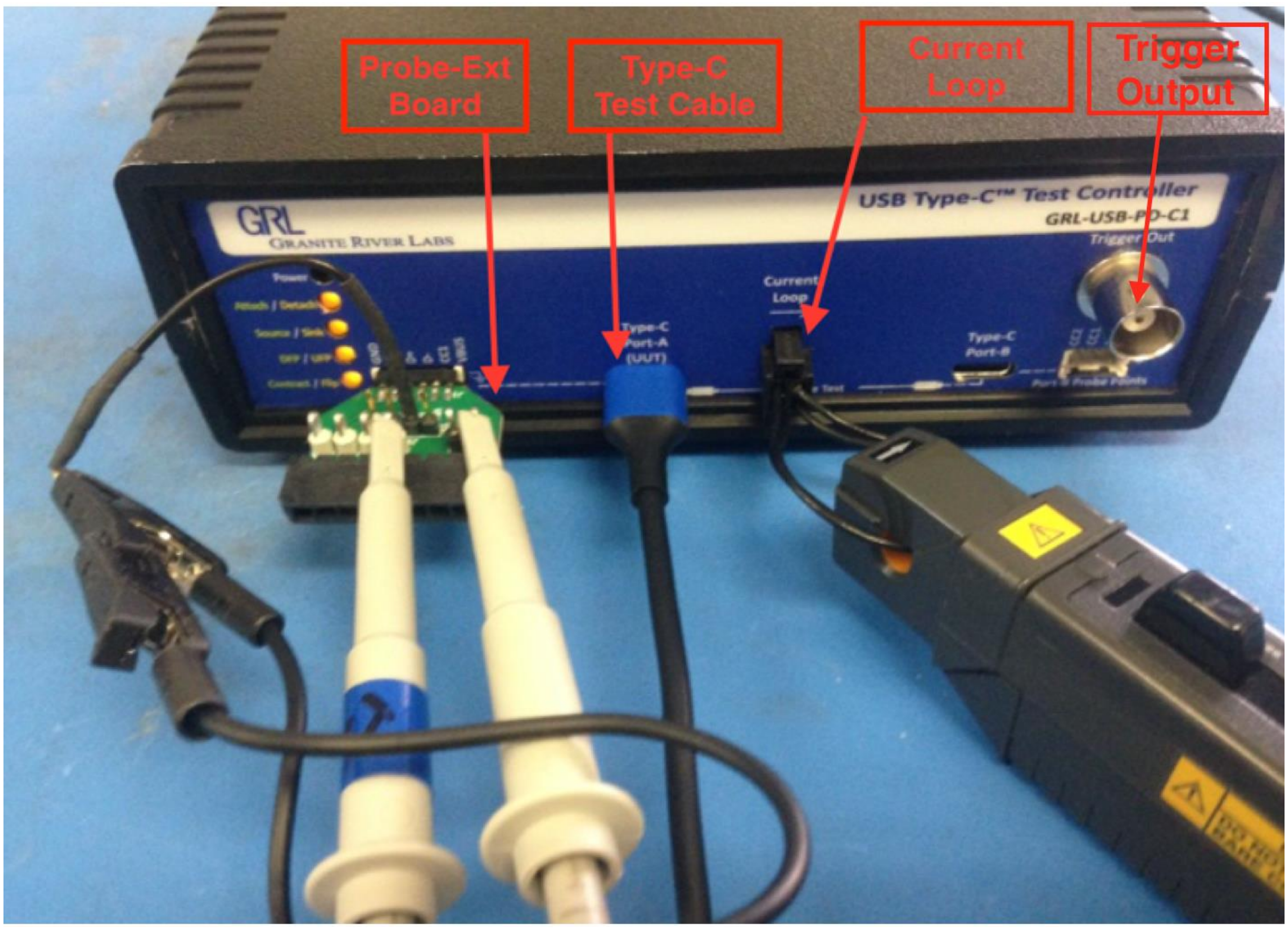


FIGURE 11: FRONT PANEL SETUP

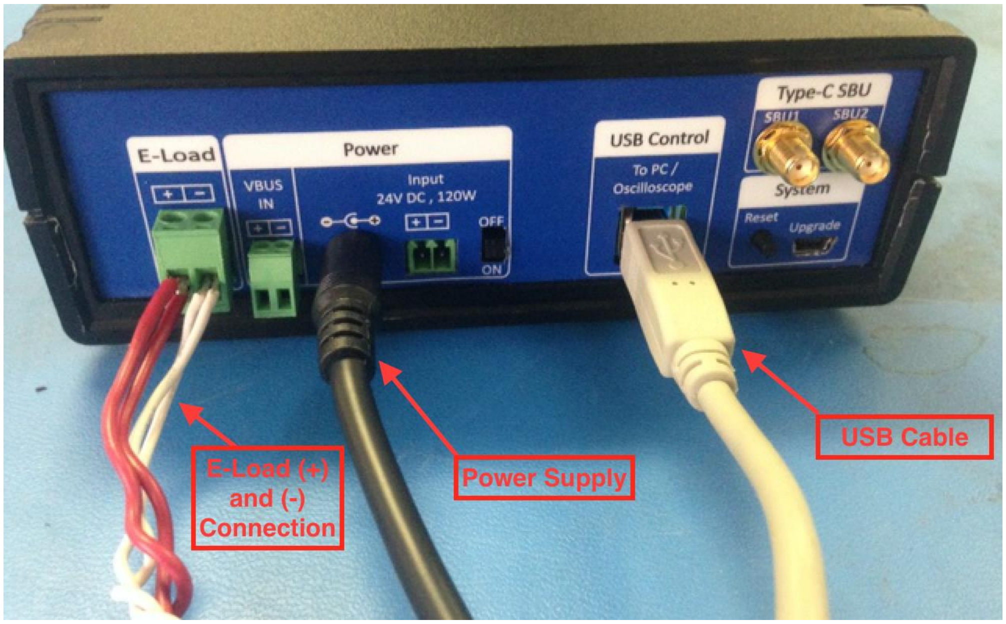
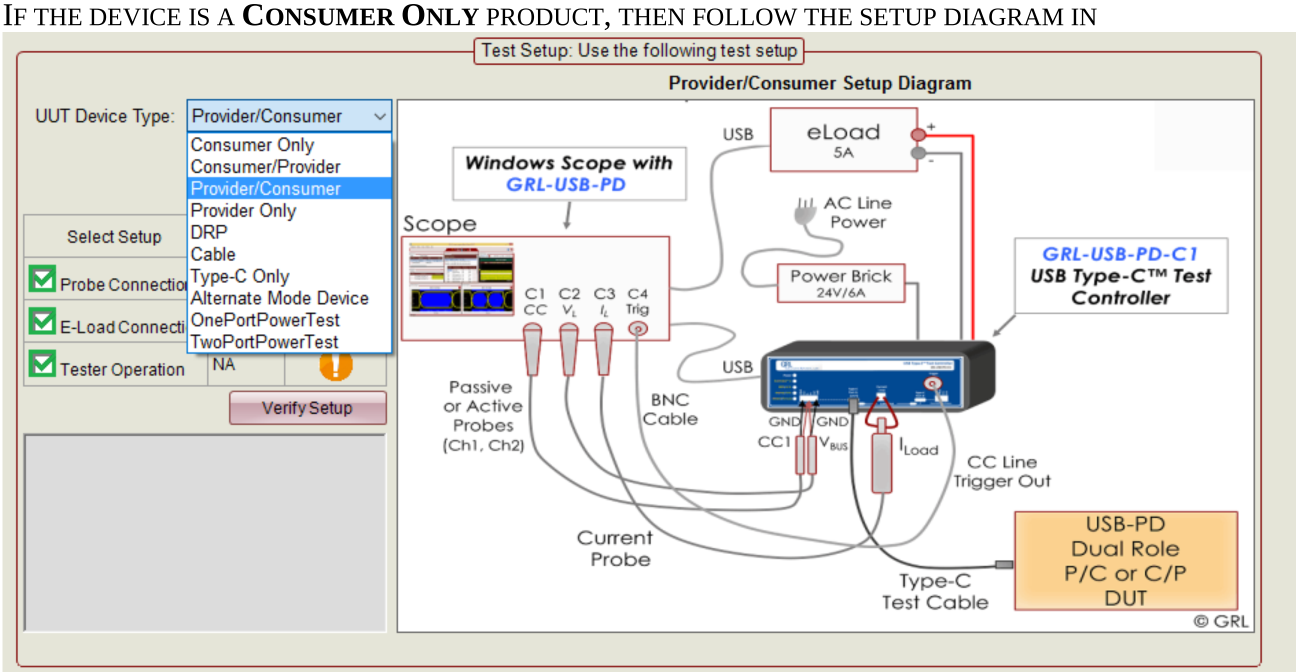


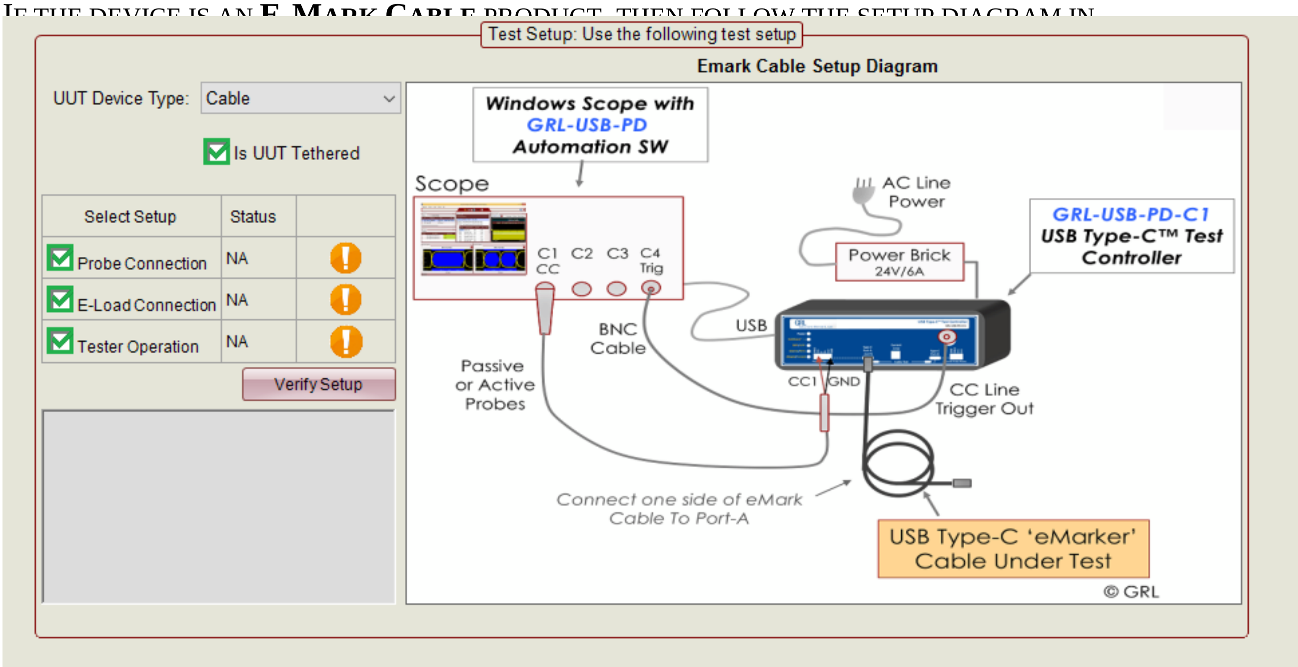
FIGURE 12: REAR PANEL SETUP

IF THE DEVICE IS A **CONSUMER ONLY** PRODUCT, THEN FOLLOW THE SETUP DIAGRAM IN



4) Figure 10, except that E-Load is not required.

If the device is an E-Mark Cable product, then follow the setup diagram in



5) Figure 13.

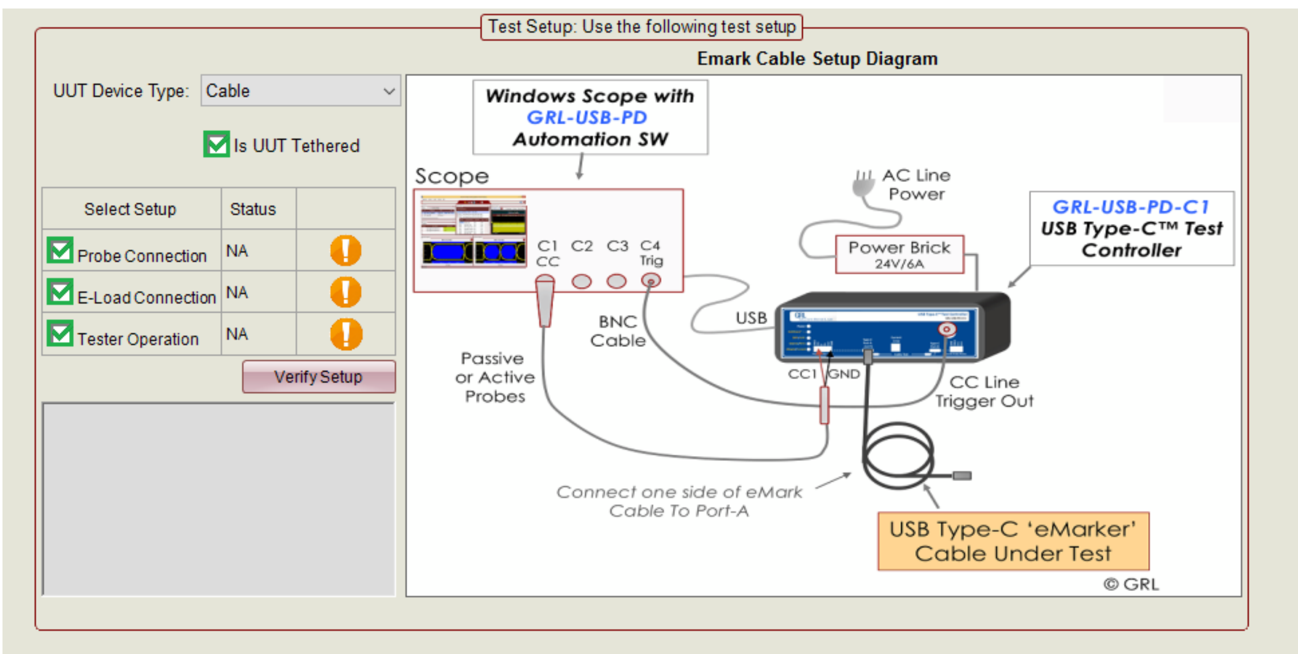


FIGURE 13: E-MARK CABLE TEST SETUP DIAGRAM

1. Connect **Ch1** Passive Probe to **CC1-GND** at **Port-A Probing Points** input of GRL-USB-PD-C1 using the **Probe-Ext1** board.

Note: CC1 and CC2 signals may be swapped depending on the 'flip orientation' of the test cable. If CC1 does not appear on Ch1 on initial test, then either flip the test cable.

2. Connect one end of the USB Type-C Cable DUT to the **Type-C Port-A** Connection on GRL-USB-PD-C1.

   6) Go to the Decoder Configuration menu.

1. Select **Live** as the Source Type. Offline is used to analyze offline waveforms that were previously captured. (See Section 11 for details on how to analyze waveforms offline.)
2. Confirm **CC Line** voltage is shown as being captured by **Ch1**.
3. Confirm **Vbus** voltage is shown as being captured by **Ch2**.
4. Confirm **ILoad** current is shown as being captured by **Ch3**.
5. Confirm the **Trigger Channel** checkbox is selected and set to **Ch4**.

Note: The required scope channel selections depend on the type of device being tested.

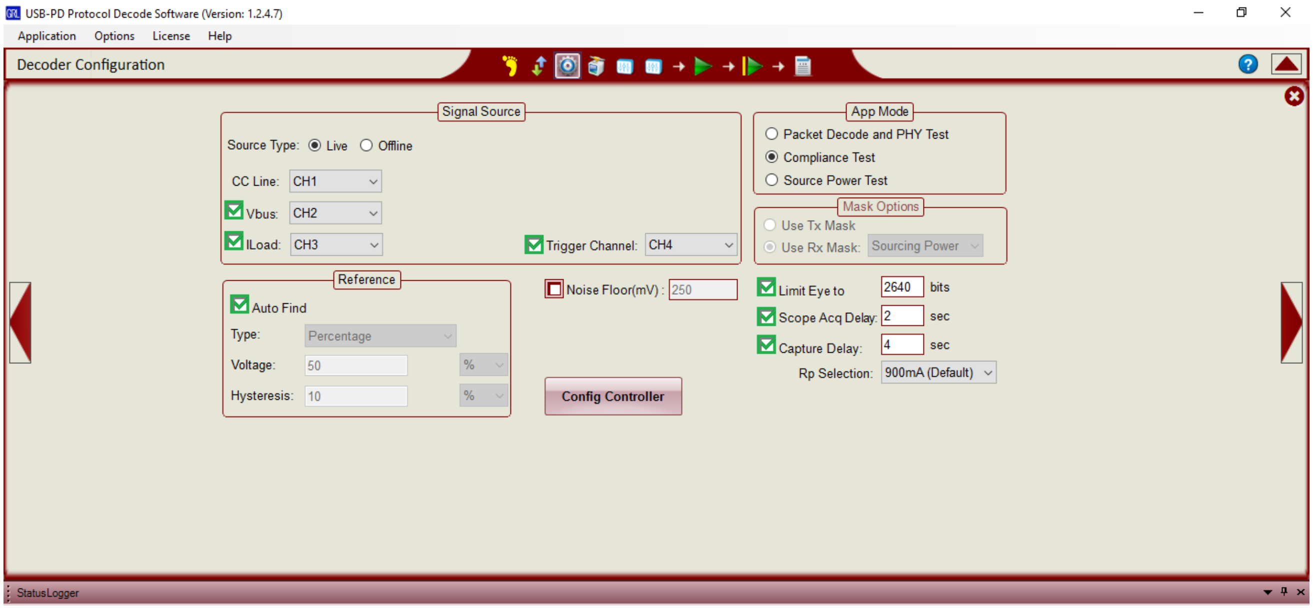
6. Confirm **Reference** is selected as **Absolute** at Voltage of 0.5625V (default). (See Section 12 for example of how the Reference control can be used to adjust the reference level on BMC Eye Clock recovery.)
7. Confirm **Compliance Test** is selected in the **App Mode** section. (See Section 11 for the use of **Packet Decode and PHY Test** feature.)
8. Confirm Use **TX Mask** is selected I the Mask Option.

   i) If testing the DUT with a Type-C Test Cable. If the DUT is a Tethered Device (Cable permanently attached to the DUT, then Use Rx Mask will be selected with Neutral Power condition.

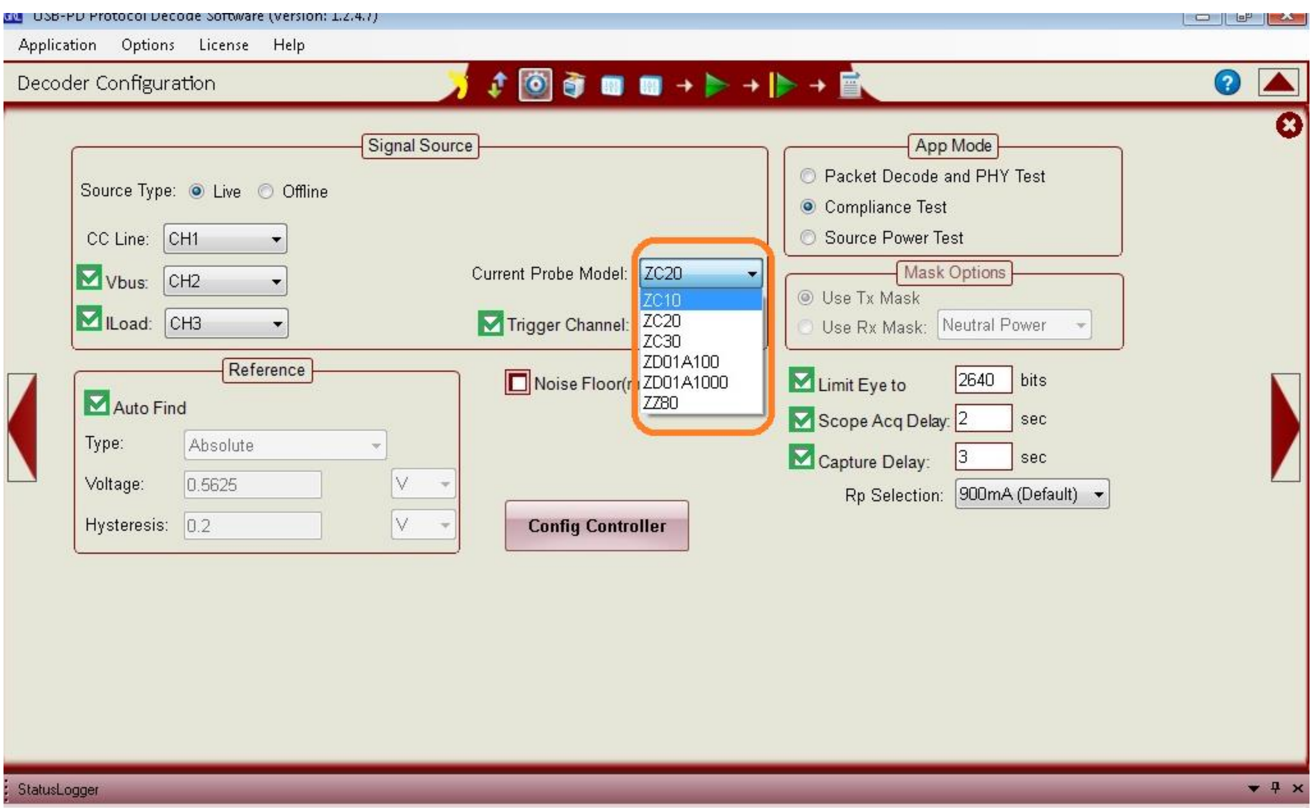
9. For Compliance Testing, use the Trigger Out Connector in the Front Panel of the controller as an oscilloscope trigger. Check the Trigger Channel box and use CH4 as trigger source. The **Trigger Channel** selection in the Configuration Panel may remain un-checked if it is desired to trigger on CC line only.

   i) For debug purposes, this selection is provided to set which oscilloscope channel is used to connect to the Trigger BMC Connector on the front panel. When this connection is made, a trigger signal is sent to the oscilloscope every time a CC packet is detected on the CC1 line.

10. For Compliance Testing, leave the **Noise Floor** unchecked, and the **Scope Acquisition Delay** and **Capture Delay** at their default values.



11. In case of Rohde & Schwarz oscilloscope when the current channel is not automatically detected by the scope the Current Channel model can be configured manually as show below.



l) The default Rp value is 900mA for the Compliance Test. Each time before running the compliance test the Rp value can be customized as shown below.

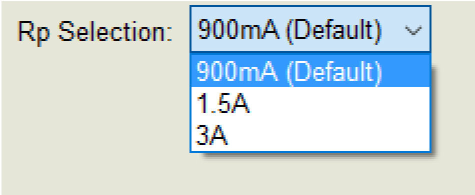


FIGURE 14: DECODER CONFIGURATION MENU

5.10.3 Import and Validate DUT Capabilities

7) Copy the Vendor Information File created (as created by the USB-IF tool, referenced in 5.10.1) over to the oscilloscope being used for testing.
8) Go to the GRL-USB-PD Software **Product Capabilities** menu.
9) Select the **Reset Capabilities** button to clear the menu for a new test.
10) The version of the ISB-IF vendor information tool supported is displayed as shown below

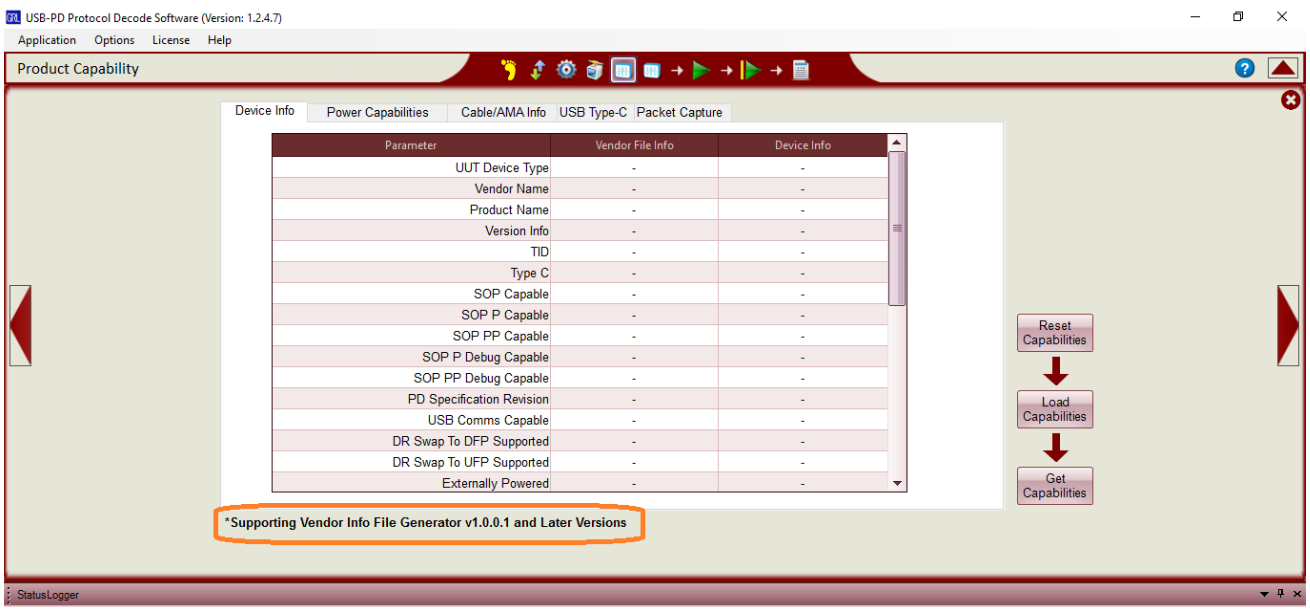


FIGURE 15: PRODUCT CAPABILITIES MENU

11) Select the **Load Capabilities** button.

1. Navigate to the Vendor Info.txt file on the file system and press **Open**.
2. Once the vendor file has been loaded, the Device Info tab shows the fields loaded from the Vendor Info file for device information.

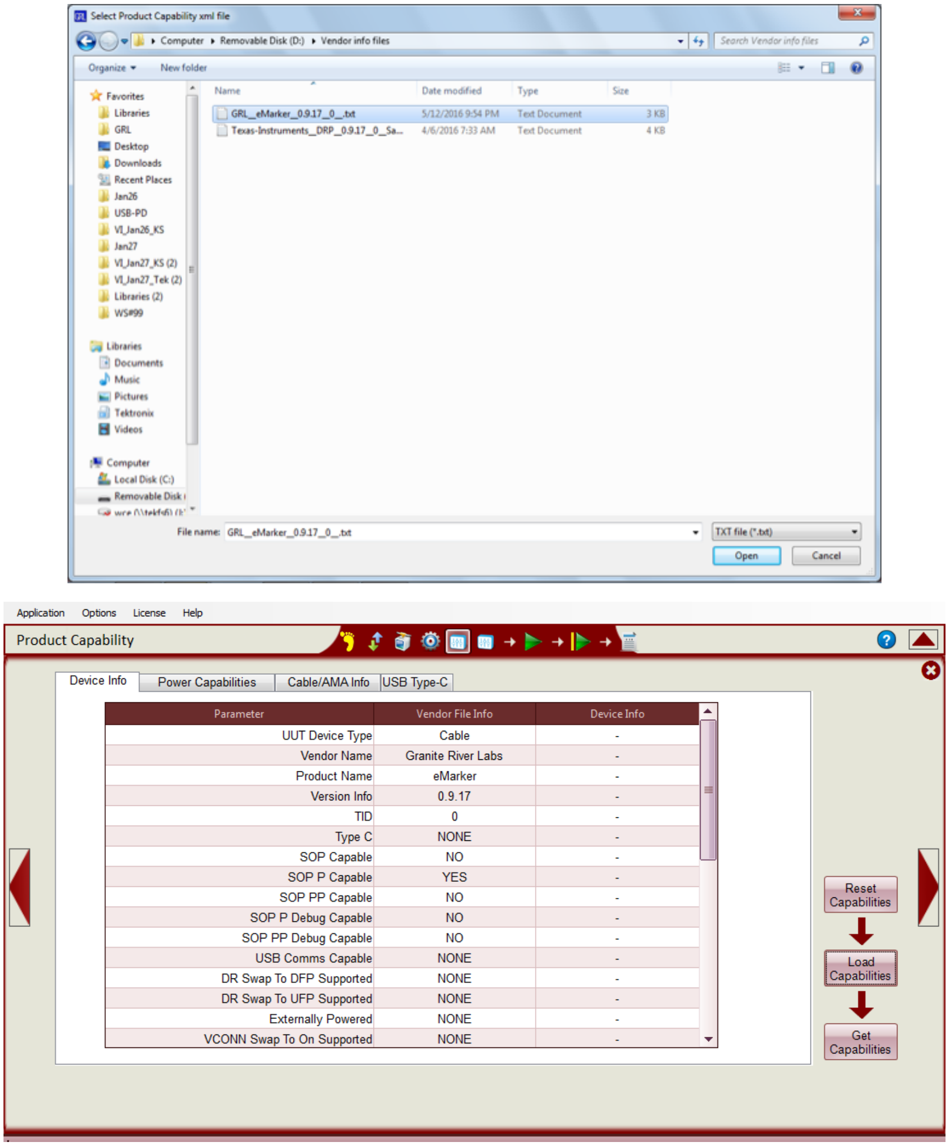


FIGURE 16: LOAD CAPABILITIES FROM FILE

12) Reset PD Controller and then press the **Get Capabilities** button. This causes the Controller to do a “Get Capabilities” from the DUT using USB-PD Protocol. When properly executed, the left-hand column is then populated with the device’s information. A message in the StatusLogger indicates that the “Product Capabilities updated”. Now the Vendor File Info (right-hand column) and actual Device Info (left-hand column) can be

compared for inconsistencies. Data from the Vendor Info file is used for many of the compliance tests.

Note: The presence of a Vendor Info file is not required to perform a test on the DUT. However, not all tests can be completed without the information from the Vendor Info file. If a Vendor Info file is not available for testing, then Step #11), above, can be skipped.

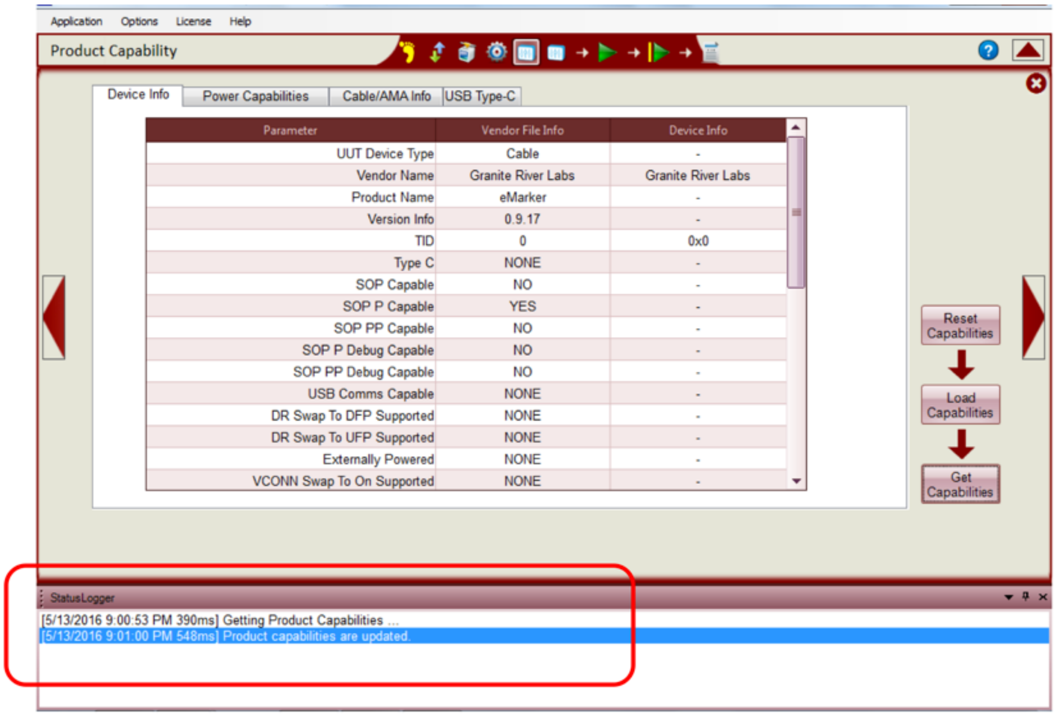
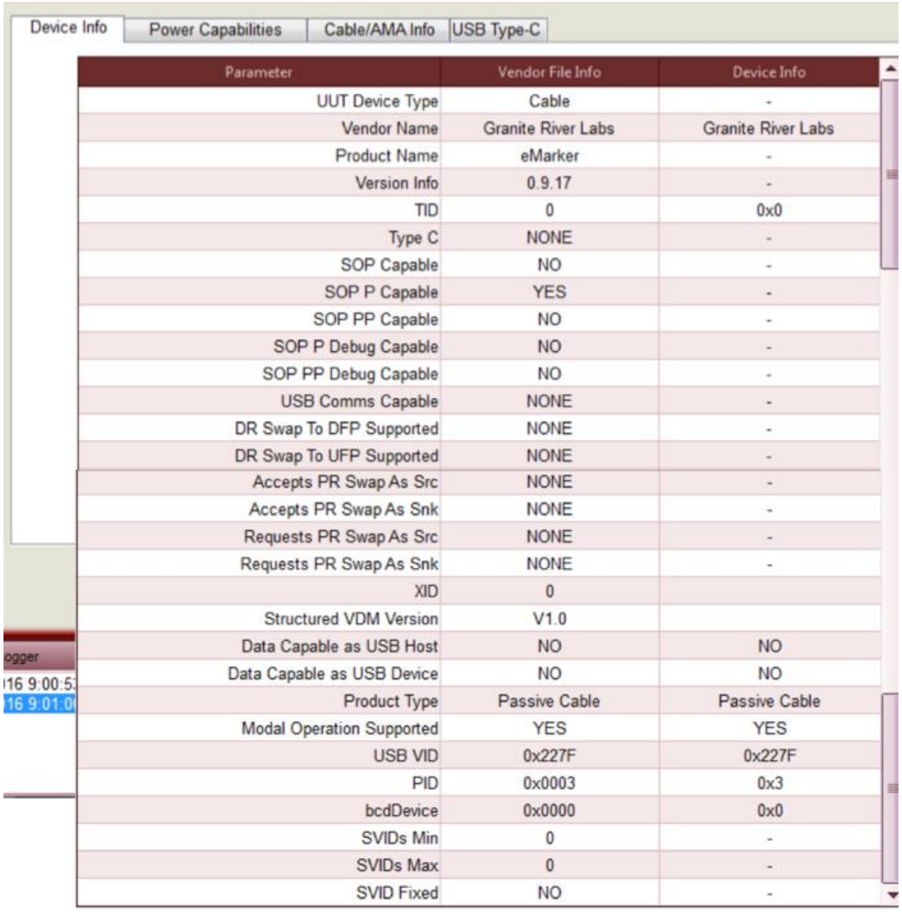


FIGURE 17: GET CAPABILITIES TRANSACTION

Note: If the left-hand column does not populate with the Vendor Name, then reset the Controller's power, disconnect and reconnect the DUT to the Controller, and try again.

1. The **Device Info** tab summarizes all of the device information. Shown in Figure 18 is the information for the eMark Cable included with the Controller. The Vendor Name, Product

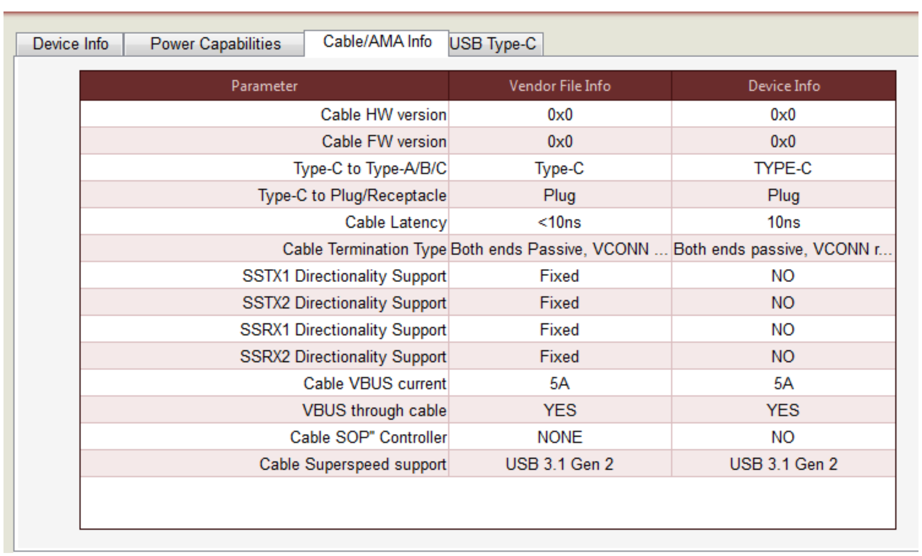
Type, USB PID (Product ID), USB VID (Vendor ID) are all read from the cable's eMarker chip.



Parameter	Vendor File Info	Device Info
UUT Device Type	Cable	-
Vendor Name	Granite River Labs	Granite River Labs
Product Name	eMarker	-
Version Info	0.9.17	-
TID	0	0x0
Type C	NONE	-
SOP Capable	NO	-
SOP P Capable	YES	-
SOP PP Capable	NO	-
SOP P Debug Capable	NO	-
SOP PP Debug Capable	NO	-
USB Comms Capable	NONE	-
DR Swap To DFP Supported	NONE	-
DR Swap To UFP Supported	NONE	-
Accepts PR Swap As Src	NONE	-
Accepts PR Swap As Snk	NONE	-
Requests PR Swap As Src	NONE	-
Requests PR Swap As Snk	NONE	-
XID	0	
Structured VDM Version	V1.0	
Data Capable as USB Host	NO	NO
Data Capable as USB Device	NO	NO
Product Type	Passive Cable	Passive Cable
Modal Operation Supported	YES	YES
USB VID	0x227F	0x227F
PID	0x0003	0x3
bcdDevice	0x0000	0x0
SVIDs Min	0	-
SVIDs Max	0	-
SVID Fixed	NO	-

FIGURE 18: DEVICE INFORMATION

2. The **Cable/AMA** tab provides information on Cable and Alt Mode Adapter SVIDs, as read from the DUT. An example is shown in Figure 19.



Parameter	Vendor File Info	Device Info
Cable HW version	0x0	0x0
Cable FW version	0x0	0x0
Type-C to Type-A/B/C	Type-C	TYPE-C
Type-C to Plug/Receptacle	Plug	Plug
Cable Latency	<10ns	10ns
Cable Termination Type	Both ends Passive, VCONN ...	Both ends passive, VCONN r...
SSTX1 Directionality Support	Fixed	NO
SSTX2 Directionality Support	Fixed	NO
SSRX1 Directionality Support	Fixed	NO
SSRX2 Directionality Support	Fixed	NO
Cable VBUS current	5A	5A
VBUS through cable	YES	YES
Cable SOP" Controller	NONE	NO
Cable Superspeed support	USB 3.1 Gen 2	USB 3.1 Gen 2

FIGURE 19: CABLE/AMA INFORMATION

3. The Power Capabilities tab provides the DUT's Source and Sink PID information. In Figure 20, the DUT is a Provider which supports three PDOs – 5V and 12V at 3A.

Device Info | Power Capabilities | Cable/AMA Info | USB Type-C

Parameter	Vendor File Info	Device Info
PD Power as Source	-	
Rp Value	-	
USB Suspend may be cleared	-	NO
Send Ping	-	NONE
No of Source PDOs	-	2
	-	
Supply Type #1	-	Fixed
Peak Current #1	-	0
Voltage #1	-	5
Max Current #1	-	3
	-	
Supply Type #2	-	Fixed
Peak Current #2	-	0
Voltage #2	-	12
Max Current #2	-	3

FIGURE 20: POWER CAPABILITIES

4. The Type-C tab provides Type-C capabilities and termination of the DUT and its accessory support. In Figure 21, the DUT's pull-up termination is 1.5A, and there is no accessory support.

Device Info | Power Capabilities | Cable/AMA Info | USB Type-C

Parameter	Vendor File Info	Device Info
Captive Cable	NO	-
RP Value	1.5A	-
Type C State Machine	SRC	-
Type C Can Act As Host	NO	-
Type C Host Speed		-
Type C Can Act As Device	NO	-
Type C Device Speed		-
Type C Implements Try SRC	NONE	-
Type C Implements Try SNK	NONE	-
Type C Is VCONN Powered Accessory	NONE	-
Type C Supports VCONN Powered Accessory	NONE	-
Type C Supports Audio Accessory	NO	-

FIGURE 21: USB TYPE-C CAPABILITIES

5.10.4 Create Test Plan from Capabilities

The combination of the Device Type and the Device Capabilities allows the GRL-USB-PD software to determine what tests need to be performed on the DUT.

Go to the Test Selection Menu and Select the desired tests to perform. All listed tests must be run for Compliance.

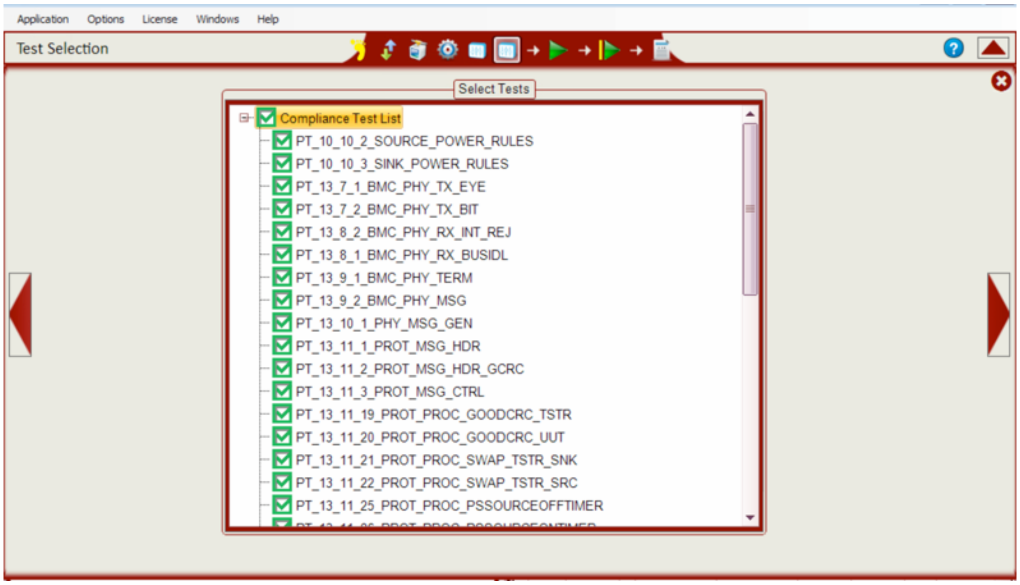


FIGURE 22: TEST SELECTION MENU

5.10.5 Run Tests

1) To run the tests, press the **Run** button.

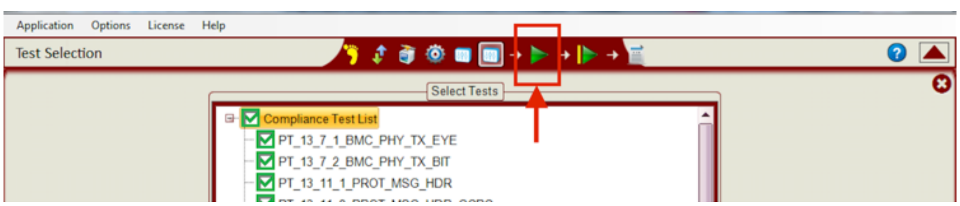


FIGURE 23: “RUN” BUTTON

2) The screen will display a wait icon while the tests are executing.

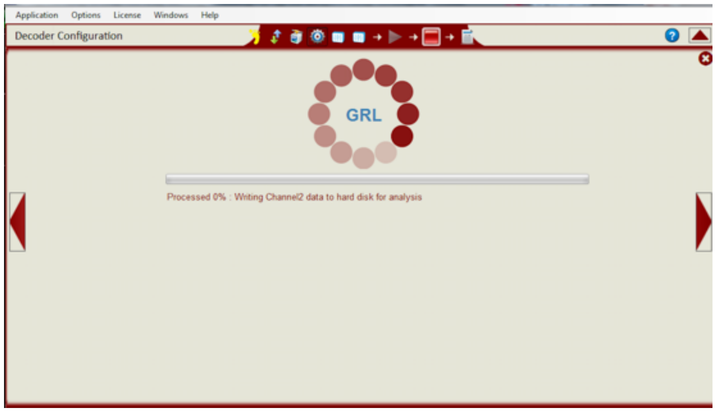


FIGURE 24: "EXECUTION" WINDOW

3) The GRL-USB-PD software automates all the tests that are selected. During test execution, some messages would appear to make sure the proper oscilloscope acquisition is seen by the operator as shown below.

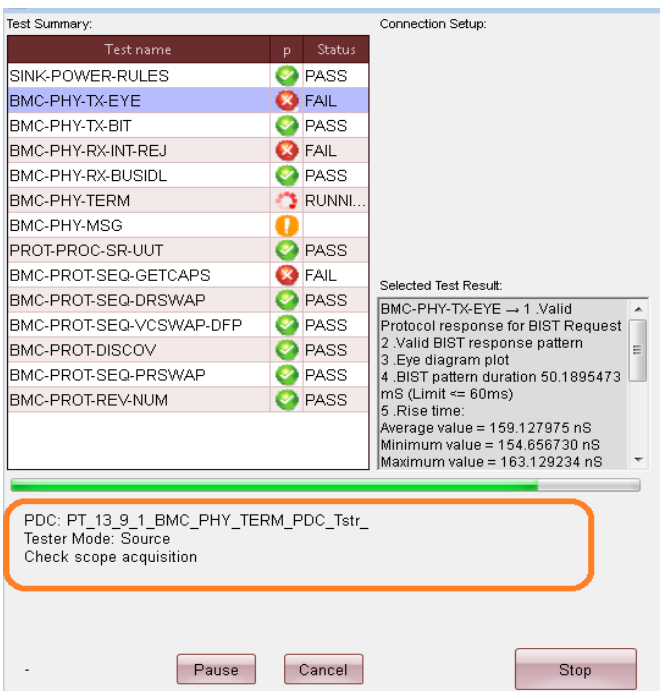


FIGURE 25: TEST RESULTS DISPLAY

4) The Compliance Test Results will be updated dynamically during test execution. While the tests are running, by clicking the test that had failed the operator would be able to see the failure description as shown below.

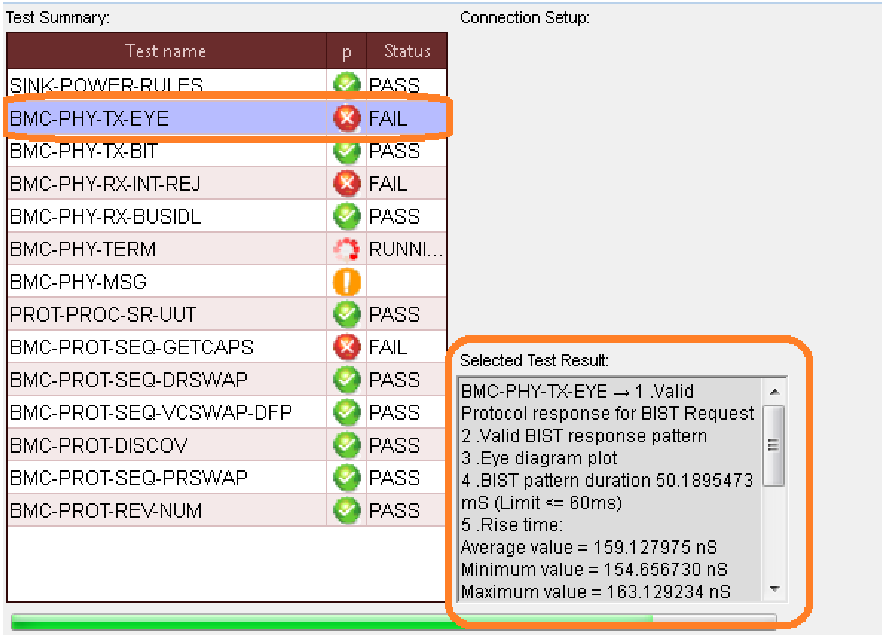


FIGURE 26: FAILURE DESCRIPTION

Note: Some dialog boxes DO require user input during testing. Examples are:

1. **Current Probe Orientation**– Image showing the Current probe orientation is displayed during the execution of e-Load Test Cases. The user has to connect the Current probe in the proper orientation with respect to the Load arrow on the front panel of the Controller. When this image appears, confirm the current probe arrow current flow is in the direction of the current being measured. For current flowing towards the eLoad (source testing), the current probe should be connected to the current loop on the front of the controller such that the arrow

on the probe is in in the opposite direction of the current flow as shown below. For Consumer test the probe is connected so that the arrows are in the same direction.

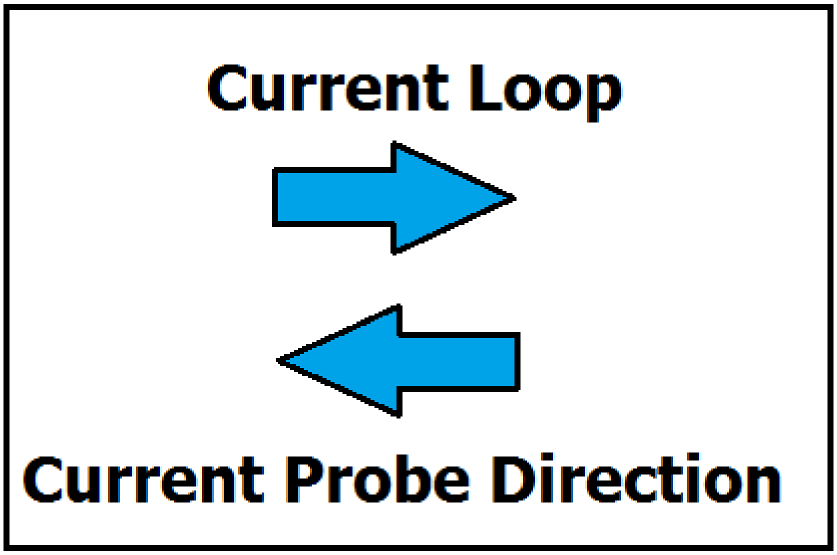


FIGURE 27: CONNECTING CURRENT PROBE

5.10.6 View Results

1) Once the compliance testing is complete, the test results will appear in the Results window. Pass/Fail results on left hand side of the window and Packet information appears on the right.

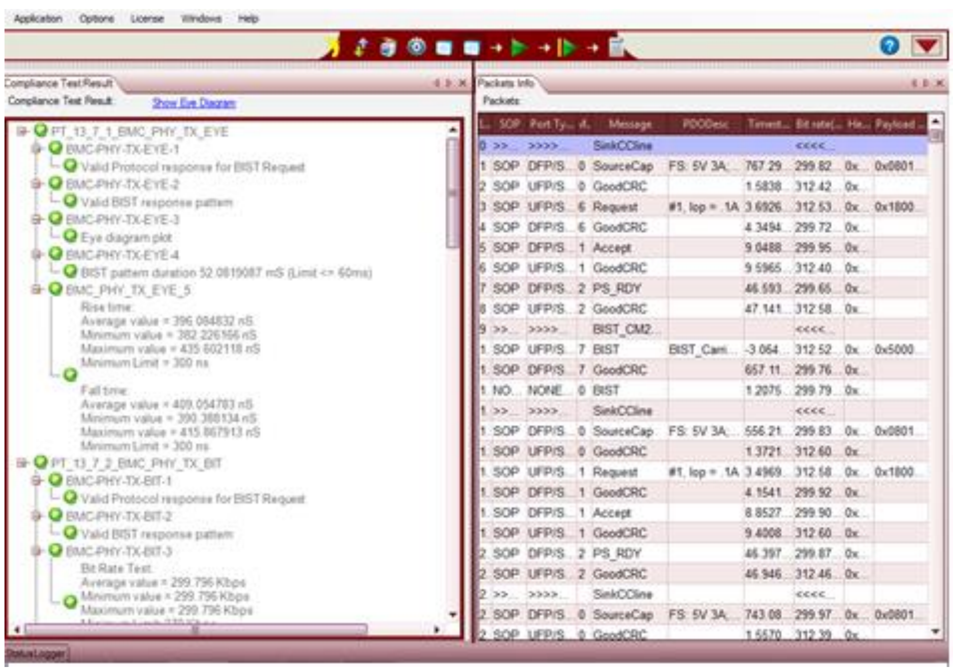


FIGURE 28: TEST RESULTS WINDOW

2) To view the BMC Eye Diagram, click the **Show Eye Diagram** link.

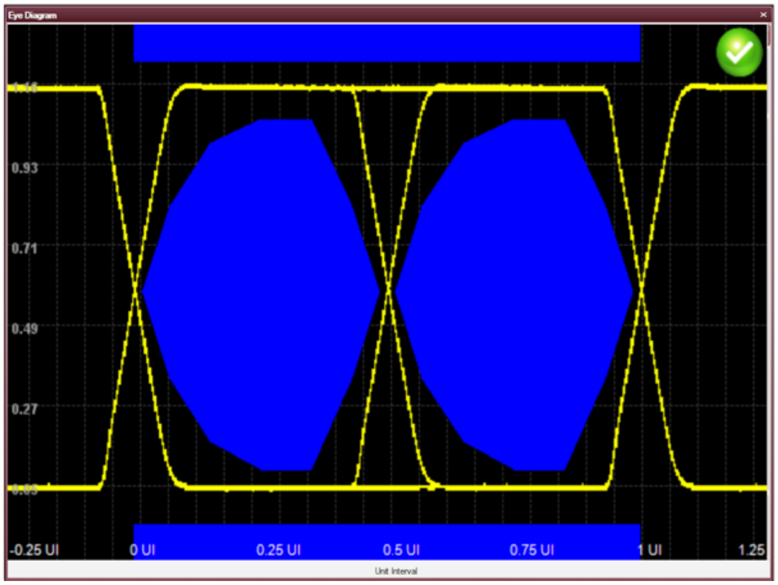


FIGURE 29: VIEWING EYE DIAGRAM

5.10.7 Save and Archive Test Results

1) Go to the **Report Generation** menu to create reports.

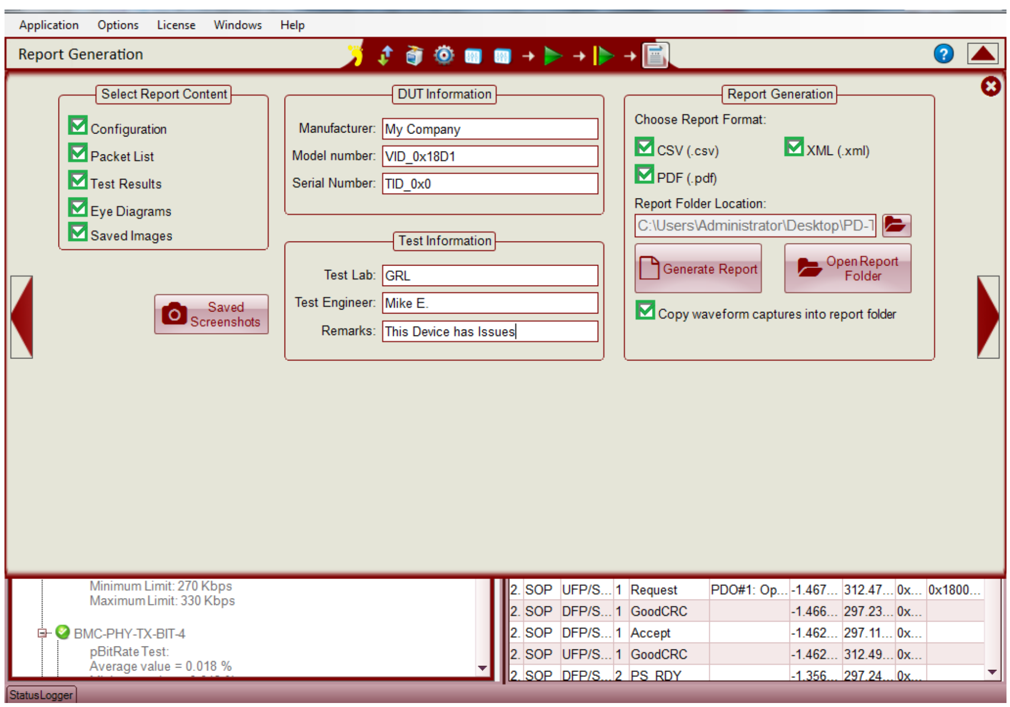


FIGURE 30: REPORT GENERATION MENU

2) Select the desired report content in the **Select Report Content** section.

3) Enter **DUT Information** and **Tester Information** that you would like to appear in the report.

4) Choose the **Report Format** you would like to have created.

5) Choose the **Report Folder Location** where you would like the report and test results to be saved.

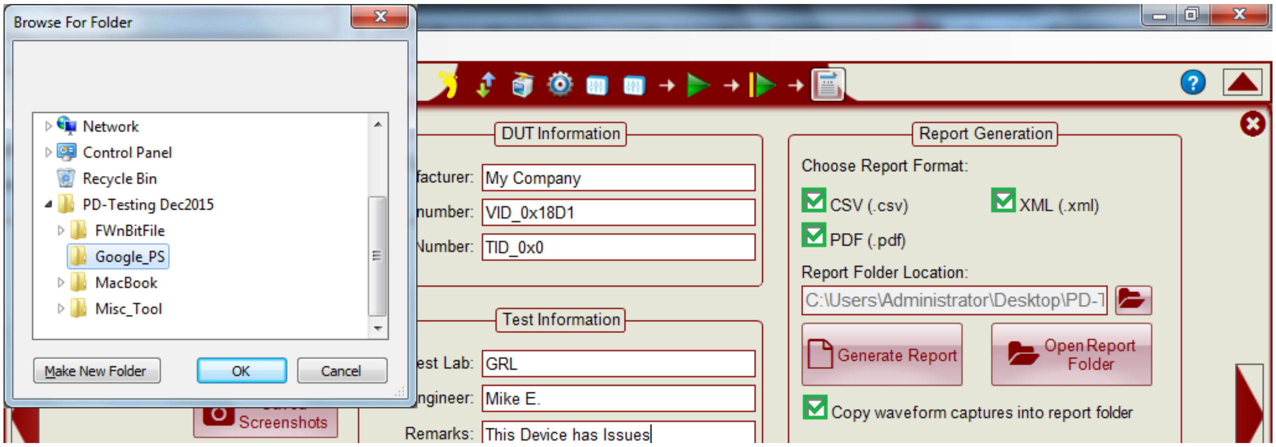


FIGURE 31: SELECT REPORT LOCATION

6) If you would like the waveforms used for testing copied over to the results folder, check the '**Copy waveform captures into report folder**' check box. It is recommended that waveforms be saved for later analysis or debug.

7) Press the **Generate Report** button to create the report.

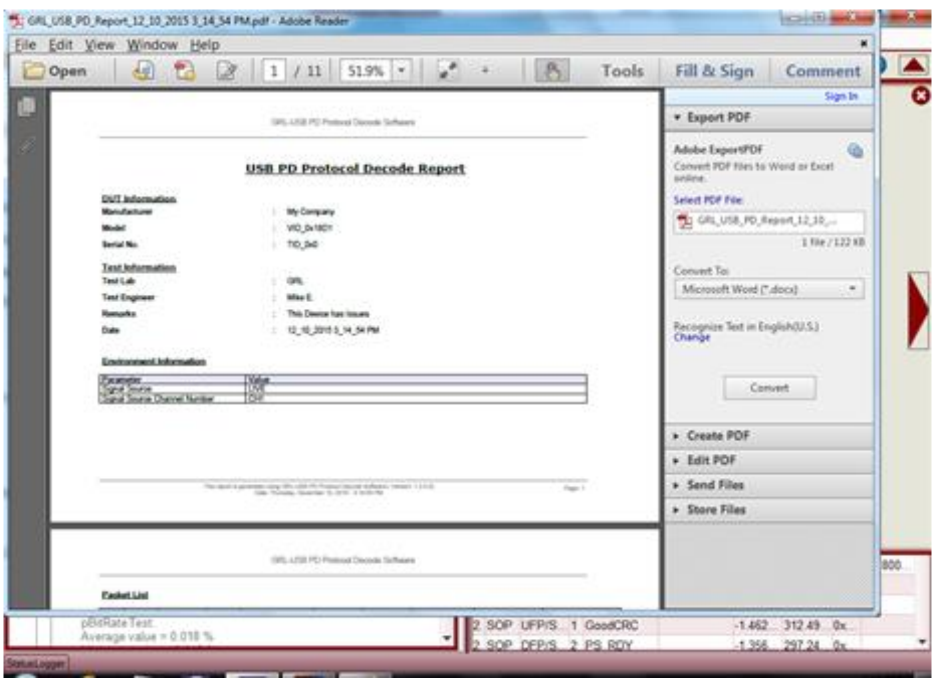


FIGURE 32: GENERATED REPORT

8) A PDF report, .csv, and .xml file will all be created and placed in the results folder.

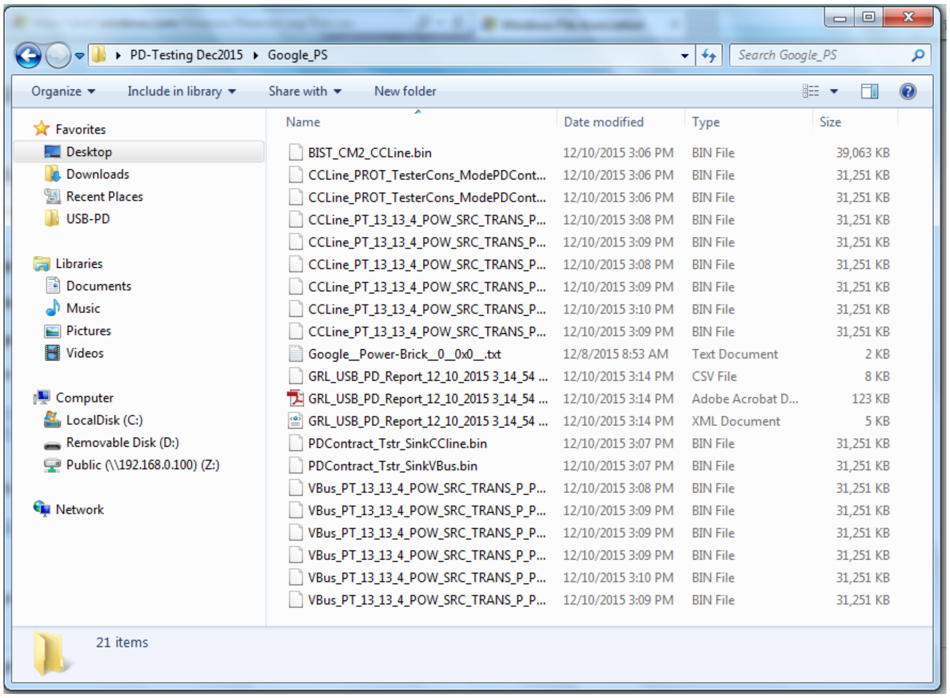


FIGURE 33: REPORT FILE LISTING

6 DisplayPort Over USB Type-C Test Methods

This section describes test methods for decoding DisplayPort over USB Type-C packets as defined in Section 5 (Discovery and USB-PD) of the *DisplayPort Alt Mode on USB Type-C Standard, Ver.1.0a, August 5th, 2015*.

Review Section 10, Appendix B: Using the Configuration Utility, before using the test methods.

6.1 Validating PD Messaging for DisplayPort Alt Mode

6.1.1 Test Setup for Validating PD Messaging for DisplayPort Alt Mode

This section describes how to validate the DP Messaging for DisplayPort Alt Mode. The test setup uses the GRL-USB-PD-C1 Controller as a Link Partner for DisplayPort Alt Mode negotiation. If the DUT is a Source the controller emulates a Sink and if the DUT is a Sink, the controller emulates a DP Source. The common setup is to connect the controller Port-A directly to the DUT using the provided USB Type-C Cable or if the DUT is a tethered DUT, connected directly to Port-A.

1) Connect the DUT to Port-A of the GRL-USB-C1 Controller as follows.

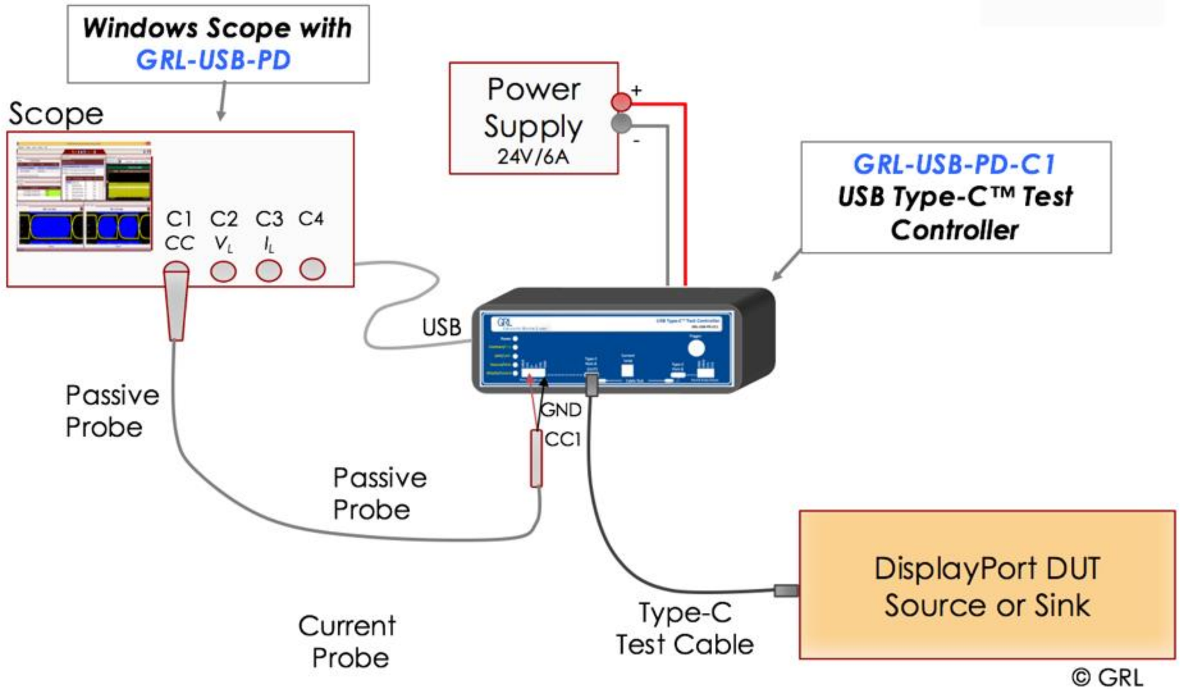


FIGURE 34: CONNECTING THE DUT FOR DISPLAYPORT OVER TYPE-C

2) In the Setup Selection Menu, select Alt Mode as the the type of device.

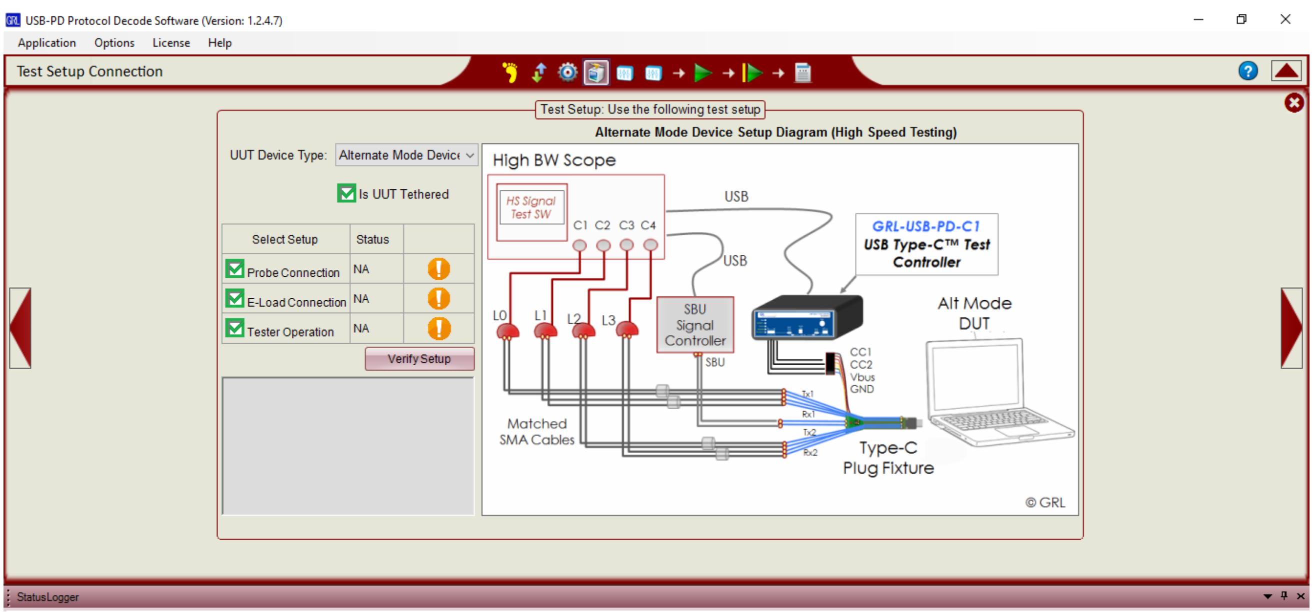


FIGURE 35: SELECTING ALT MODE DEVICE AS DUT

6.1.2 Establishing PD Mode in the DUT

The following test steps refer to details on the Configure Controller window.

Section numbers in the major steps refer to sections in the *DisplayPort Alt Mode on USB Type-C Standard*.

1) If the DUT is a **Source,** then get the DUT into PD Mode.

1. Unplug the DUT from Tester or simulate DUT detach condition by clicking **Simulate Detach**.
2. Set the controller mode to **UFP/Sink** in the **Configure Tab** of the Configure Controller window.
3. Plug-in the DUT if it is not connected to Tester to get the DUT into PD source mode.

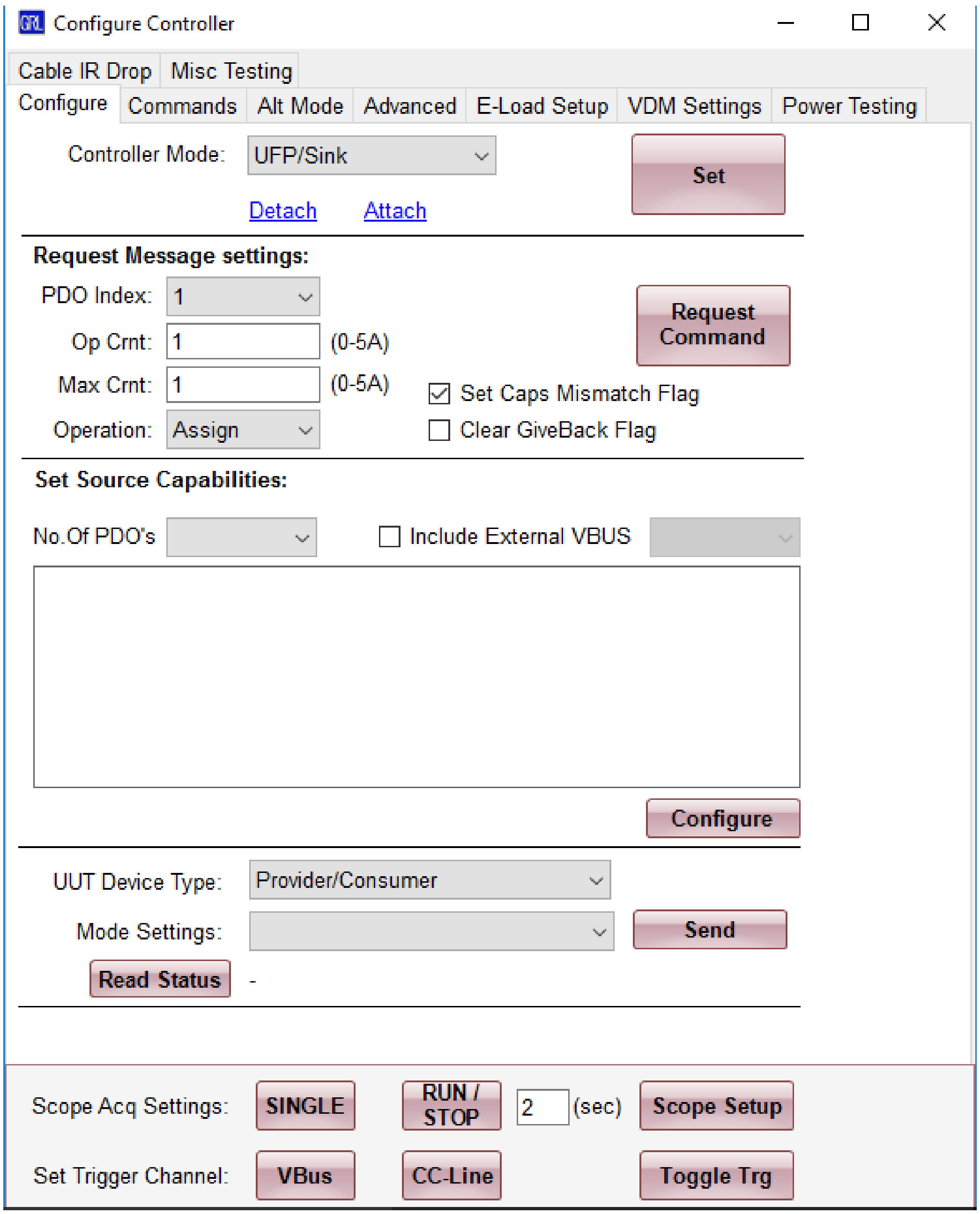


FIGURE 36: CONFIGURE TAB IN CONFIGURE CONTROLLER WINDOW

2) If the device is a **Sink,** then Get the DUT into PD Mode.

1. Unplug the DUT from Tester or simulate DUT detach condition by clicking **Simulate Detach**.
2. Set the controller mode to **DFP/Source** in the **Configure Tab** of the Configure Controller window.
3. Plug-in the DUT if it is not connected to Tester to get the DUT into PD sink mode.

3) Decode and Analyze Protocol Messages:

1. Click on Scope Setup button to load the Scope horizontal and vertical settings to capture PD messages.
2. Click on SINGLE button to enable the Scope acquisition.
3. Set the trigger source to Vbus or CC-Line by clicking the corresponding button shown in Figure 42, to capture PD Contract message sequence. Need to ensure that the "Signal Source Section" of "Decode Configuration" window CC-Line and Vbus is enabled, and selects the channels to which these signals are connected.
4. After selecting trigger channel to Vbus or CC-Line, click **Single** button to wait for the trigger to occur on the Scope.
5. After signal acquisition, click to **Run without Acquisition** button (Green arrow with prefixed yellow line) in the USB-PD Software window.

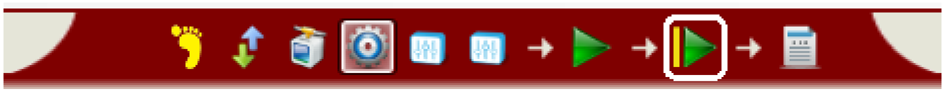


FIGURE 37: RUN BUTTON IN CONFIGURE CONTROLLER WINDOW

6.1.3 Verifying the VDM Header

This section shows detail on decoding the Structured VDM Header for DisplayPort as described in Section 5.2.1 (Table 5-1) of the DisplayPort Alt Mode on USB Type-C specification.

1) Get the DUT into PD **UFP/Sink** mode. If DUT is a Provider Only device, then switch the data role of the DUT to respond Discover Initiator from Tester:

1. Get the DUT into Source mode.
2. Issue Data Role Swap message from **Commands Tab**.

2) Enable oscilloscope acquisition.

3) Select VDM Discover ID Initiator item in the **Commands Tab** and click on **Send** button.

4) Decode and analyze the response message from DUT

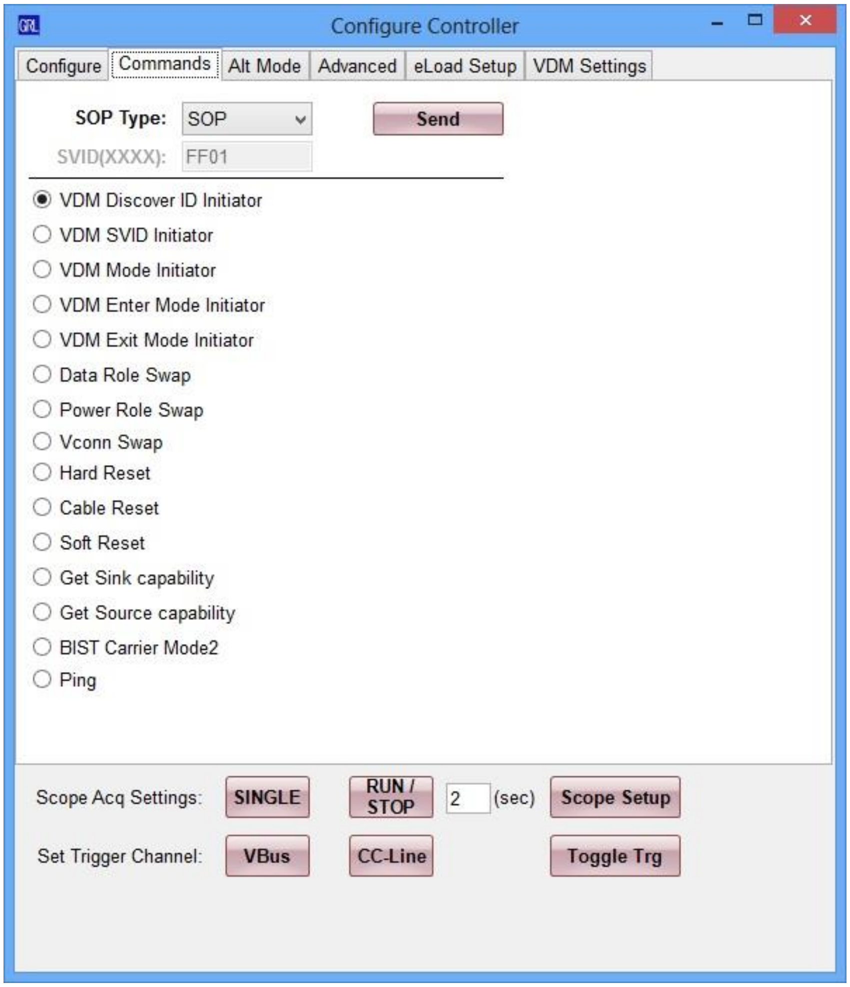


FIGURE 38: COMMANDS TAB IN CONFIGURE CONTROLLER WINDOW

6.1.4 Verifying DisplayPort Enter Mode

This section shows detail on decoding DisplayPort Enter Mode for DisplayPort as described in Section 5.2.2 (Table 5-2) of the DisplayPort Alt Mode on USB Type-C specification.

1) Get the DUT into PD **UFP/Sink** mode. For Provider Only DUT, switch the data role of the DUT:

1. Get the DUT into Source mode.
2. Issue Data Role Swap message from **Commands Tab**.

2) Enable oscilloscope acquisition.

3) Select **VDM Enter Mode Initiator** item in the **Commands Tab** and click on **Send** button.

4) Decode and analyze the response message from DUT.

6.1.5 Verifying DisplayPort Status Update

This section shows detail on decoding the Status Update as described in Section 5.2.3 (Table 5-3) of the DisplayPort Alt Mode on USB Type-C specification.

1) Get the DUT into PD **UFP/Sink** mode. For Provider Only DUT, switch the data role of the DUT:

1. Get the DUT into Source mode.
2. Issue Data role swap message from **Commands** Tab.

2) Enable Scope acquisition.

3) Configure DisplayPort Status Update message in **Alt Mode Tab**.

4) Click on Send Command button.

5) Decode and analyze the response message from DUT.

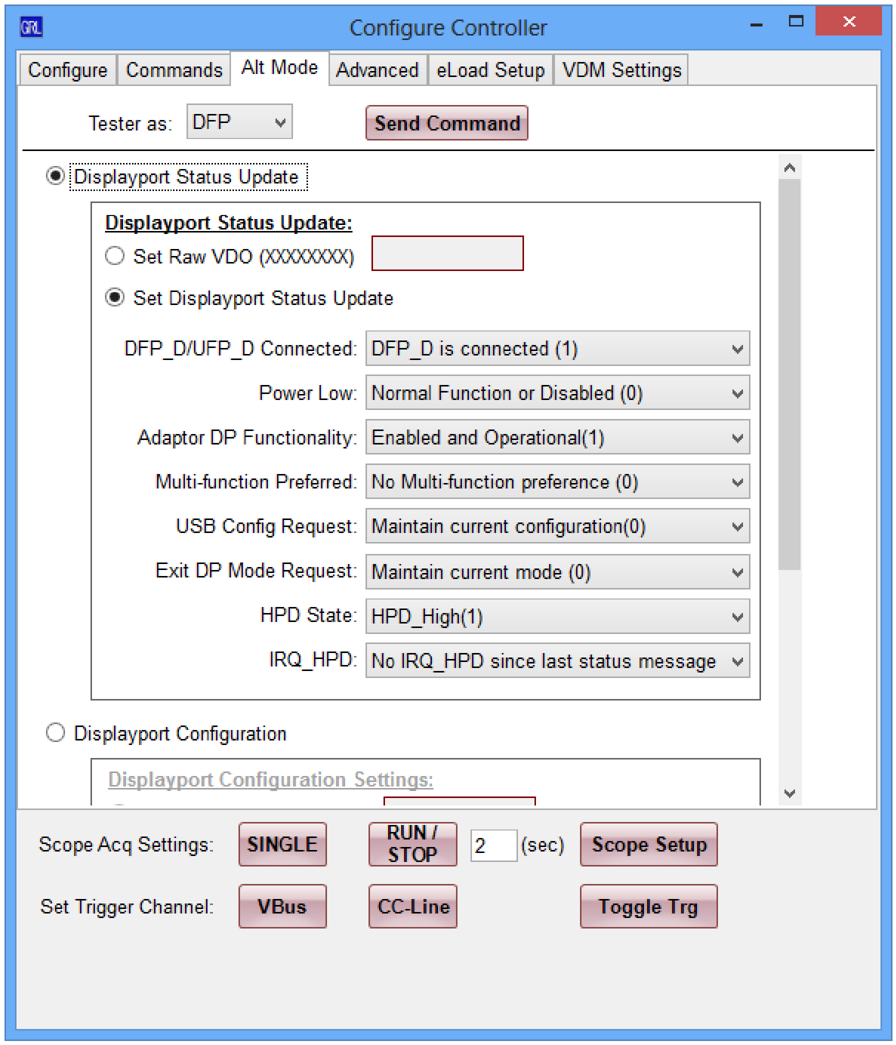


FIGURE 39: ALT MODE TAB IN CONFIGURE CONTROLLER WINDOW – DFP_D

6.1.6 Verifying DisplayPort Configuration

This section shows detail on decoding the DisplayPort Configuration as described in Section 5.2.4 (Table 5-4) of the DisplayPort Alt Mode on USB Type-C specification.

1) Get the DUT into PD **UFP/Sink** mode. For Provider Only DUT, switch the data role of the DUT:

1. Get the DUT into Source mode.
2. Issue Data Role Swap message from **Commands Tab**.

2) Enable Scope acquisition.

3) Configure DisplayPort Configuration message in **Alt Mode Tab.**

4) Click on **Send Command** button.

5) Decode and analyze the response message from DUT.

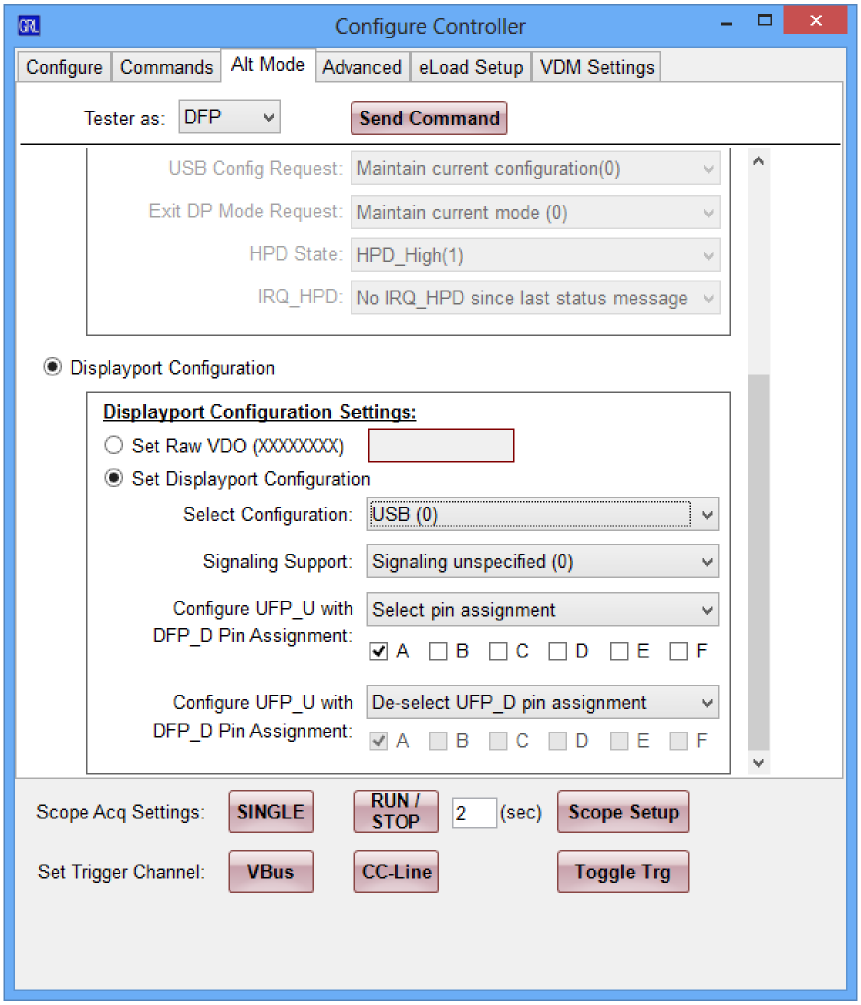


FIGURE 40: ALT MODE TAB IN CONFIGURE CONTROLLER WINDOW – USB(0)

6.1.7 Verifying DisplayPort Attention

This section shows detail on decoding the DisplayPort Attention as described I Section 5.2.5 of the DisplayPort Alt Mode on USB Type-C specification.

1) Get the DUT into PD **UFP/Sink** mode. For Provider Only DUT, switch the data role of the DUT:

1. Get the DUT into Source mode.
2. Issue Data Role Swap message from **Commands Tab**.

2) Enable Scope acquisition.

3) Configure DisplayPort Status Update section in **Alt Mode Tab** and click on **Send Run-time Attention Message**.
4) Decode and analyze the message from DUT.

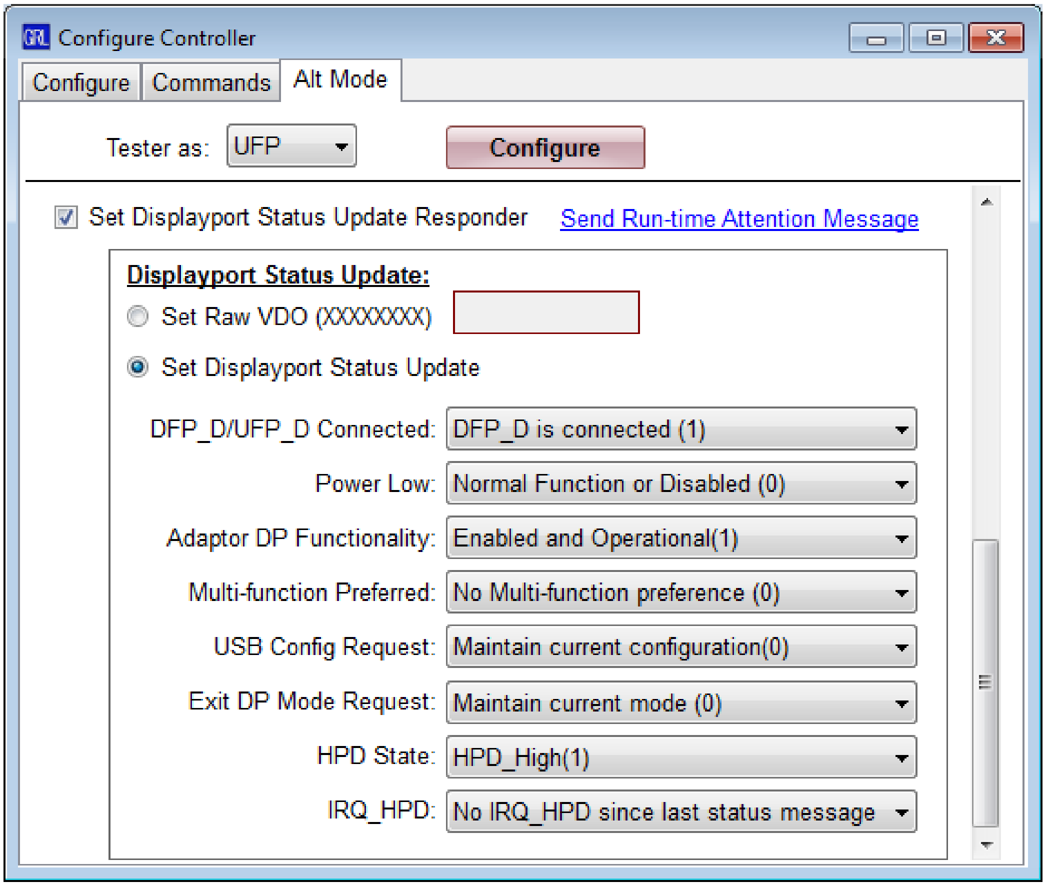


FIGURE 41: ALT MODE TAB IN CONFIGURE CONTROLLER WINDOW – RUN-TIME ATTN

6.1.8 Verifying Exit Mode

This section shows detail on decoding the DisplayPort Exit Mode as described in Section 5.2.6 of the DisplayPort Alt Mode on USB Type-C specification.

1) Get the DUT into PD **UFP/Sink** mode. For Provider Only DUT, first get the DUT into Source mode then issue Data Role Swap message from Commands tab to switch the data role of the DUT to respond Discover Initiator from Tester.
2) Enable Scope acquisition.
3) Select VDM Exit Mode Initiator item in the **Commands Tab** and click on **Send** button.
4) Decode and analyze the response message from DUT.

6.2 DisplayPort on Type-C DP 1.2b PHY Source Testing

The DP over Type-C PHY CTS from VESA requires testing of DisplayPort Source and Sink Signal Quality over the USB Type-C Connector. For devices that support 2 lanes of DisplayPort and USB3.1 Gen1/Gen2 Tx/Rx on the other two signal pairs (known as 2+2 Mode), crosstalk must be tested. Also if the device is a Power Provider, the DisplayPort PHY signaling needs to be compliant under maximum power conditions. This section describes how to use the GRL-USB-PD-C1 Controller manually to achieve these PHY test modes on a device with DisplayPort over USB-C. The PHY testing itself is done using existing DisplayPort 1.2b PHY test solutions.

6.2.1 4 Lane DisplayPort PHY testing on USB Type-C

6.2.1.1 Test setup for 4 Lane DisplayPort PHY testing on USB Type-C

Following test setup required for DisplayPort over Type C testing:

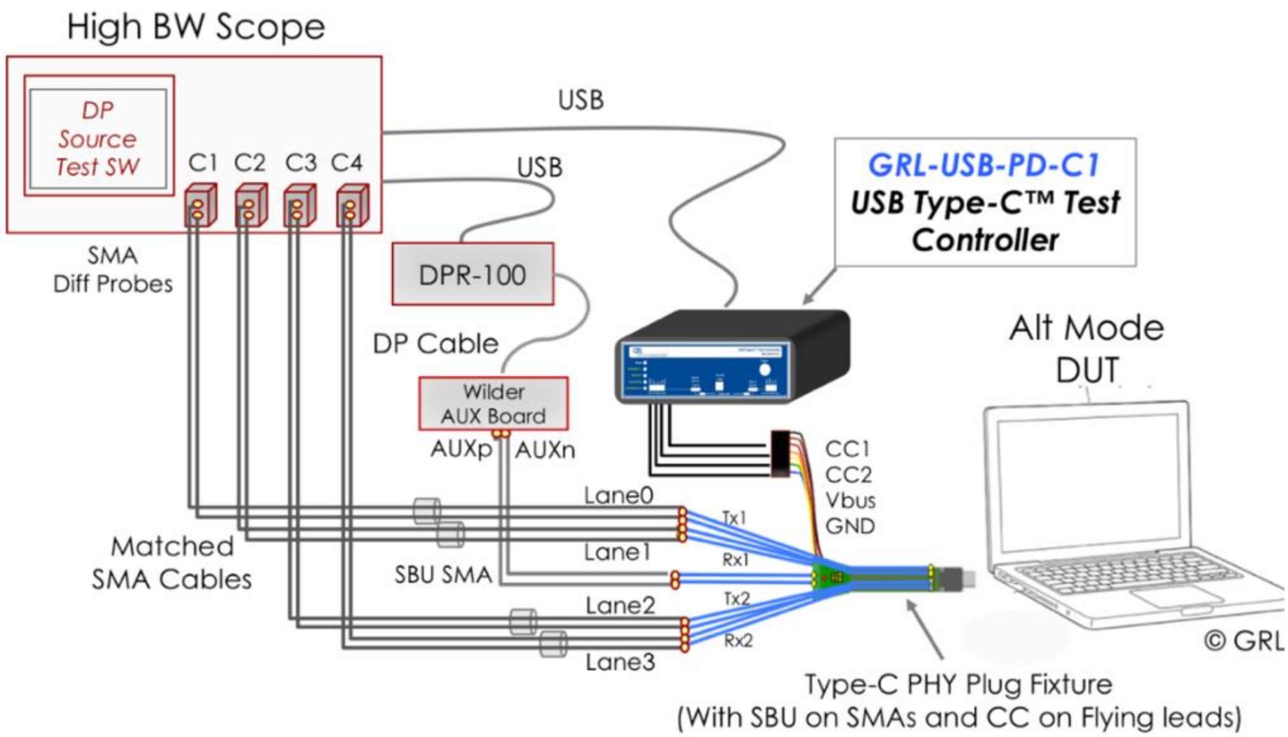


FIGURE 42: DISPLAYPORT PHY TEST SETUP 4 LANE MODE

Note: the PHY test fixture used in this example has the SBU lines broken out into SMAs. Thus, the AUXp and AUXn lines are fed directly from the AUX controller to the test fixture SBU lines. The AUX/SBU connection to the controller is fixture manufacturer dependent. The GRL-USB-PD-C1 is designed to work with multiple vendor's USB Type-C test fixtures and connection method may vary.

Follow below mentioned steps to make the connection setup that shown in Figure 42:

1) Connect Type-C CC line communication signals from the GRL-USB-PD-C1 to DUT with the help of "Probe EXT-1" and "Type-C cable extender" and which in turn must be connected to CC1, CC2, Vbus and Ground of "Type-C PHY Plug Fixture".
2) Connect Main Link signals from "Type-C PHY Plug Fixture" to the Scope using differential probe.

3) SBU1 & SBU2 (A8 & B8) signals from “Type-C PHY Plug Fixture” to Wilder AUX Board.
4) Optional: CC line communication between DUT and GRL-USB-PD-C1 can be monitored by probing CC1 & Vbus on “Probe EXT-1” (not shown in Figure 42).
5) Using DisplayPort cable connects Wilder Fixture and DPR-100, to update DisplayPort DPCD register.

6.2.1.2 Initiating Alt Mode for DisplayPort 4 Lane PHY Testing

1) Create the test setup as shown in Figure 42.
2) Unplug the DUT from the test setup by removing “Type-C PHY Plug Fixture”.
3) Open the GRL-USB-PD application and navigate to Configure Controller, as in Figure 43.

Follow the step by step process to initiate Alt Mode Setting for Display Port.

1. Select Configure Tab. Select Controller Mode as UFP/Sink. Select “Enable VDM” as Mode Settings and click **Send** button to set the configuration in the Tester.

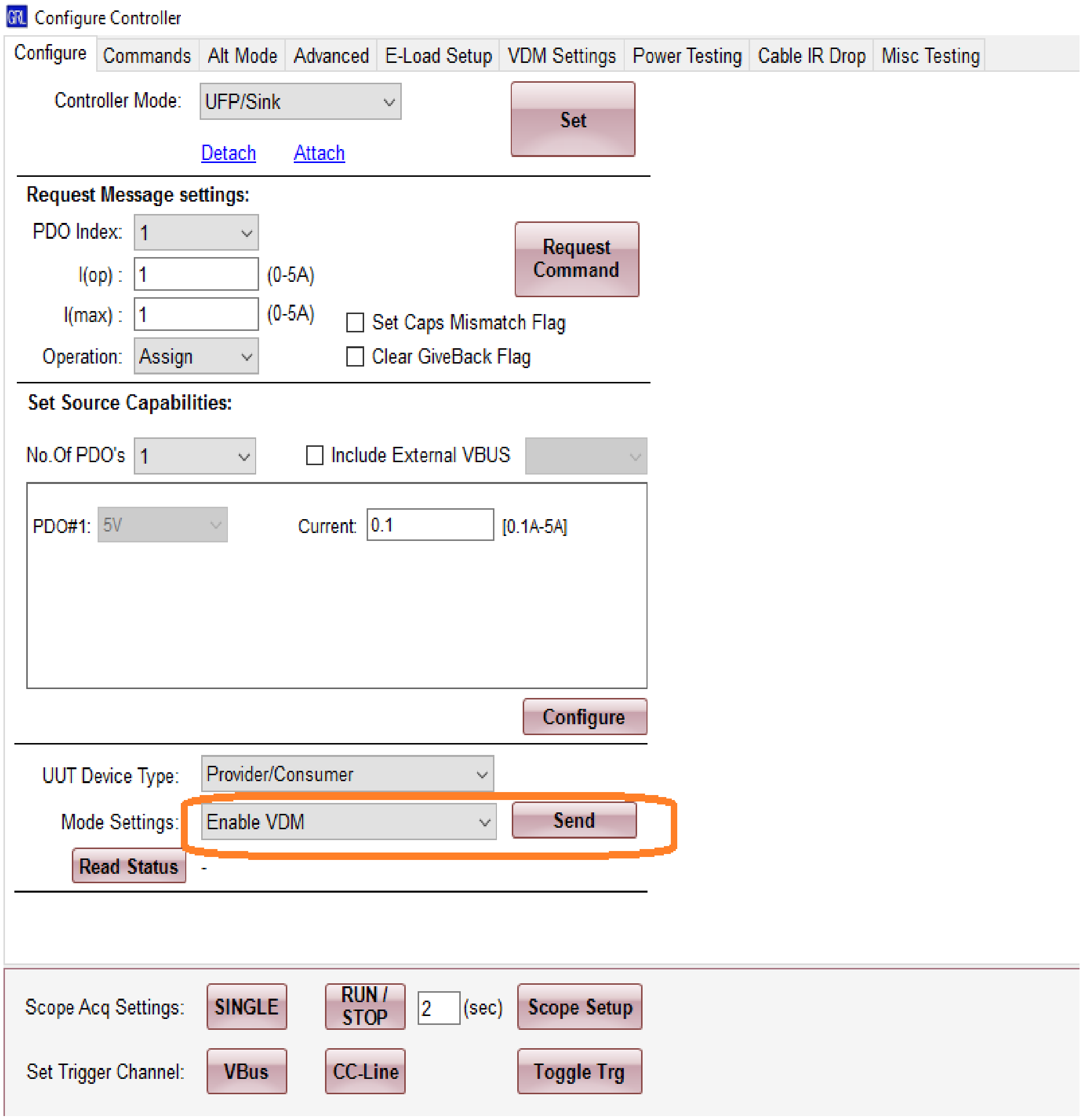


FIGURE 43: CONFIGURE – ENABLE VDM SETTING

2. To set tester in VDM Source Configuration select VDMConfig_TesterSink_ACK in the Mode Settings of the Configure tab, and click **Send** button to set the configuration in the Tester. See Figure 44.

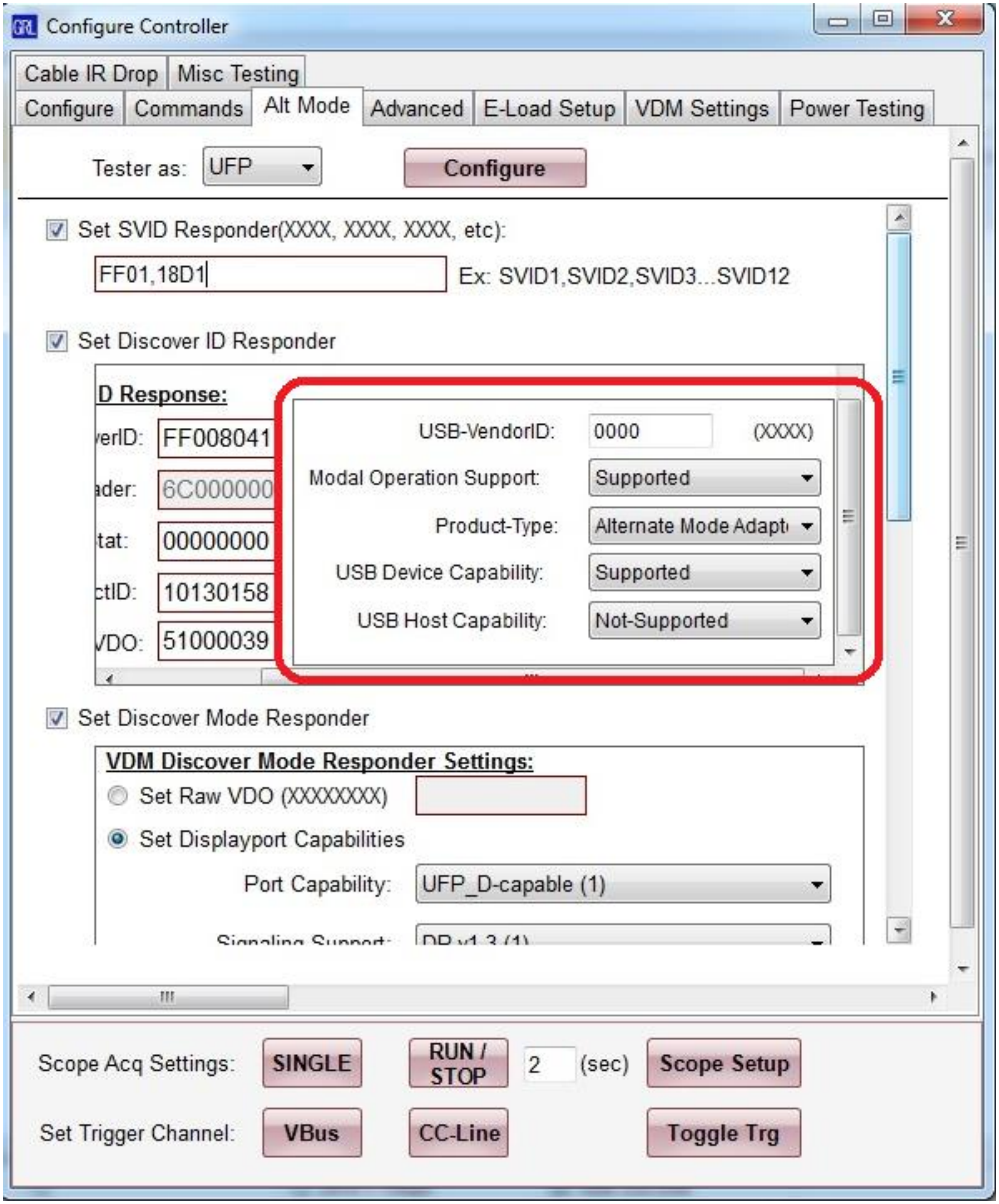
*

FIGURE 44: CONFIGURE – SET VDMCONFIG_TESTERSINK_ACK

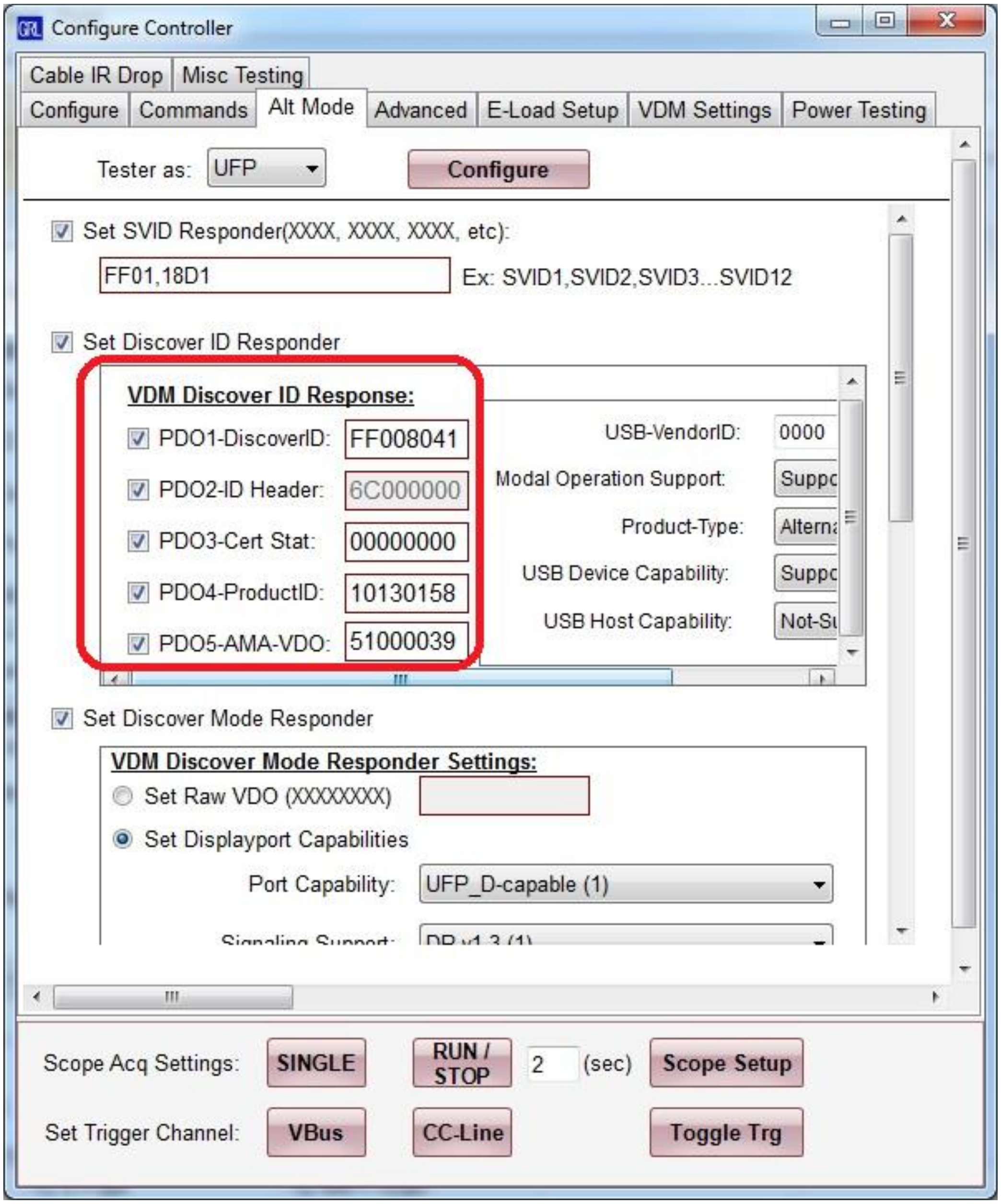
4) Select Alt Mode Tab from Config Controller.

i) Check "Set SVID Responder" check box. Input hexadecimal values for bcdDevice (0158) and USB Product ID (1013) in the Product VDO field for enumerating for USB 3.0 or 2.0

Set USB Vendor ID in the PDO2-ID Header LSB bytes to 05AC as shown in


Configure Controller
Cable IR Drop
Misc Testing
Configure
Commands
Alt Mode
Advanced
E-Load Setup
VDM Settings
Power Testing
Tester as:
UFP
Configure
Set SVID Responder(XXXX, XXXX, XXXX, etc):
FF01,18D1
Ex: SVID1,SVID2,SVID3...SVID12
Set Discover ID Responder
D Response:
FF008041
6C000000
00000000
10130158
51000039
USB-VendorID:
0000
(XXXX)
Modal Operation Support:
Supported
Product-Type:
Alternate Mode Adapt
USB Device Capability:
Supported
USB Host Capability:
Not-Supported
Set Discover Mode Responder
VDM Discover Mode Responder Settings:
Set Raw VDO (XXXXXXXX)
Set Displayport Capabilities
Port Capability:
UFP_D-capable (1)
Scope Acq Settings:
SINGLE
RUN / STOP
2
(sec)
Scope Setup
Set Trigger Channel:
VBus
CC-Line
Toggle Trg

ii) Figure 45.


Configure Controller
Cable IR Drop
Misc Testing
Configure
Commands
Alt Mode
Advanced
E-Load Setup
VDM Settings
Power Testing
Tester as:
UFP
Configure
Set SVID Responder(XXXX, XXXX, XXXX, etc):
FF01,18D1
Ex: SVID1,SVID2,SVID3...SVID12
Set Discover ID Responder
VDM Discover ID Response:
PDO1-DiscoverID:
FF008041
PDO2-ID Header:
6C000000
PDO3-Cert Stat:
00000000
PDO4-ProductID:
10130158
PDO5-AMA-VDO:
51000039
USB-VendorID:
0000
Modal Operation Support:
Product-Type:
USB Device Capability:
USB Host Capability:
Set Discover Mode Responder
VDM Discover Mode Responder Settings:
Set Raw VDO (XXXXXXXX)
Set Displayport Capabilities
Port Capability:
UFP_D-capable (1)
Scope Acq Settings:
SINGLE
RUN / STOP
2
(sec)
Scope Setup
Set Trigger Channel:
VBus
CC-Line
Toggle Trg

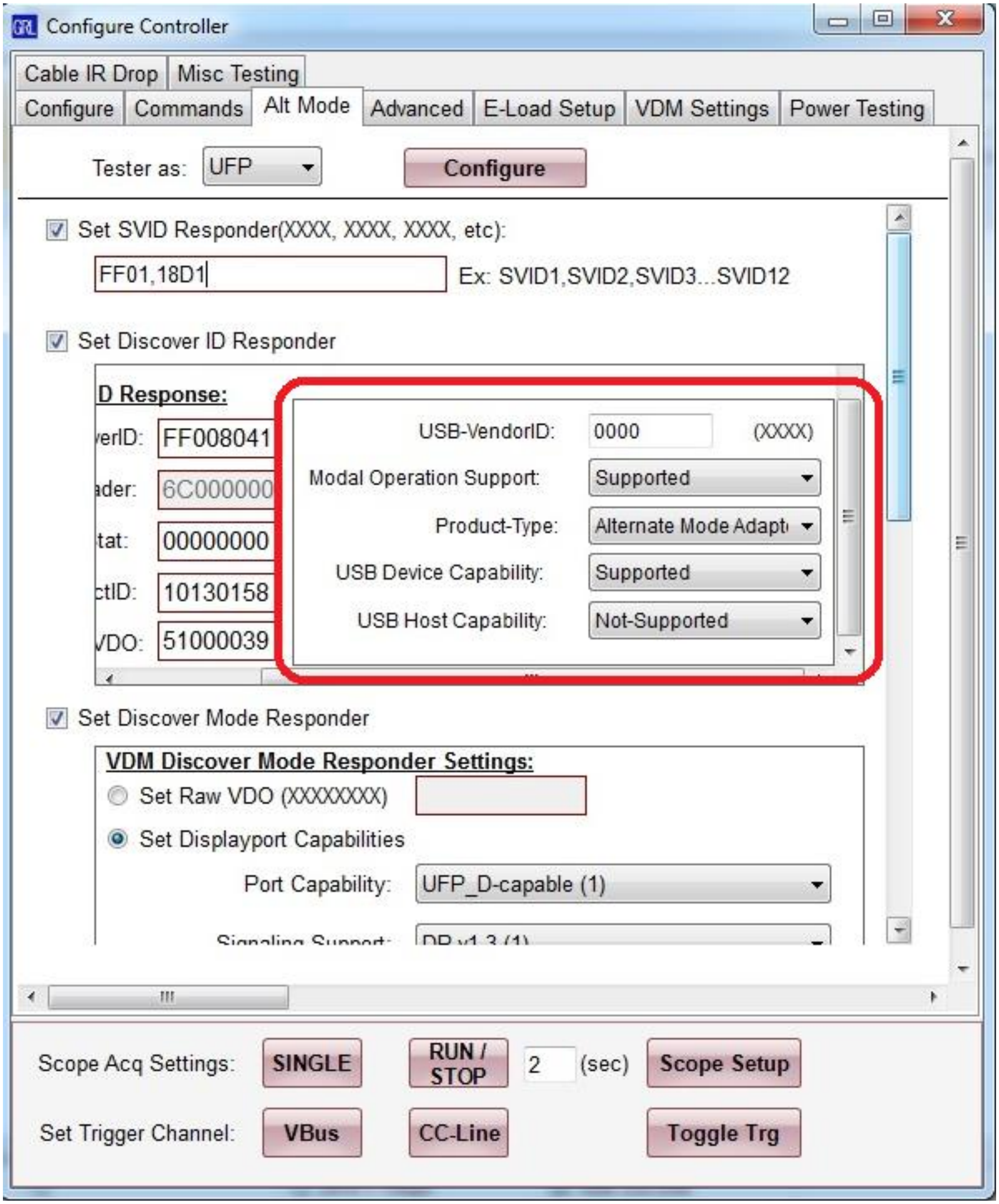


Figure 45: Alt Mode - Set Discover SVID Responder Configuration

iii) Enter the SVID's in the format "FF01, 18D1". Up to 12 SVID's can be set. An example is shown in Figure 46.

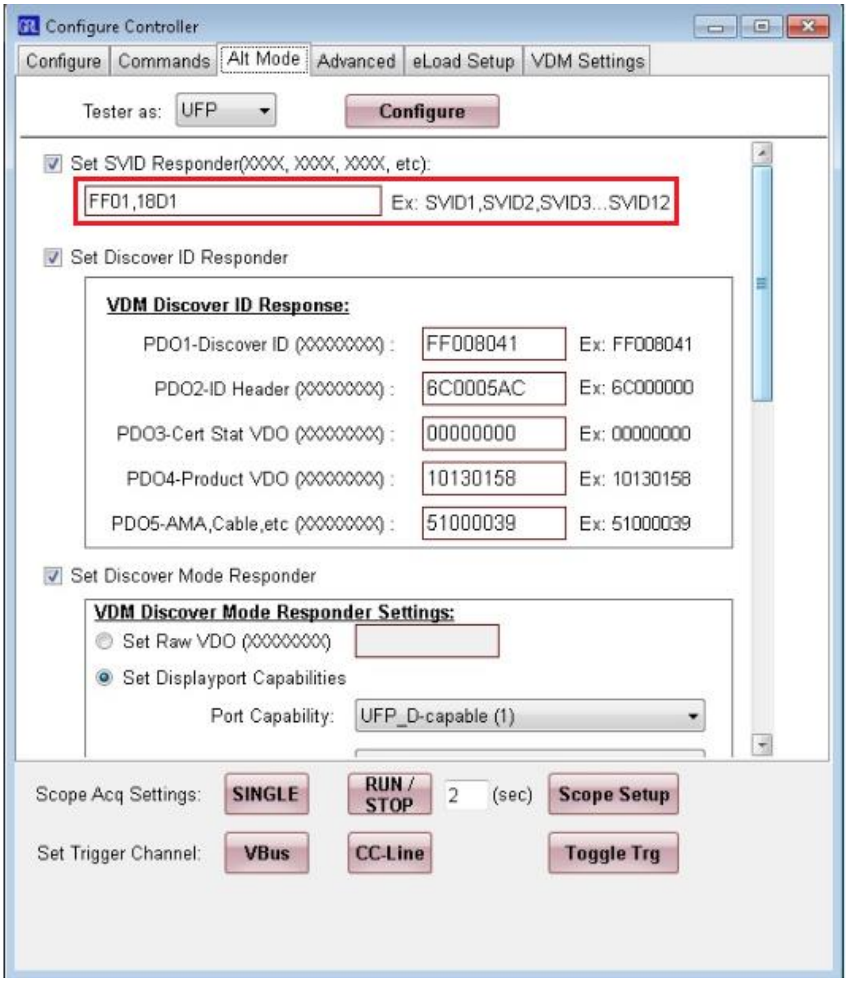


FIGURE 46: ALT MODE - SET SVID'S RESPONDER

iv) Set signaling support to **DP v1.3** in **DisplayPort Capabilities** section, for configuring the controller as Sink, shown in Figure 47.

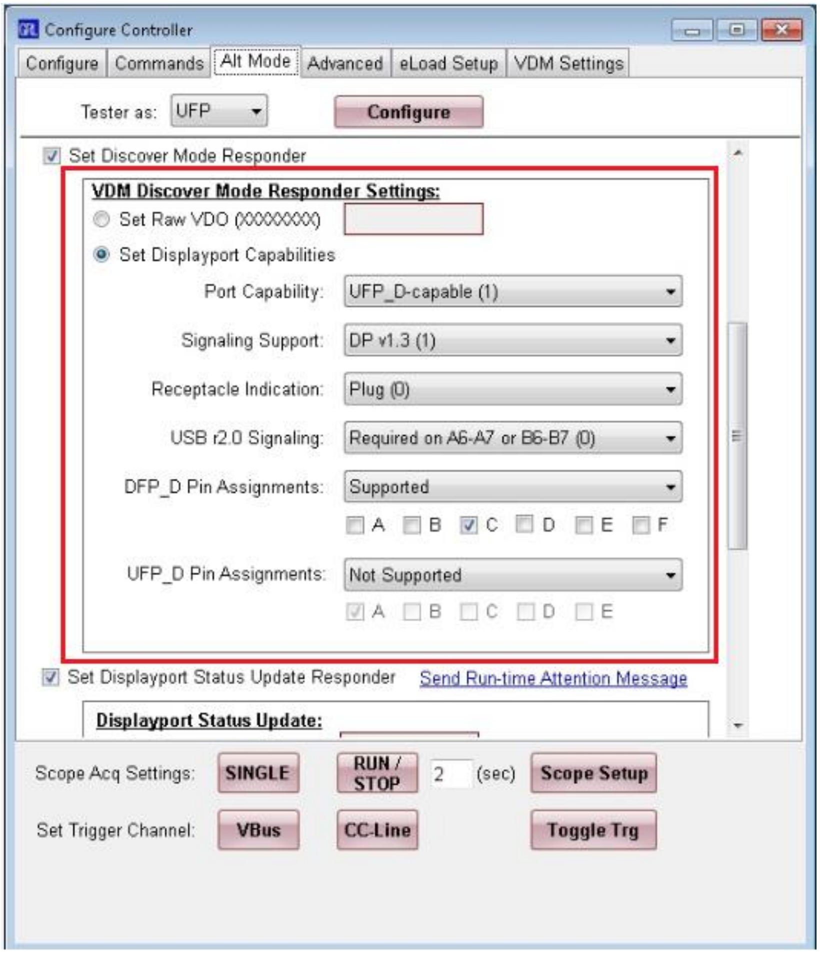


FIGURE 47: ALT MODE - SET DISCOVER MODE RESPONDER

*Note: Select the **Pin Assignments** based on the connected Sink device. Refer to "Pin Assignment and Description" section of the DP Alt Mode on Type-C specification for configuration.*

v) Enable oscilloscope acquisition if required to monitor CC line communication between GRL-USB-PD-C1 and DUT connected.

6.2.1.3 Performing Display Port 4 Lane DP 1.2b Source PHY Testing

After performing the above procedure for Alt Mode Initiation, the DUT is prepared to receive commands from the AUX Controller. To perform the test, the timing of HPD/IRQ must be managed by the host PC that is controlling the Unigraf AUX Controller and the GRL-USB-PD-C1 PD Controller. GRL has developed a software utility called *GRL AUX Config Tool* (described in the next section) to configure the DUT in the proper test mode. To test the Source using the Test Equipment (TE) vendor specific software:

1) Configure DisplayPort AUX controller (DPR-100) based on the DUT capability as mentioned to start the DisplayPort PHY testing.
2) Select 'Manual' test mode in the *TE vendor specific PHY test software*.
3) Run the test script from the *TE vendor specific PHY test software*.

4) When the *TE vendor specific PHY test software* prompts the user for Data Rate, Pattern, Swing, and pre-emphasis setting, use the *GRL AUX Config Tool* to send the proper test signal.
5) Press 'OK' to continue testing using the *TE vendor specific PHY test software*.

Note: This procedure describes the way to manually execute the PHY testing. This is a very time consuming method for testing. Thus, GRL has provided a DLL version of the GRL AUX Config Tool to the major TE vendors to be integrated into their automation tools. Please consult with your TE vendor of choice for details on integration timelines.

6.2.2 2+2 Lane DisplayPort PHY testing on USB Type-C

6.2.2.1 DisplayPort 2+2 lane Test Setup

For testing the DUT in 2+2 mode, where 2 lanes are used for sending DisplayPort signal and remaining 2 lanes are used for USB3.1 communication.

The setup required for testing the DUT with the 2+2 mode is shown in Figure 48.

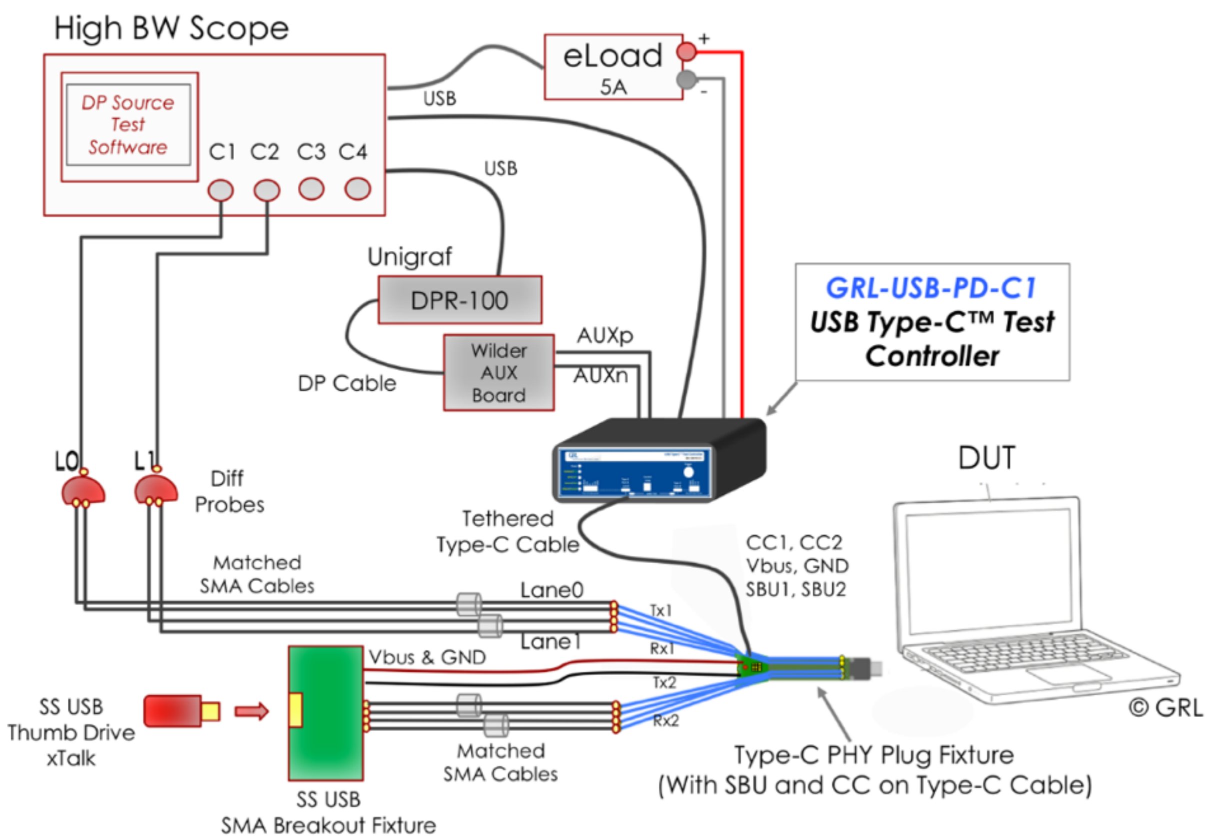


FIGURE 48: DISPLAY PORT PHY TEST SETUP 2+2 LANE MODE

Note: the PHY test fixture used in this example has the SBU lines embedded in a USB Type-C Cable that attaches directly to the controller. Thus, the AUXp and AUXn lines are fed into the SBU1 and SBU2 input connectors on the back of the controller. SBU1 and SBU2 lines are presented to the test fixture through the Type-C tethered cable. The AUX/SBU connection to the controller is fixture manufacturer dependent The GRL-USB-PD-C1 is designed to work with multiple vendors' USB Type-C test fixtures and connection method may vary.

1) Two lanes of Main link (ML0 & ML1) must be connected to SS USB Breakout Board. Ensure that the USB 3.0 device is connected from RX1 / ML1 of the Type-C fixture connected to SSTX+ & SSTX-, and then connect TX1 / ML0 of the Type-C fixture to SSRX+ & SSRX- on the SS USB Breakout fixture.
2) Only two signals of Main Link (ML2 & ML3) from "Type-C PHY Plug Fixture" must be connected to the Scope using differential probe.
3) SBU1 & SBU2 (A8 & B8) signals from "Type-C PHY Plug Fixture" to Wilder AUX Board.
4) Using DP cable, connect Wilder Fixture and DPR-100 to update DisplayPort DPCD register automatically while performing test. Connect USB cable between DPR-100 and Scope where the DPR-100 software is installed.
5) Optional: CC line communication between DUT and GRL-USB-PD-C1 can be monitored by probing CC1 & Vbus on "Probe EXT-1" (not shown in Figure 48).

6.2.2.2 Initiating Alt Mode for DisplayPort 2+2 Lane PHY Testing

1) Create the test setup as shown in the previous section.
2) Unplug the DUT from the test setup by removing "Type-C PHY Plug Fixture".
3) Open the GRL-USB-PD application and navigate to configure controller.

1. Set "Enable VDM" in the Mode Settings of the Configure tab, and click **Send** button to set the configuration in the Tester, as shown in Figure 49.

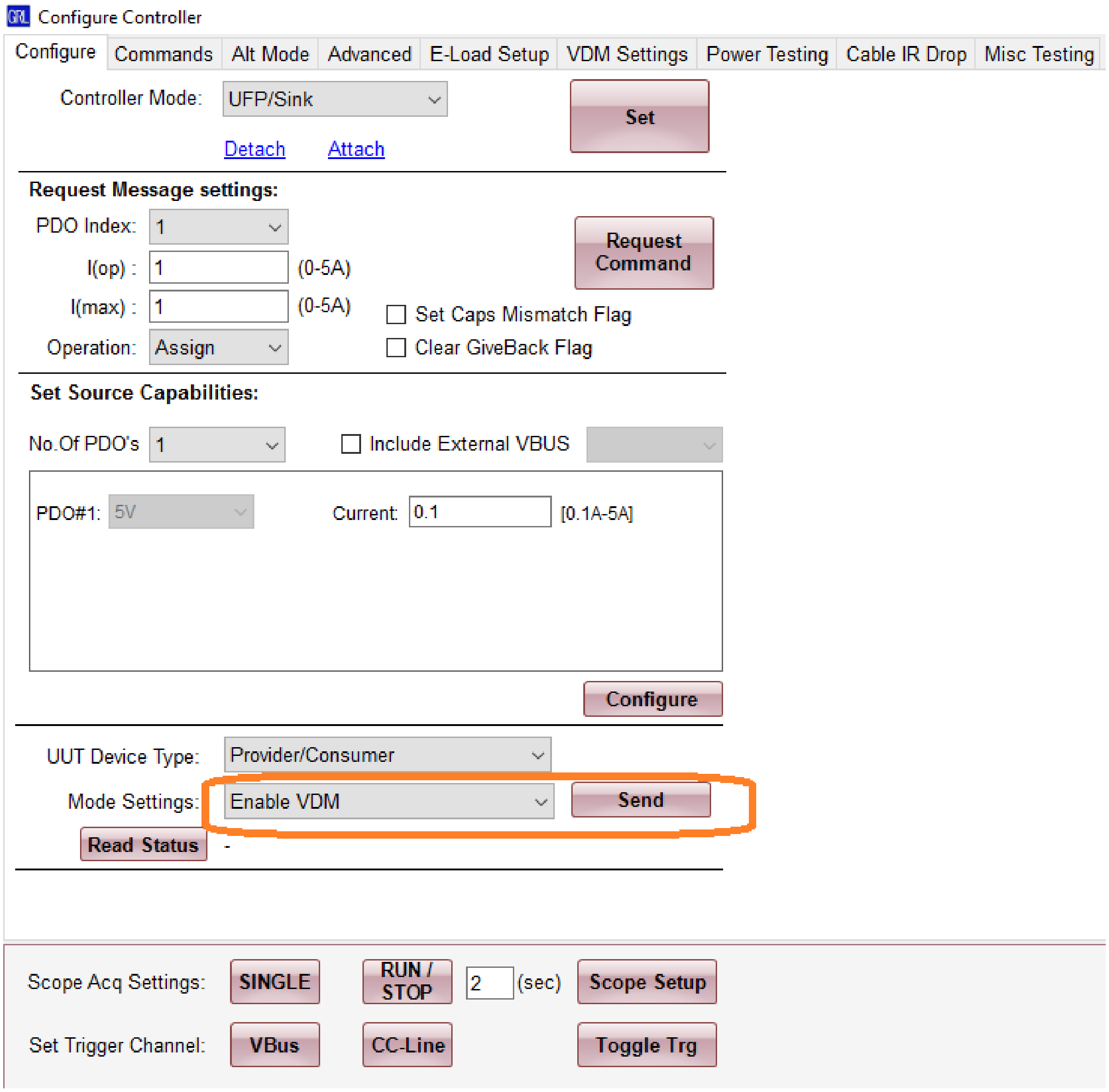


FIGURE 49: CONFIGURE – ENABLE VDM SETTING

2. To set tester in VDM Source Configuration select VDMConfig_TesterSink_ACK in the Mode Settings of the Configure tab, and click **Send** button to set the configuration in the Tester, as shown in Figure 50.

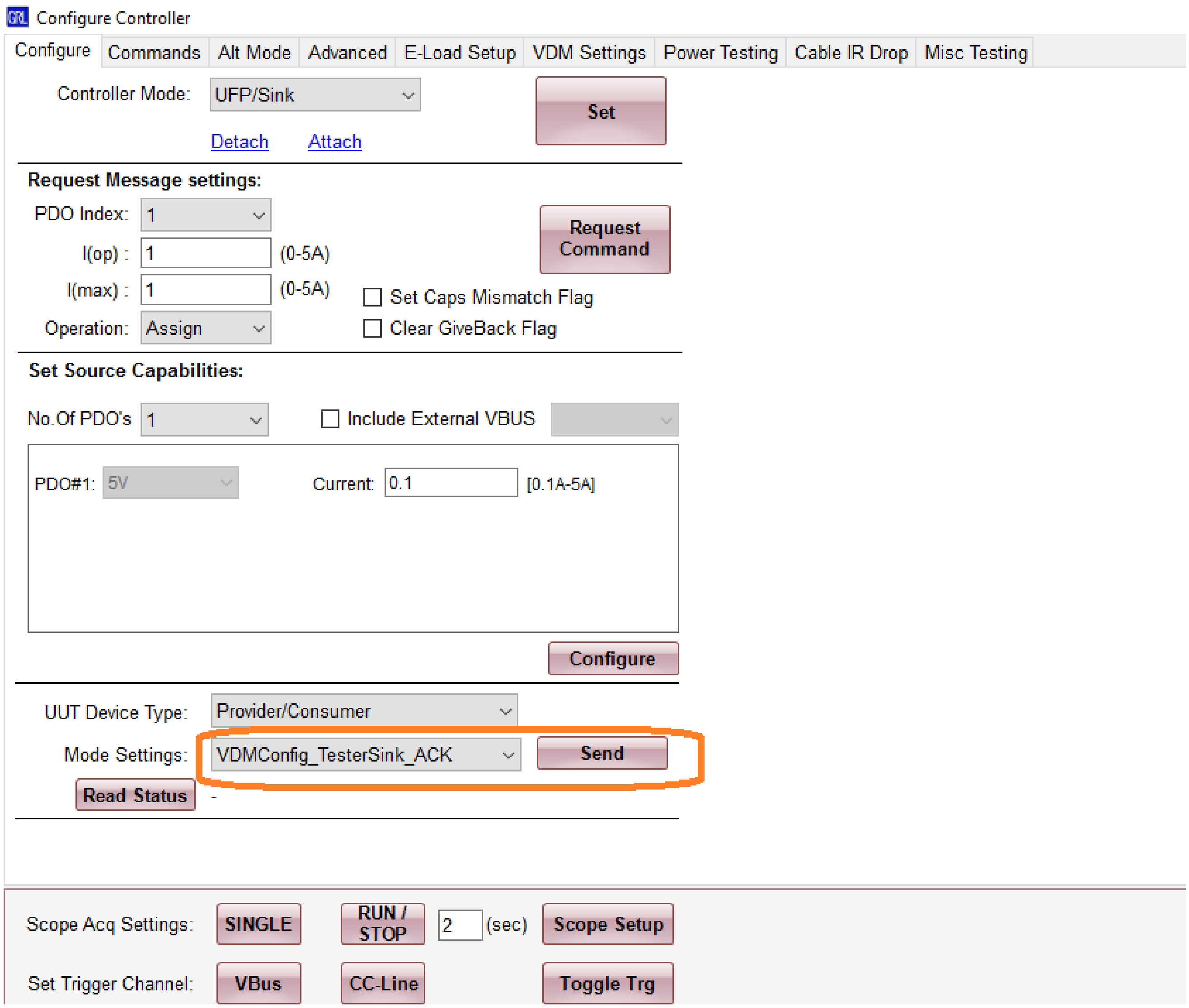


FIGURE 50: CONFIGURE – SET VDMCONFIG_TESTERSINK_ACK

Select Alt Mode Tab .Configure SVID Responder, Discover Mode Responder, DisplayPort Status Update Responder messages details in Alt Mode Tab to test DisplayPort Source.

3. Discover SVID Responder: Configure Tester SVID acknowledgement:

   i) Set hex value of bcdDevice (0158) and USB Product ID (1013) in the Product VDO field for enumerating for USB 3.0 or 2.0 as shown in Figure 51.

   ii) Set USB Vendor ID in the PDO2-ID Header LSB bytes to 05AC.

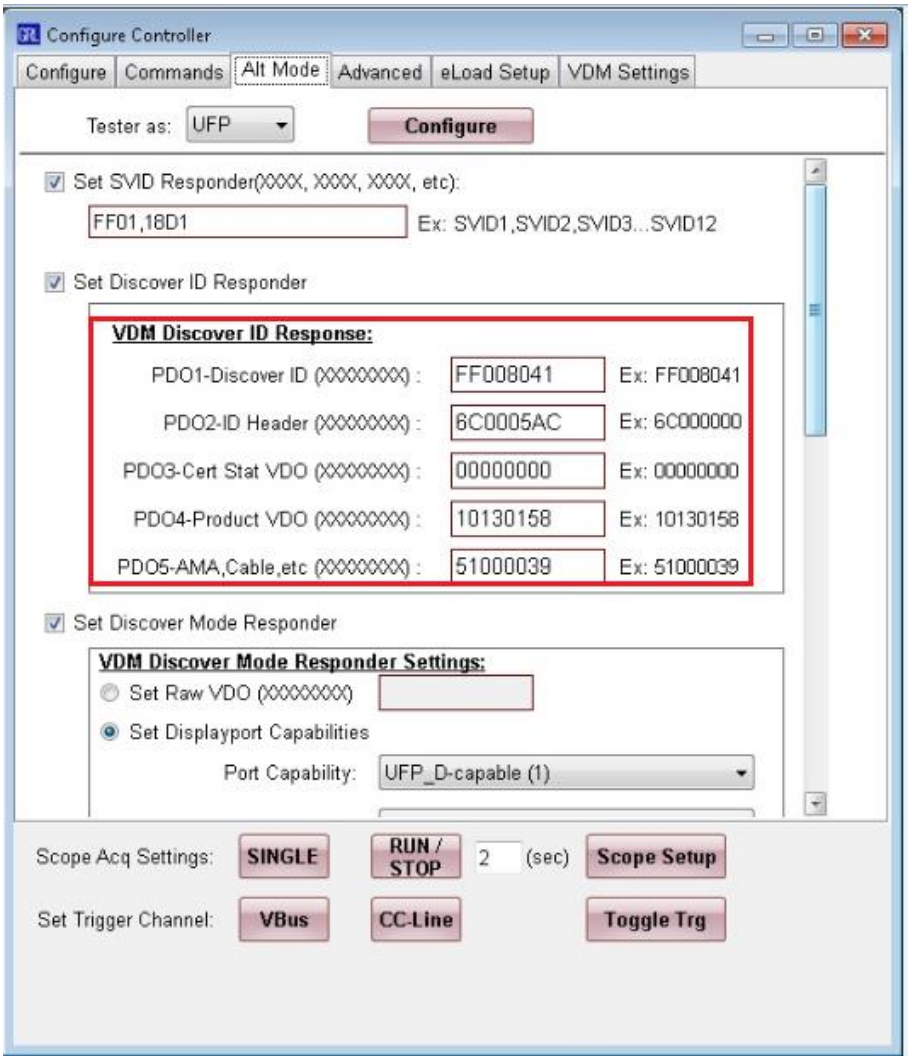


FIGURE 51: ALT MODE – SET DISCOVER SVID RESPONDER CONFIGURATION

4. Set SVID by selecting "SVID Responder" with the SVID's in the format such as "FF01, 18D1", Up to 12 SVID's can be set. An example is shown in Figure 52.

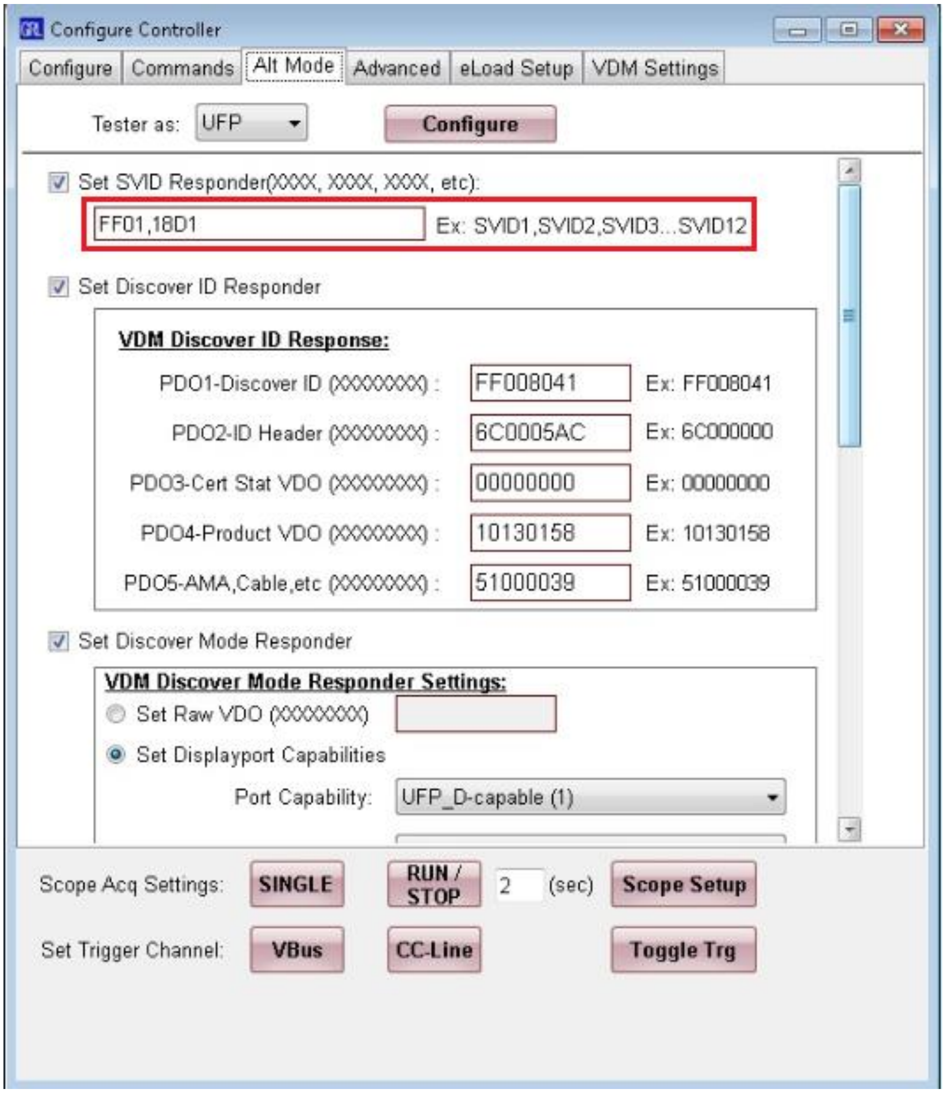


FIGURE 52: ALT MODE – SET SVIDS

5. Select signaling support to **DP v1.3** in **DisplayPort Capabilities** section, for configuring the controller as sink, as shown in Figure 53.

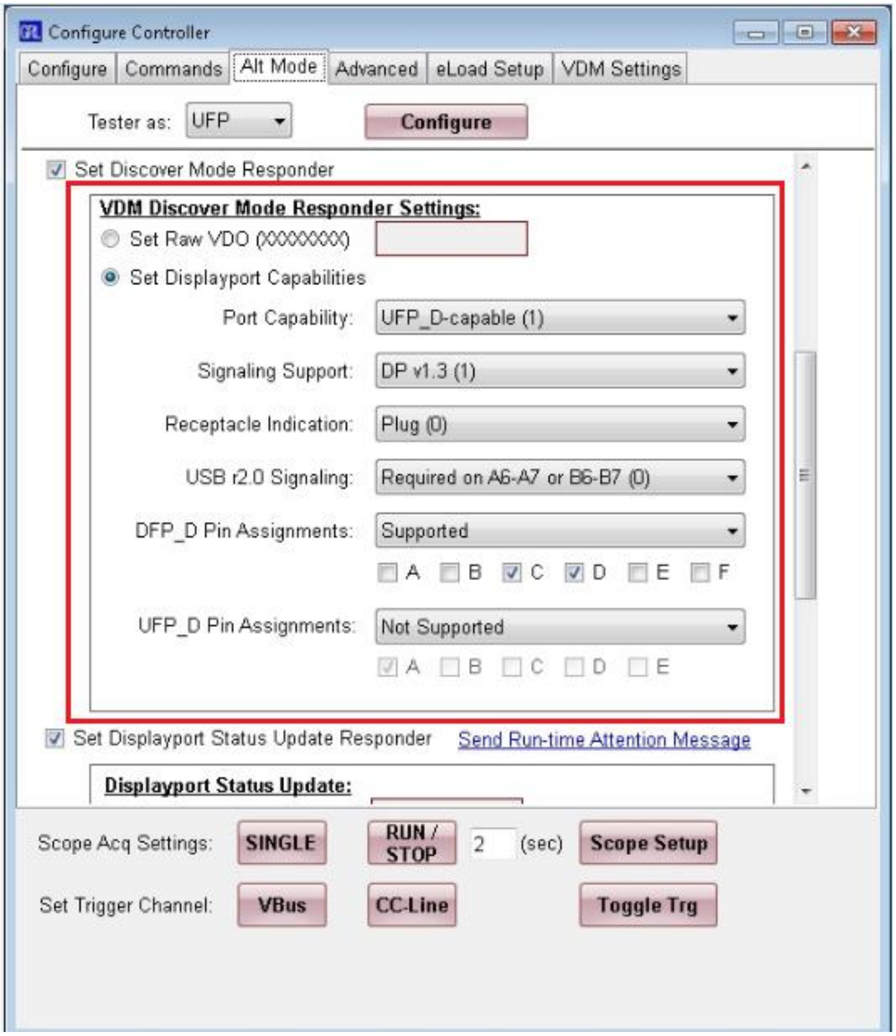


FIGURE 53: ALT MODE – SET DISCOVER MODE RESPONDER

*Note: Select the **Pin Assignments** based on the connected Sink device. Refer "Pin Assignment and Description" section of the DP Alt Mode on Type-C specification for configuration.*

6. Send Status message with the configuration as shown in Figure 54. Status message is used for sending attention message whenever there is a change in the Aux signaling to take effect.

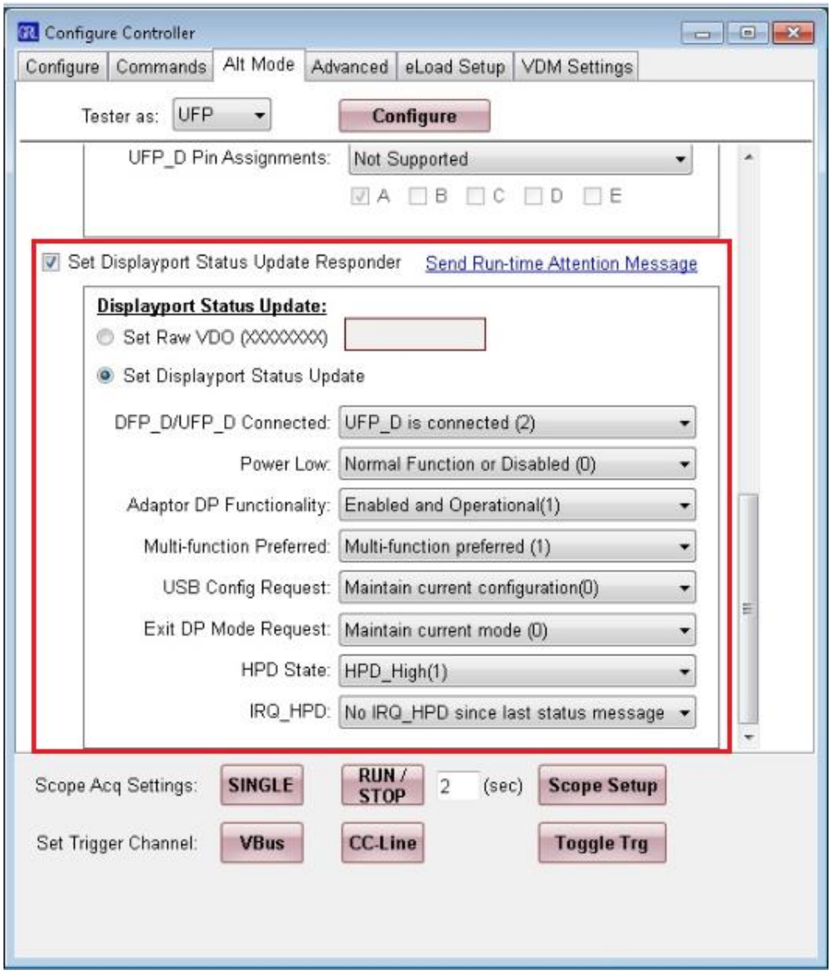


FIGURE 54: ALT MODE – SET STATUS MESSAGE

6.2.2.3 Performing DisplayPort 2+2 Lane DP 1.2b Source PHY Testing

Refer to Section above for the PHY Test procedure using *TE vendor specific PHY test software*.

6.2.3 Combining Max Power Provider Configuration with Above Test Conditions

1) Assign maximum PDO Index supported by DUT in Request Message settings in Configure tab as shown in Figure 55.
2) Configure the GRL-USB-PD-C1 PDO request message setting with the maximum current PDO index of the DUT as shown in Figure 55.
3) In Operation dropdown, select Assign from the drop down.
4) Click Request Command button.
5) Based on the number of lanes in the Display Port refer to section 6.2.1.1 or 6.2.2 for the configurations to be set.

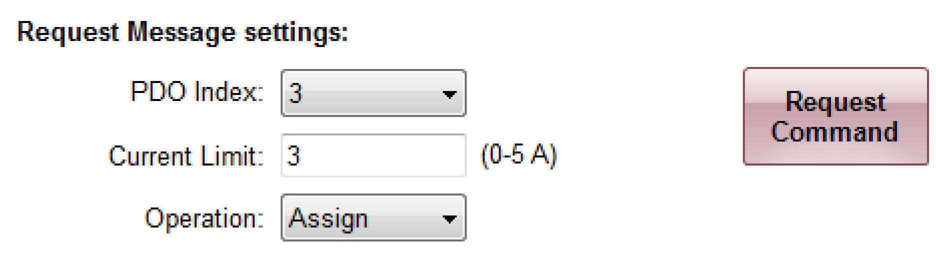
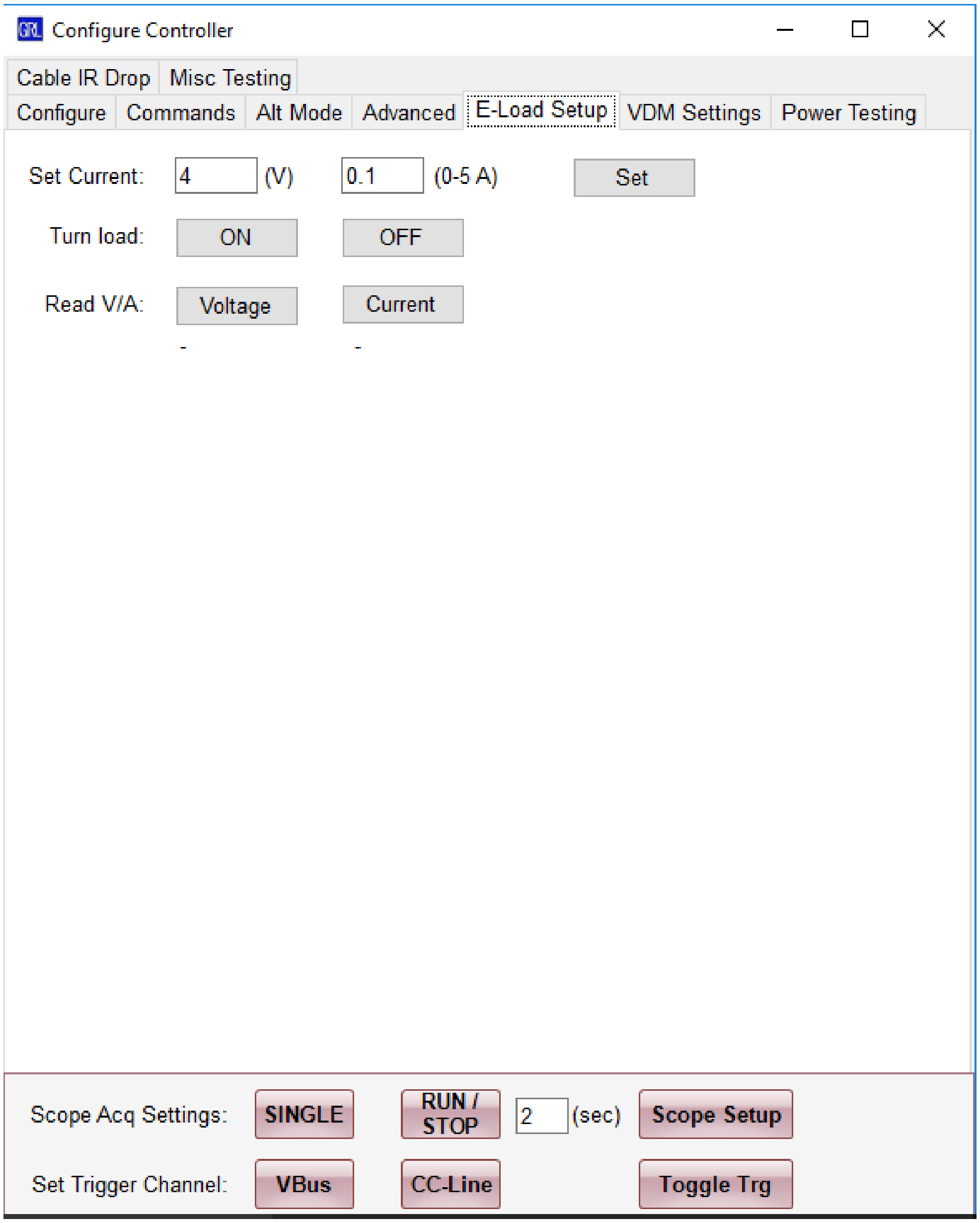


FIGURE 55: CONFIGURE TAB – REQUEST MESSAGE SETTINGS FOR PDO

In the e-Lload setup it is preferred to set the maximum current for testing.

Note: Refer to section below for the Oscilloscope and eLoad Connection Setup.



6) Follow the DisplayPort testing described in the previous sections after configuring the controller with the PDO index request message setting.

6.2.4 GRL Aux Configuration Tool

After configuring the GRL-USB-PD-C1 as explained in the above section, Display Port PHY testing follows the steps below. A "GRL Aux Config Tool" is used for configuring the DPCD registers of DPR-100 is shown in Figure 56.

1) Before configuring DP Sink or Source Device supply a correct DPR-100 license key to the Serial Key field of the "GRL Aux Config Tool" application.
2) Based on the DUT capability select the drop down list from Aux Config Tool Application and press "Set".
3) After above step, the DUT screen will blink once indicating the new DPCD register configuration has been set and Attention command being initiated using CC line from the GRL-USB-PD-C1 controller.
4) After step 3, DUT will initiate read request on Aux line and read DPCD registers from DPR-100, then link training starts. Status of the command will be displayed next to "Status:"
5) With all above steps executed successfully, the DisplayPort Main Link signals connected to the Scope from the DUT should be observed for a change with respect to the configuration set in the "GRL Aux Config Tool".

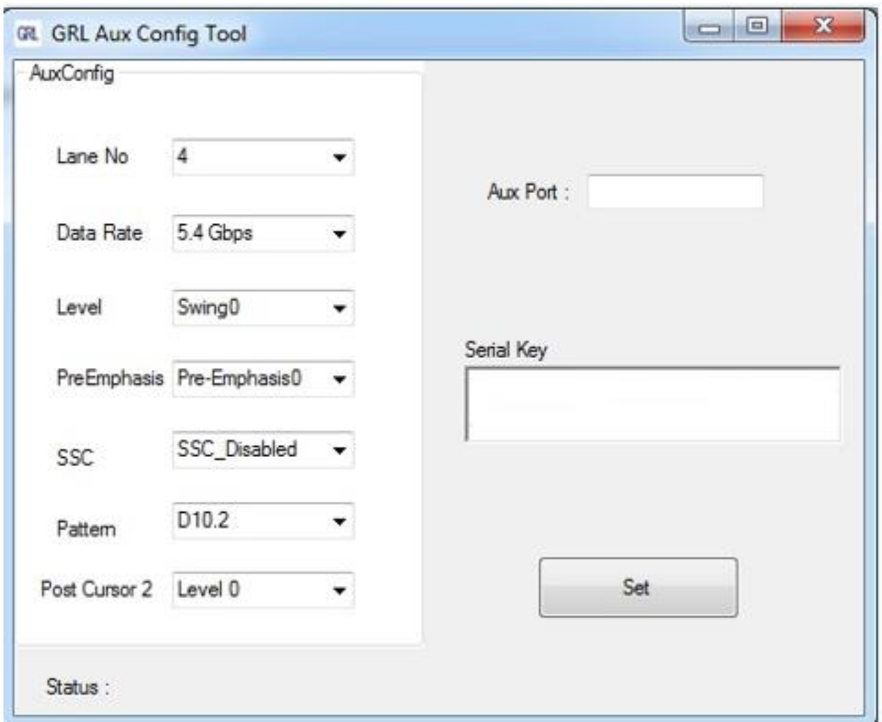


FIGURE 56: GRL UTILITY FOR DISPLAYPORT DPCD SETTING

6.3 DisplayPort on Type-C DP 1.2b PHY Sink Testing

6.3.1 Configuring a DUT for Sink Testing

1) Configure **SVID Responder**, **Discover Mode Responder**, **DisplayPort Status Update** Responder messages details in Alt mode tab as shown in Figure 40. For configuring controller in Source 2+2 mode, follow the example mentioned in each section below. Up

to Discover Mode VDM message, the Tester will initiate automatically after setting "Enable VDM" and "VDMConfig_TesterSource_ACK" in the Mode Settings of the Configure tab and click **Send** button to set the configuration in the Tester.

2) TO SEND ENTER MODE, STATUS UPDATE AND DP CONFIGURATION MESSAGES, USE THE COMMAND TAB AND the Alt Mode tabs:

1. Select signaling support to **DP v1.3** in **DisplayPort Capabilities** section. The table below may be considered for configuring the Controller as Source for 2+2 mode, with 2 lanes for DP main link and 2 lanes for USB3.0 data signaling.

*Note: Select the **Pin Assignments** based on the connected Sink device. Refer "Pin Assignment and Description" section of the DP Alt Mode on Type-C specification.*

2. The configuration in Figure 58 may be taken as an example for setting the Status message of the Sink, and for sending attention message whenever change in the Aux signaling or in the VDM configuration to have impact on the DUT.
3. Enable oscilloscope acquisition.
4. Get the DUT into **PD Source** mode.
5. Decode and analyze the message sequence.

3) Get the DUT into PD Sink mode.
4) Assign SVID value as FF01 in the Commands tab.
5) Send Enter Mode Initiator message.
6) Configure and send the DisplayPort Status message sections as shown in Figure 57, based on the DUT capabilities.

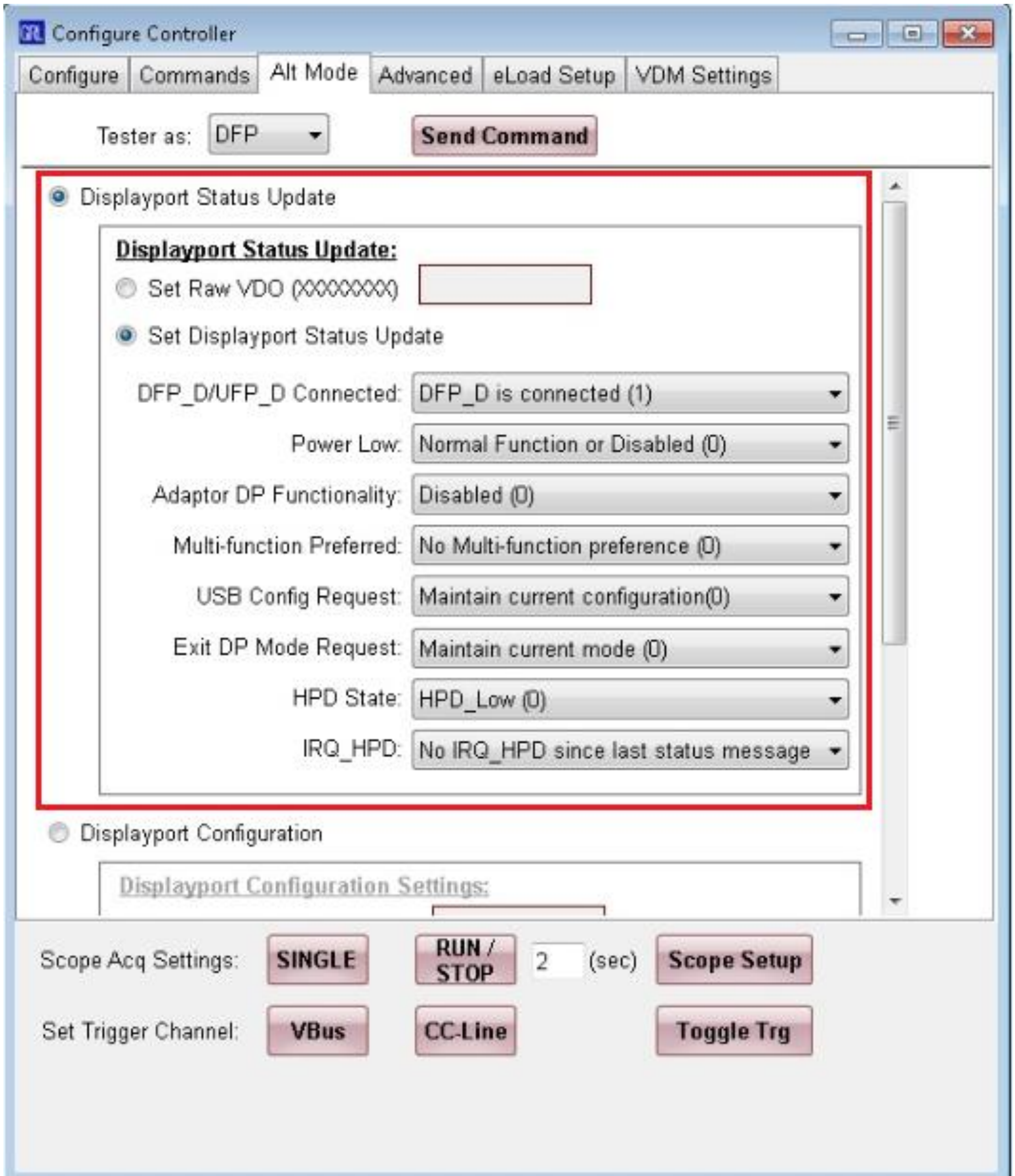


FIGURE 57: ALT MODE TAB IN CONFIGURE CONTROLLER – 2+2 LANE SINK STATUS

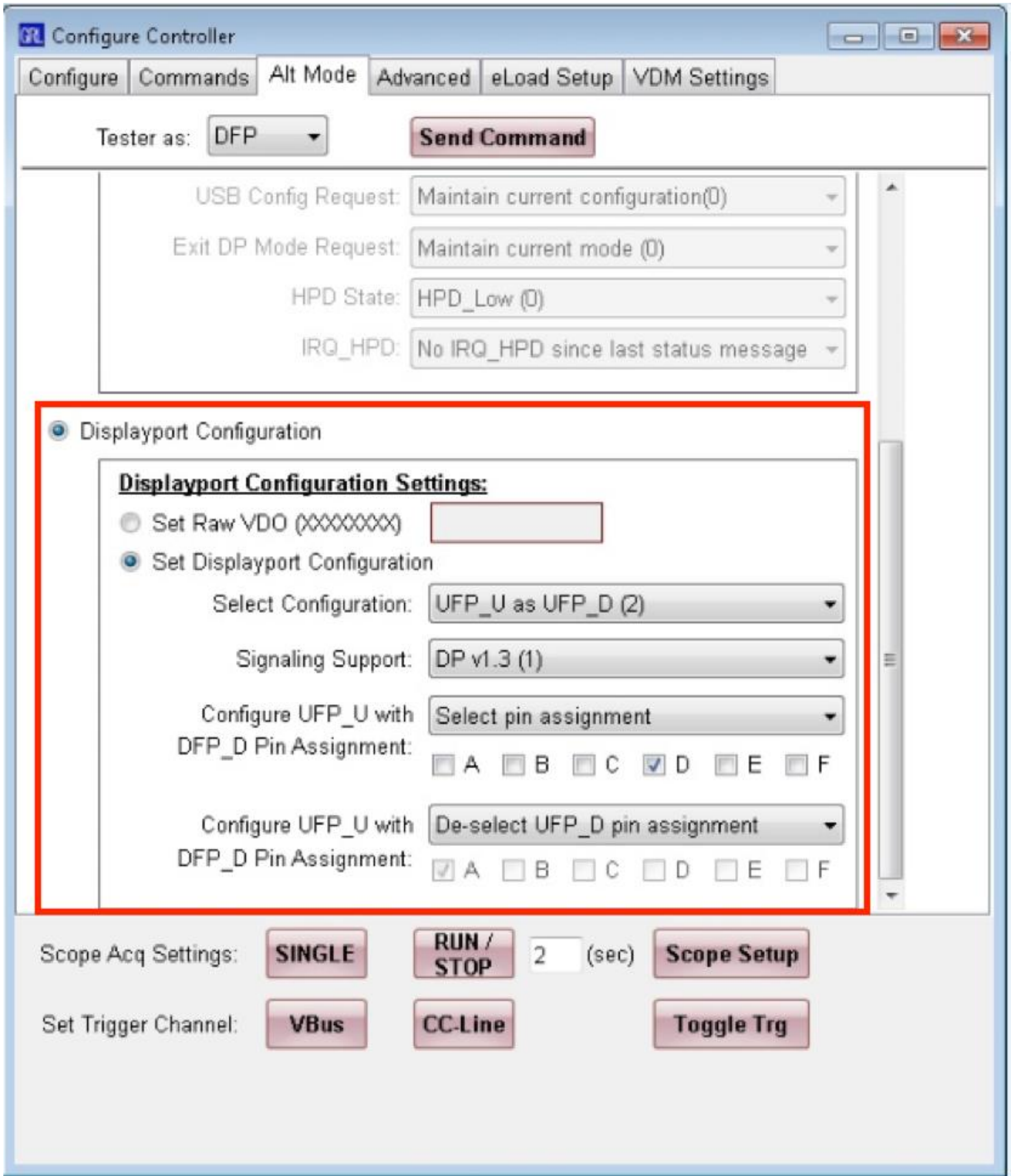


FIGURE 58: ALT MODE TAB IN CONFIGURE CONTROLLER – 2+2 LANE SINK CONFIG

7) Select the signaling support to DP v1.3 and assign the pin configurations based on the DUT capabilities and send the DisplayPort Configuration message section as shown in Figure 58.
8) Select the signaling support to USB Gen2 and assign the pin configurations based on the DUT capabilities and send the DisplayPort Configuration message section as shown in Figure 58.

6.3.2 Combining Max Power Provider Configuration with Above Test Conditions.

1) Assign maximum **PDO Index** supported by DUT in **Request Message settings** in Configure tab as shown in Figure 59.
2) Set **maximum current** offered by DUT for the selected PDO index.
3) Choose **Assign** in the Operation drop down and click on Request Command button.
4) Get the DUT into PD Source mode.
5) Based on the number of lanes in the Display Port refer to section 6.2.1.1 or 6.2.2 for the configurations to be set.

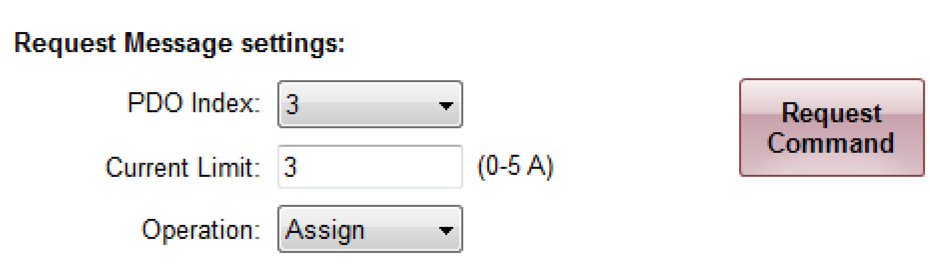


FIGURE 59: CONFIGURE TAB – REQUEST MESSAGE SETTINGS FOR PDO

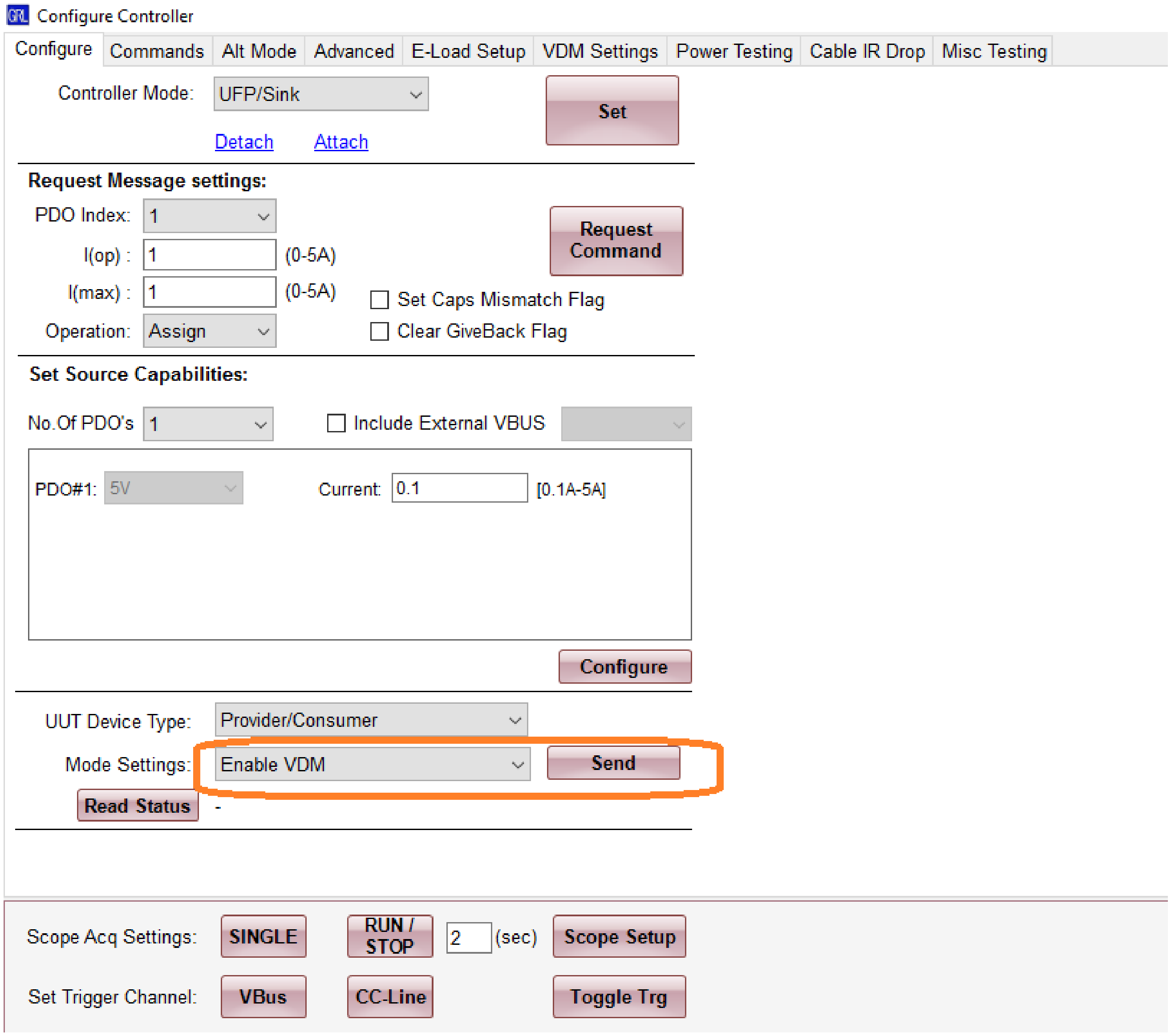


FIGURE 60: ALT MODE TAB IN CONFIGURE CONTROLLER – 2+2 LANE SINK ENABLE VDM

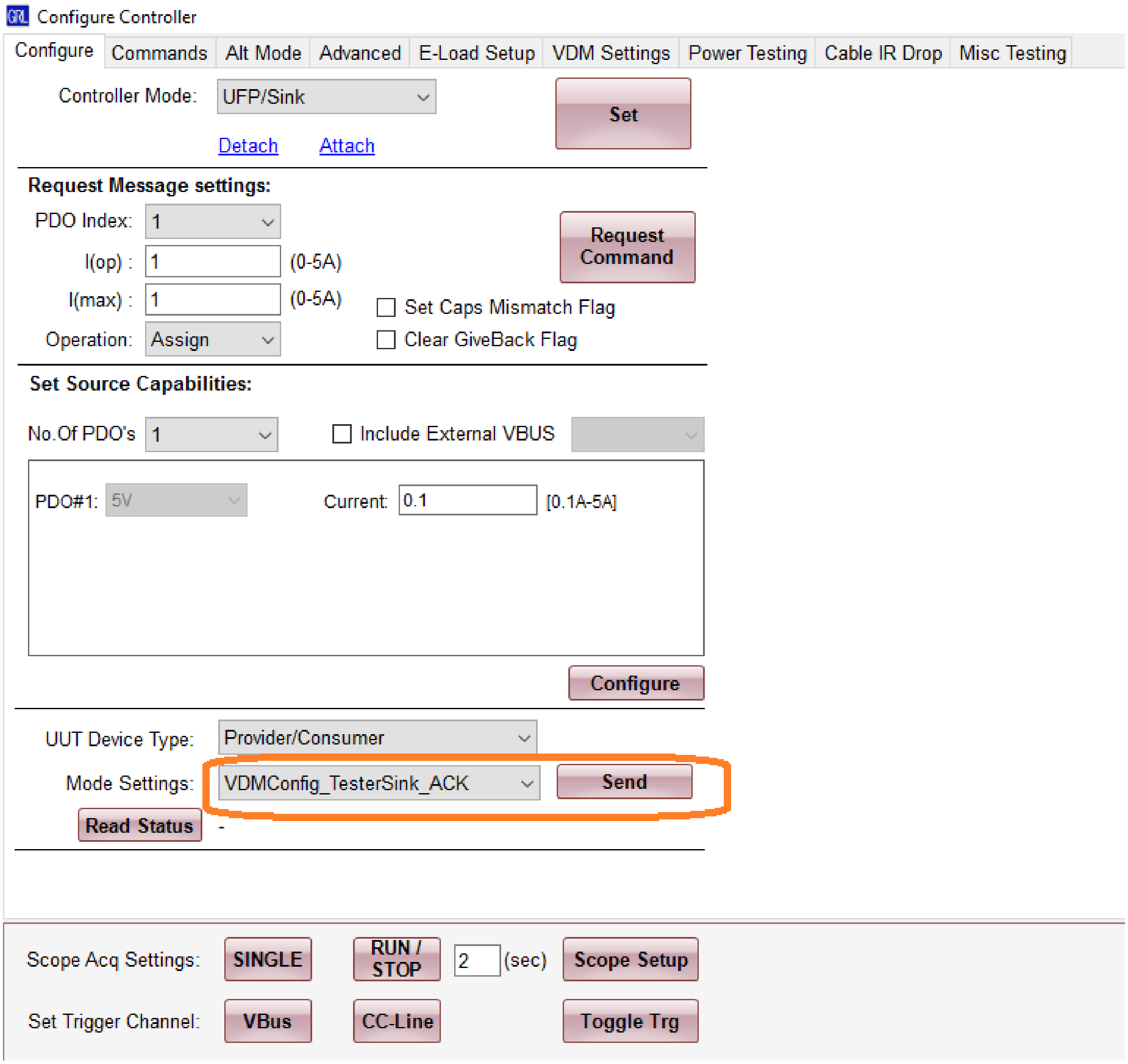


FIGURE 61: ALT MODE TAB IN CONFIGURE CONTROLLER – 2+2 LANE SINK VDMCONFIG

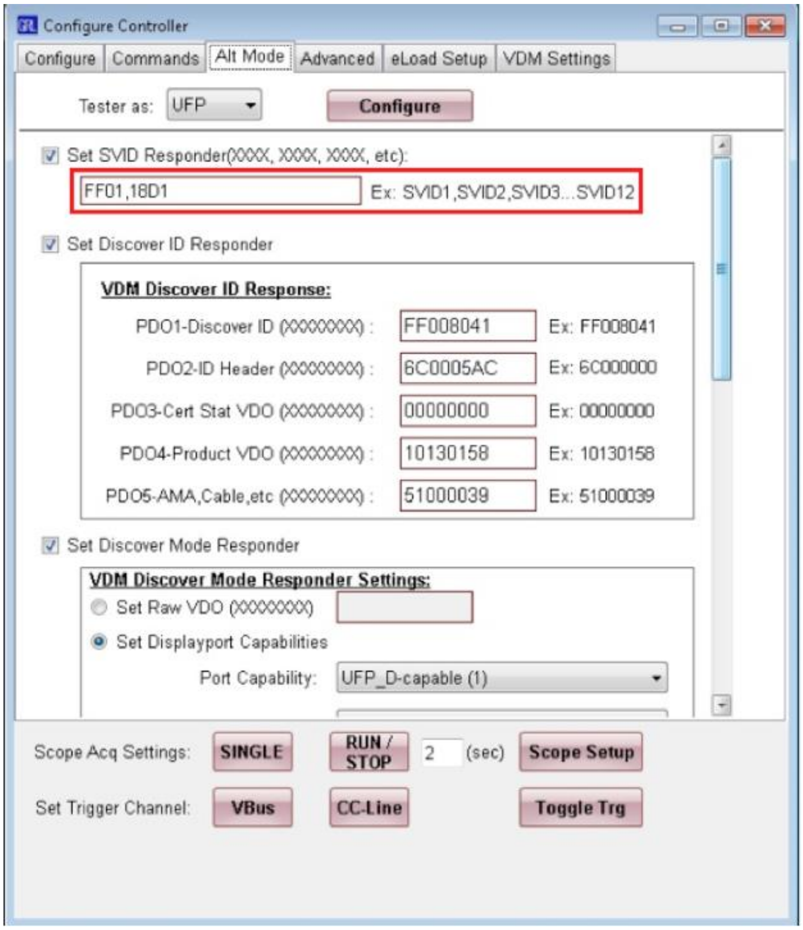


FIGURE 62: ALT MODE TAB IN CONFIGURE CONTROLLER – 2+2 LANE SINK SVID VDM

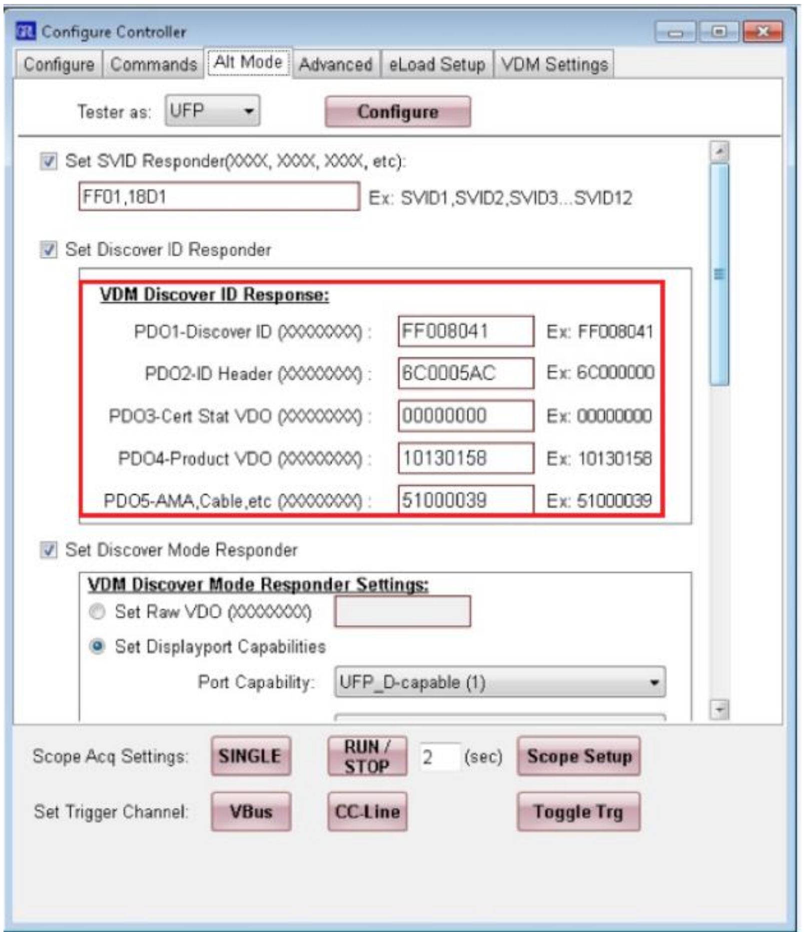


FIGURE 63: ALT MODE TAB IN CONFIGURE CONTROLLER – 2+2 LANE SINK DISCOVER VDM

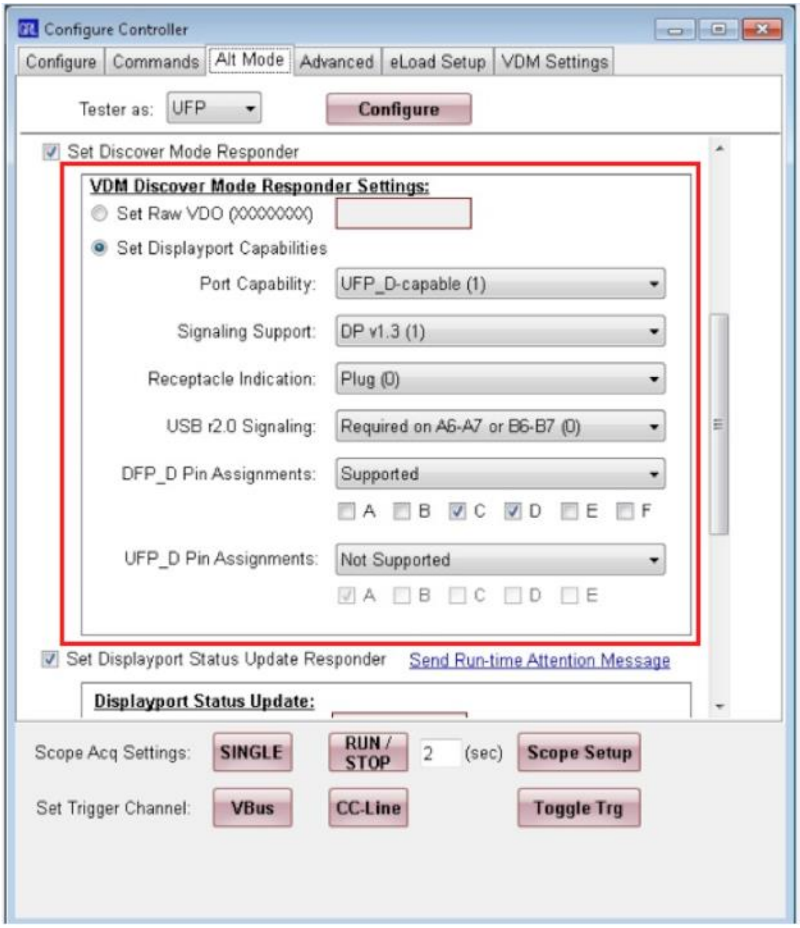


FIGURE 64: ALT MODE TAB IN CONFIGURE CONTROLLER – 2+2 LANE SINK RESPONDER

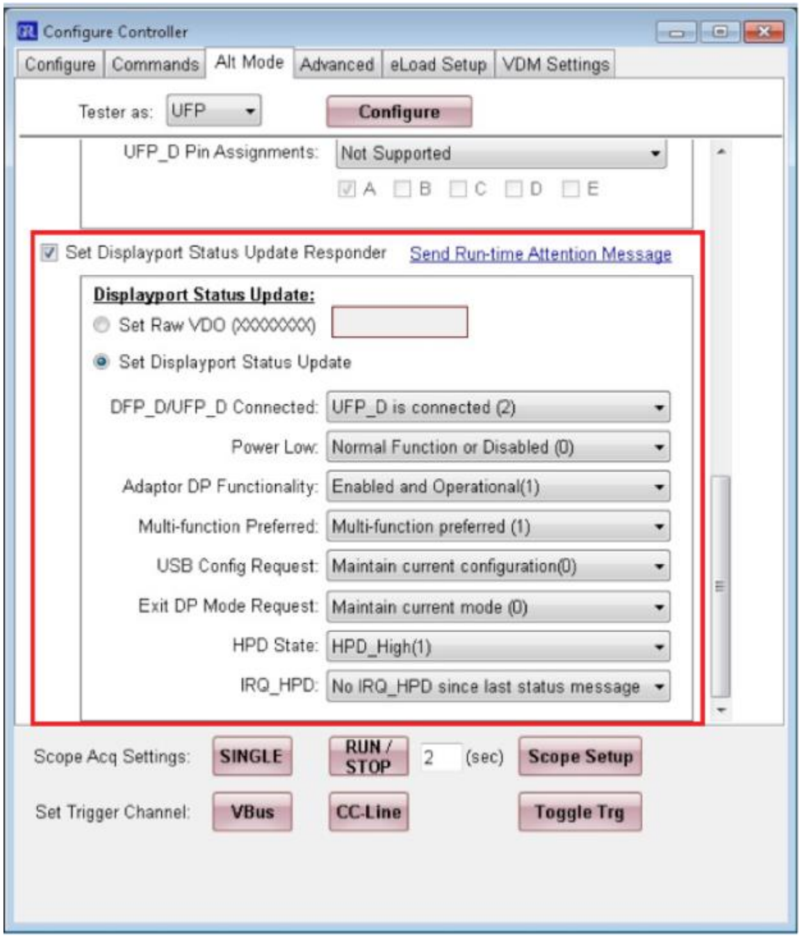


FIGURE 65: ALT MODE TAB IN CONFIGURE CONTROLLER – 2+2 LANE SINK STATUS

7 Additional Test Procedures

7.1 Procedure to Enable Vbus from external power supply

1. By default, GRL USB-PD-C1 test solution provides three VBus source voltage levels (5V, 12V and 20V). To have customized VBus source voltage level, user can make use of external DC power supply by connecting it to theTester rear panel and with following software configuration.

2. Configure external DC power supply to provide required VBus voltage level (5V - 20V) and connect it to Tester's rear panel **Vbus IN** socket.

3. Open Config Controller Window from Decoder Configuration panel in GRL USB-PD SW.

4. Configure required power profiles under **Set Source Capabilities** section and check "**Include External Vbus"** option to select choose Vbus from external DC power supply for one of the source power profile**.**

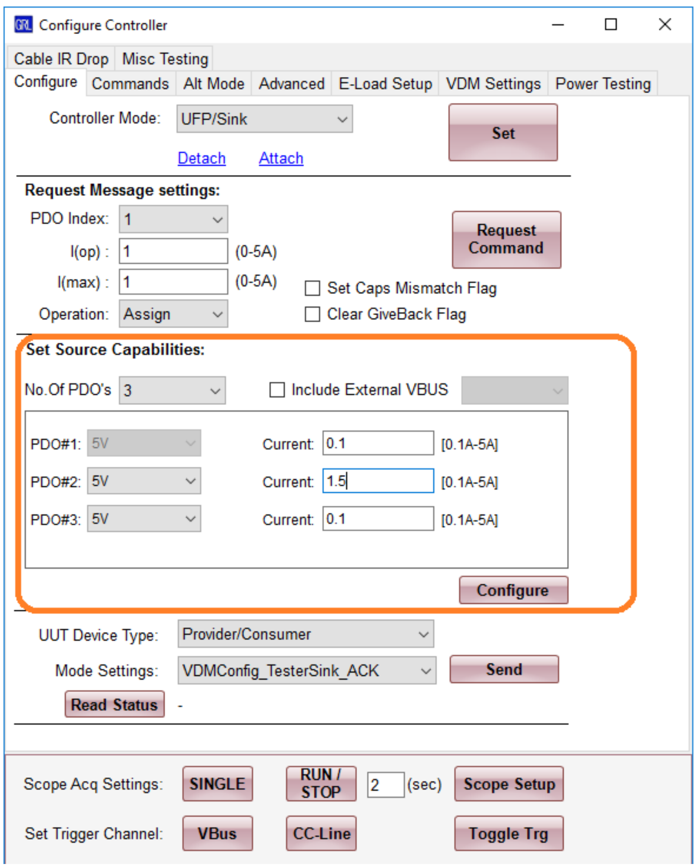
5. Choose the power profile index where external Vbus has to be configured in the drop down box next to "**Include External Vbus**" as shown in below figure.

6. Click on Configure button to set the source capabilities.

7. Configure the controller mode as **DFP/Source** at the top of the Config Controller window and click **Set** button next to it to configure Tester as Source.

8. Probe CC-Line and Vbus to scope to verify the Vbus voltage level.

9. Connect the DUT and click on **Attach** link under the Controller mode to negotiate the PD contract.



7.2 Procedure to Test External VConn (3V)

Following is the step by step description to perform for the external VConn(3V) testing

Step1: Connect Probe of External Power Supply to **CC2-GND** at **Probing Points** input of GRL-USB-PD-C1 using the **Probe-Ext1** board.

Step2: Set the Voltage Level to 3V in the External Power Supply

Step3: Connect **Ch1** Passive Probe to **CC1-GND** at **Port-A Probing Points** input of GRL-USB-PD-C1 using the **Probe-Ext1** board.

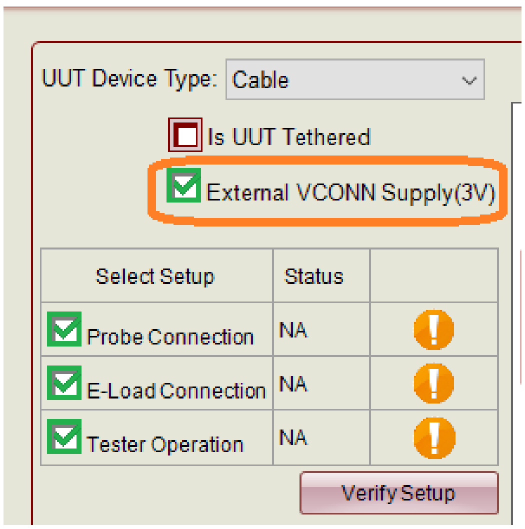
Step4: Make sure VBus is not connected.

Step5: Navigate to Test Step Connection Panel.

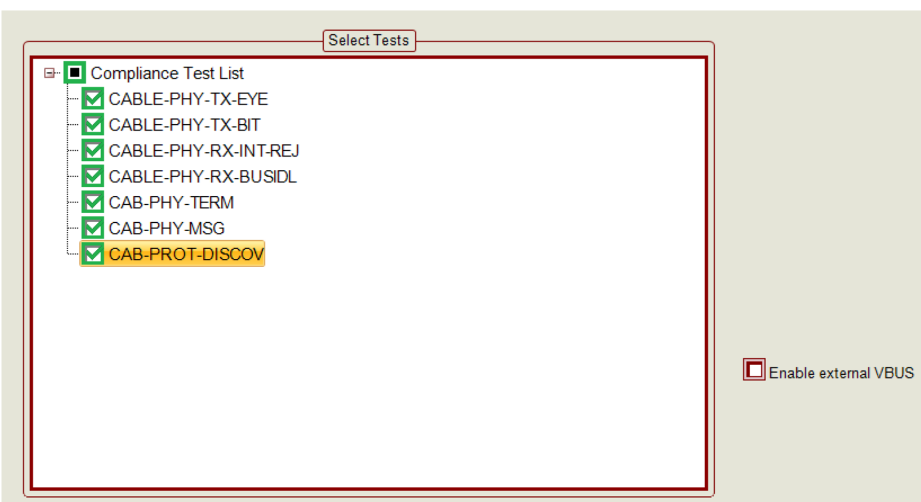
Step6: Select Cable as UUT Device Type

Step7: Make Sure the Cable type DUT is connected to the Controller.

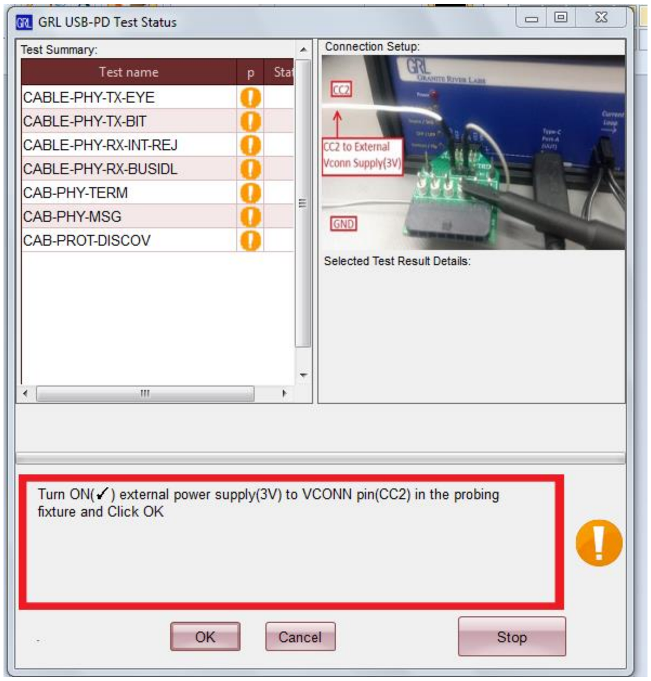
Step8: Check the External VConn Supply (3V) option as shown below.



Step9: Navigate to Test Selection Panel. Select the Tests as shown below and run the Compliance Test as shown below.



Step10: Carefully follow the instruction as to turn ON/OFF the power supply during test execution as shown below.



Step11: Once the Compliance test execution is completed for all cases reverse the cable and connect it to the controller. If required Save the Reports.

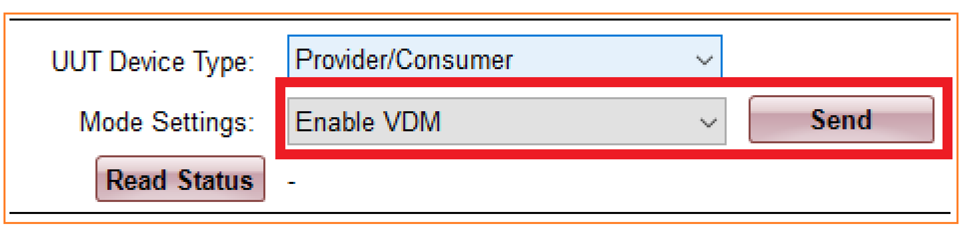
Step12: Re Run the Compliance Test

Step13: Once the Compliance test execution is completed for all Navigate to Test Selection Panel and un check the External VConn Supply (3V) option. Turn Off External Power Supply.

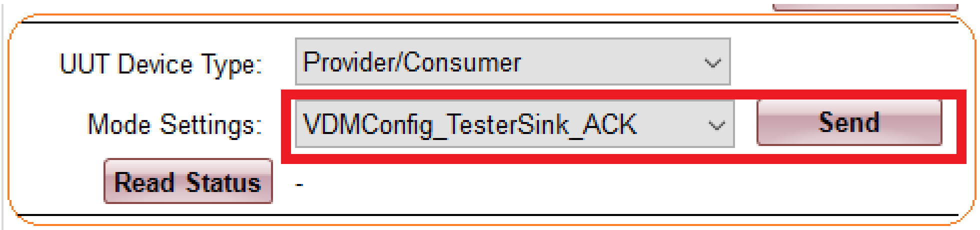
Step14: Re Run the Compliance Test for Internal 5V Power Supply for both ends of the cable.

7.3 Procedure to Test Alt-Mode for ThunderBolt Device

Step1: Open Config Controller window and Send Enable VDM command in Mode Settings Drop down Box.



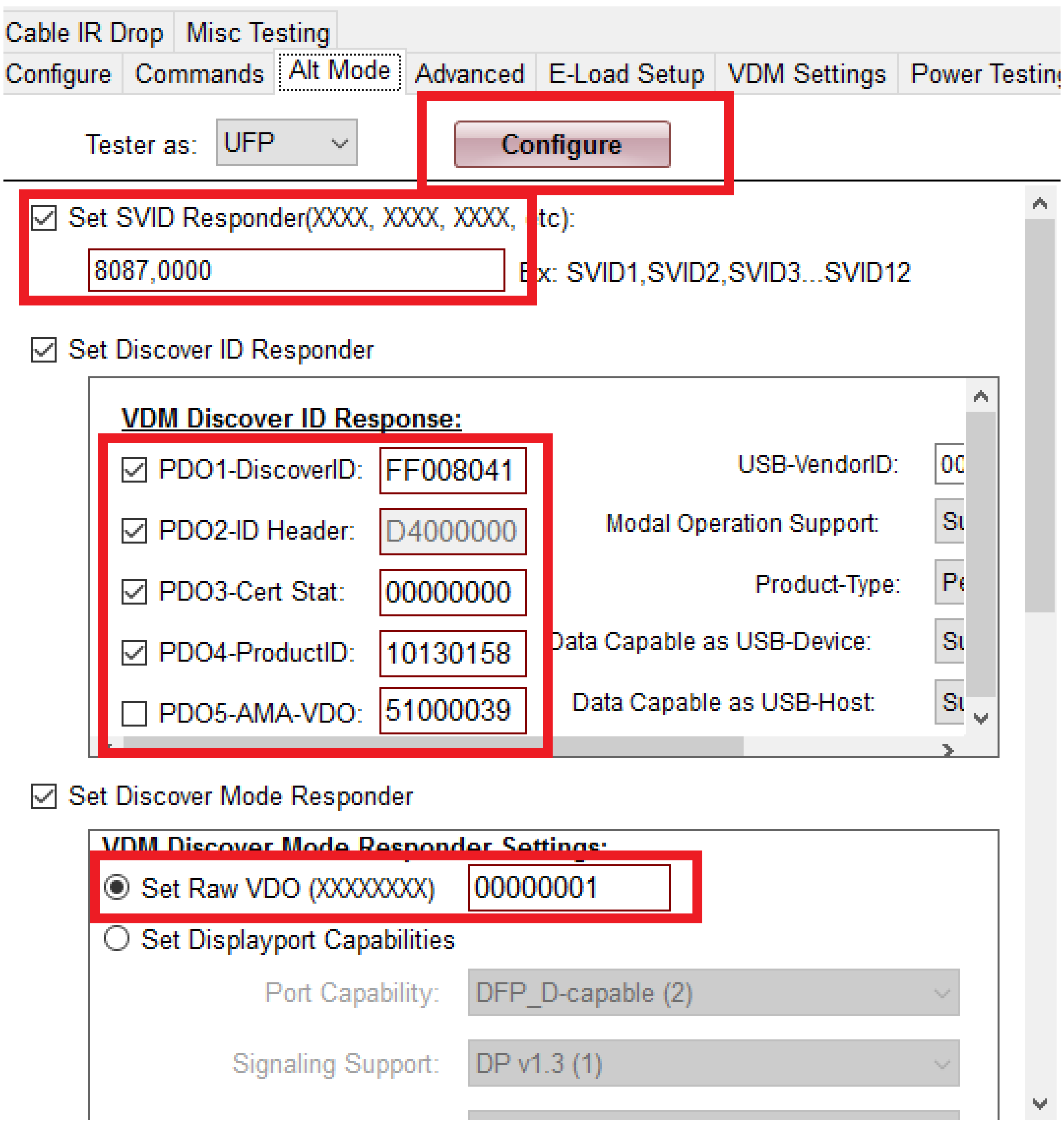
Step2: Send VDM_ConfigTestersink_ACK command from Mode-Settings Drop down Box.



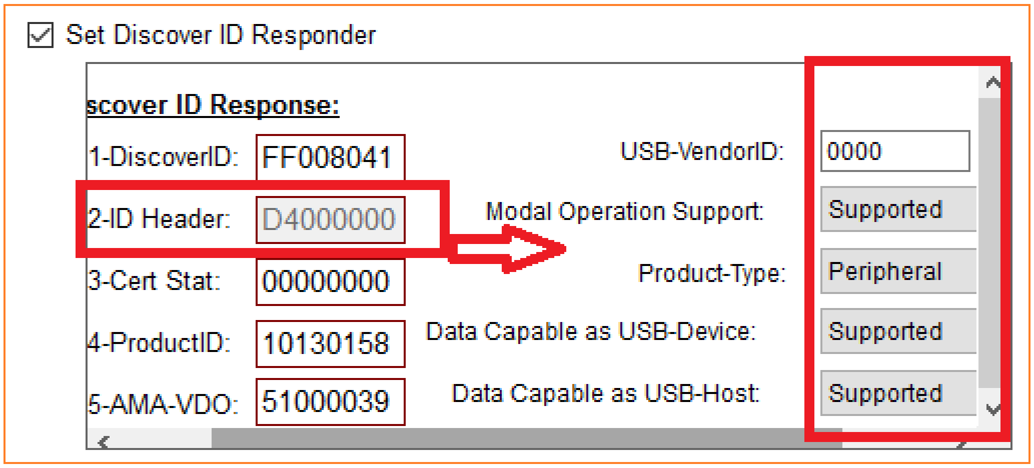
Step3: Navigate to Alt mode tab and Select Tester as UFP

Step4: Select SVID responder and Set SVID as “8087”.

Step5: Then select Discover-ID responder and Configure as shown below.



Step6: In Discover-ID responder select ID-Header as shown below.



Step7: Select Discover mode responder and select Raw data and set ”0x00000001”.

Step8: Click Configure Button.

Step9: Perform PD-Contract.

Step10: Navigate to Packet Capture Tab in Product Capability Window and verify that the device has initiated the Enter Mode.

8 Universal Serial Bus Type-C and Power Delivery Source Power Requirements Testing

8.1 Test Plan Overview

The *USB-C_Source_Power_Test_*is developed by the USB-IF’s Power Delivery Working Group.

The following sections include summaries of tests that are covered from Chapter 2 of the test plan *USB-C_Source_Power_Test_Specification_2015_12_30* for the Certification.

The ‘Test Name’ in the following table can be cross-referenced with the test cases in Chapter 2 of the test plan, to identify the test assertions covered by each test.

Test Ref #	Test Name	Test Description
2.1	Load Test	The Load test verifies that when each port is fully loaded at voltage V the Source can still deliver voltage in the tolerance range of vSrcNew or vSafe5V.
2.3	Hard Reset Test	The Hard Reset Test verifies that the PD Source port follows the voltage requirements for a PD Hard Reset.
2.5	Over Current Test	The Over Current Test verifies that the PD Source port follows the overcurrent requirements

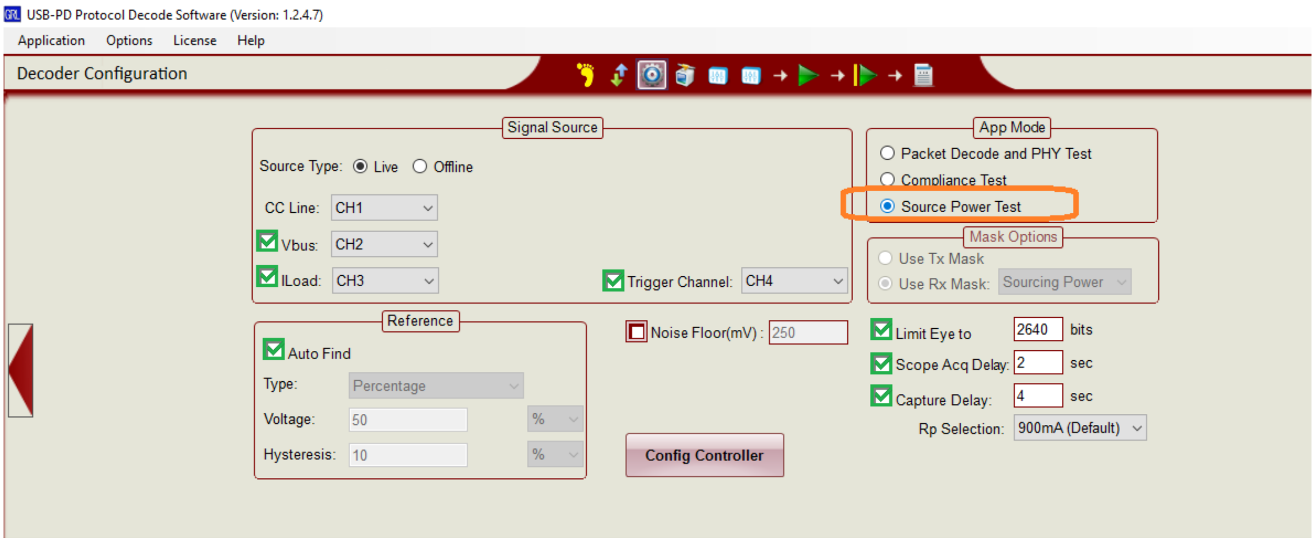
Note:

1. The supported test cases are can be run on one USB PD port at a time.

2. For the values of vSrcNew, vSrcNeg ,vSrcSlewPos ,vSafe5V,tSrcSettle ,tSrcReady ,tSrcReady ,vSrcNew and tSrcTransient refer to the USB Power Delivery Specification.

Refer to section 3 and 4 for installing the software and doing the oscilloscope and E-Load setup.

In Decoder Configuration Window choose Source Power Test in the App Mode Setting as shown below.

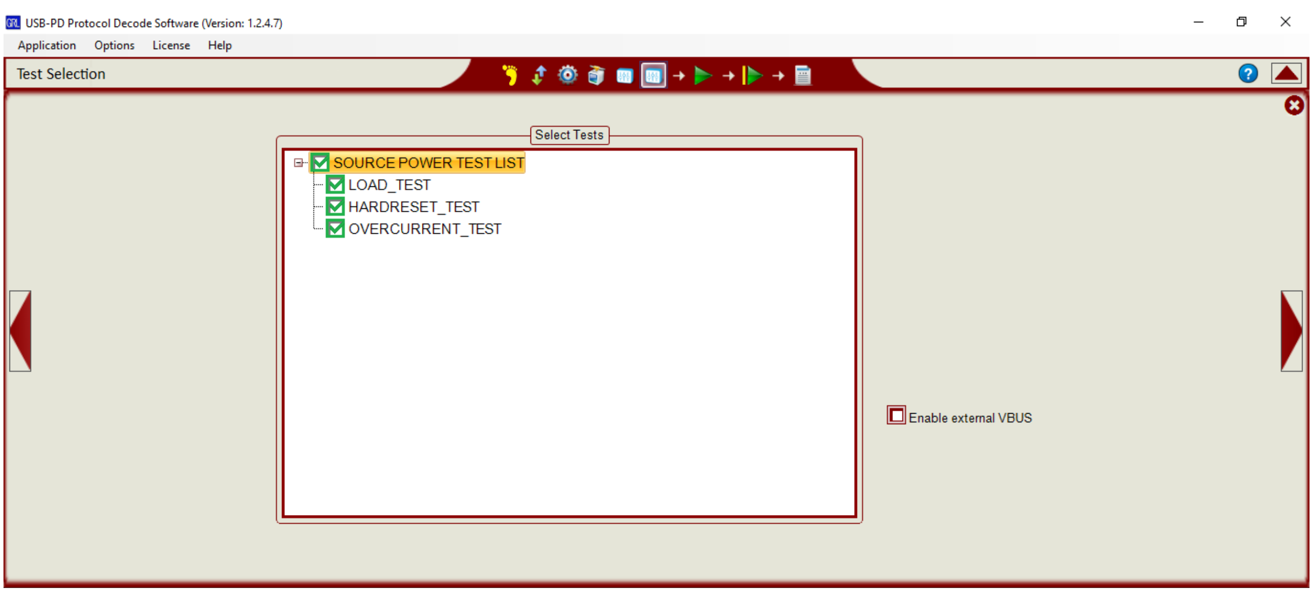


In Test Setup Connection, select UUT type as one of the following options.

- Consumer\Provider
- Provider\Consumer
- Provider Only
- DRP

Navigate to Product Capability Window. Import and Validate the DUT Capabilities as shown in 5.10.3. Verify that the Power Capabilities of the DUT is updated correctly in Power Capabilities tab.

Got to Test Selection Window. Select the Source Power Tests as shown below and Run the Test Cases.



8.1.1 Load Test

A. Purpose:

1. The Load test verifies that when each port is fully loaded at voltage V the Source can still deliver voltage in the tolerance range of vSrcNew or vSafe5V. 2.
2. This test is required for all USB Type-C source-capable ports.

B. Asserts Covered:

1. 7.1.4#2
2. 7.1.4#3
3. 7.1.4#4
4. 7.1.4#5
5. 7.1.4#6
6. 7.1.4#7
7. 7.1.4#8
8. 7.1.9#1
9. 7.1.9#2
10. 7.1.9#3

C. Procedure:

1. For each attached port the SPT (Source Power Tester) connects and utilizes a Sink Capability of 5V, 0 A

2. During each port attach process the SPT verifies:

    a. If the Source voltage initially droops, it shall not fall below vSrcNeg.

    b. After the Source transitions its voltage out of vSafe0V range, its voltage increases monotonically under vSrcSlewPos rate until the voltage passes vSafe5V min.

    c. The Source voltage remains within vSafe5V once it crosses vSafe5V min.

    d. The Source settles into vSafe5V within tSrcSettle from its initial transition out of vSafe0V range.

    e. The remaining attached ports do not droop more than 330mV or for longer than tSrcTransient

3. For the first port Px with which the SPT establishes a contract:

    a. SPT requests max current for the next untested Source Capability PDO (let V be the Voltage of this PDO):

        1. The SPT sends a Request for the PDO

        2. The SPT verifies:

            a. If the Source voltage initially droops, it shall not fall below vSafe5VTransition.

b. After the Source transitions its voltage out of vSafe5V range, its voltage increases monotonically under vSrcSlewPos rate until the voltage passes vSrcValid min.

c. The Source voltage remains within vSrcValid range once it crosses vSrcValid min.

d. The Source settles into vSrcNew within tSrcSettle from its transition out of vSafe5V range.

e. The remaining attached ports do not droop more than 330mV or for longer than vSrcTransient.

3. After tSrcReady from the initial voltage transition, the SPT enables the max load in 25% increments.

4. The SPT verifies:

a. If the Source voltage leaves vSrcNew range, it stays within vSrcValid and returns to vSrcNew within tSrcTransient.

b. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than vSrcTransient.

b. If nNumPorts > 1, then for each remaining port Py:

1. If the port supports PD:

a. The SPT requests max current for the Source Capability PDO at voltage V.

i. If the PDO at V does not exist, skip the port and continue with the next port at step 0.

ii. The SPT sends a Request for the PDO.

iii. The SPT verifies:

1. If the Source voltage initially droops, it shall not fall below vSafe5VTransition.

2. After the Source transitions its voltage out of vSafe5V range, its voltage increases monotonically under vSrcSlewPos rate until the voltage passes vSrcValid min.

3. The Source voltage remains within vSrcValid range once it crosses vSrcValid min.

4. The Source settles into vSrcNew within tSrcSettle from its transition out of vSafe5V range.

5. The remaining attached ports do not droop more than max (330mV, vSrcNew) or for longer than tSrcTransient.

iv. After tSrcReady from the initial voltage transition, the SPT enables the max load in 25% increments.

v. The SPT verifies:

1. If the Source voltage leaves the vSrcNew range, it stays within vSrcValid and settles to vSrcNew within tSrcTransient.

2. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than tSrcTransient.

2. If the port does not support PD the SPT loads the max current advertised on Rp.

a. The SPT verifies:

i. The Source voltage does not droop more than 330mV or for longer than tSrcTransient.

ii. The remaining ports do not droop below max (330mV, vSrcNew) or droop for longer than tSrcTransient.

3. Move to step 0 for the next remaining port.

c. For each port Py loaded in step 0

1. The SPT disables the load in 25% increments.

2. The SPT verifies:

a. If the Source voltage leaves the vSrcNew range, it stays within vSrcValid and settles to vSrcNew within tSrcTransient.

b. The remaining ports do not leave vSafe5V or vSrcNew range.

3. Move to step 0 for the next loaded port.

d. For port Px loaded in step 0

1. The SPT disables the load in 25% increments.

2. The SPT verifies:

a. If the Source voltage leaves the vSrcNew range, it stays within vSrcValid and settles to vSrcNew within tSrcTransient.

b. The remaining ports do not leave vSafe5V or vSrcNew range.

e. If the Source Capability PDO (at voltage V) on Port Px advertised peak current capability, return to step 0, Request the PDO again and step through the test while utilizing the peak current with operating current at 2/3 max current advertised on Port Px.

f. Move to step 0 to test the next Source Capability PDO.

4. If no port supports USB PD:

a. For each port Px:

1. The SPT loads the max current advertised on Rp.

2. The SPT verifies:

a. If the Source voltage does not droop or drop below 330mV or for longer than tSrcTransient.

b. The remaining ports do not droop more than 330mV during the transient load on the port Px or for longer than tSrcTransient.

8.1.2 Hard Reset

A. Purpose:

1. The Hard Reset Test verifies that the PD Source port follows the voltage requirements for a PD Hard Reset.
2. This test is required for all USB Type-C source-capable ports.

B. Asserts Covered:

1. 7.1.6#1
2. 7.1.6#4
3. 7.4.1#17

Test Procedure:

1. The SPT attaches all ports and utilizes a Sink Capability of 5V, 0A.

2. For each port with which the SPT establishes a PD contract:

a. Request the max current for the highest voltage Source Capability PDO.

b. The SPT verifies the PD request is accepted and a contract is established.

c. The SPT applies the max load in 25% increments.

d. The SPT sends a Hard Reset.

e. The SPT verifies that from the start of the Source voltage transition:

1. The Source voltage drops to vSafe5V within tSafe5V

2. The Source voltage drops to vSafe0V within tSafe0V

f. The SPT disables the load on the port.

g. The SPT verifies:

1. The Source voltage remains within vSafe0V for tSrcRecover

2. The Source voltage does not dip below vSrcNeg for the duration of the Hard Reset.

8.1.3 Over Current Test

A. Purpose:

1. The Over Current Test verifies that the PD Source port follows the overcurrent requirements.
2. This test is required for any PD source-capable port.

B. Asserts Covered:

1. 7.1.8.3#1

2. 7.1.8.3#2

C. Test Procedure:

1. The SPT attaches all ports and utilizes a Sink Capability of 5V, 0A.

2. For each port with which the SPT establishes a PD contract:

a. The SPT requests the max current for the negotiated source PDO

b. The SPT applies the negotiated current load to the port in 25% increments

c. The SPT increases the load by 100mA

d. If a hard reset is detected, the SPT verifies:

1. The voltage transition below vSrcValid min occurs within tSrcOcPresent after the load was increased.

2. After transition below vSrcValid, the voltage decreases monotonically toward vSafe0V

e. Else if the load =< 5.5A, Repeat step C.2.cc. f. Disable the load

g. The SPT informs the user of the value at which the over current condition triggered or the maximum current applied if it did not trigger.

h. Repeat step C.2.a for the next advertised Source Capability PDO until no more exist

9 Appendix A: USB Type-C Controller (GRL-USB-PD-C1)

9.1 General Information

9.2 GRL-USB-PD-C1 Shipping Box Contents

GRL-USB-PD-C1 Controller

9.2.1.1.1 **USB Type-C Test Cable** – 25cm (10 inch) Type-C 5A eMark Cable, used for connecting the UUT to the Controller.

Probe EXT-1 helps to probe CC Line & Vbus to Oscilloscope. This fixture will be connected into Port A probe points.

Probe EXT-2 helps to probe CC line & Vbus from the Port B Type C Port. This fixture will be connected into Port B probe points.

E-Load / Vbus connectors. Helps to connect Vbus & E-Load to controller.

Vbus in and Power input connectors. Using this port Vbus can be supplied from the external power supply.

Current loop to connect the current probe. This should be installed for the normal operation of the controller.

Text fixture connector cable

USB 3.0 Control cable used to connect the tester and Oscilloscope.

USB Programming cable used to update the FPGA data and will be connected into system upgrade USB port.

Power Supply & Power Cord

1M BMC Cable

9.3 GRL-USB-PD-C1 Connection Details

Step 1 Install the current loop on the front panel of USB-PD-C1

USB Type-C^{TM} Test Controller Front Panel

Step 2 Plug on E-Load connector in the rear panel as shown below.

USB Type-C^{TM} Test Controller Rear Panel

Step 3 Connect power supply adapter to the Power port in the rear panel.

Step 4 Connect Probe EXT-1 into Port-A probe points on the front panel. Connect Vbus and CC1/CC2 of Probe EXT-1 to oscilloscope channels.

Step 5 Connect the tester through USB 3 Connector (given on the rear panel) to the Oscilloscope. Install the drivers if they are not installed.

Step 7 There are 5 LEDs on the front panel.

Power LED	Once the power supply switch is on, the Power LED turns red, while the remaining LEDs turn orange which indicates that the tester is in Sink state.
Attach/Detach (Green/Orange)	Connect any DUT using Type C Cable. The Attach/Detach LED turns green once the DUT is attached, and it turns orange when the DUT is detached.
Source/Sink (Green/Orange)	When the tester is configured as Source, the LED turns green, and when the tester is attached as Sink the LED turns orange.
DFP/UFP (Green/Orange)	Once the data role is in DFP, the LED turns green. In UFP it turns orange.
Contract Flip	If tester's CC1 is connected to CC2 of the DUT, a Flip occurs.

10 Appendix B: Using the Configuration Utility

This section describes how to use the **Config Controller** utility, which is used to manually send USB-PD Commands from the GRL-USB-PD-C1 controller. To access the **Config Controller** utility, go to the **Decoder Configuration** menu and press the **Config Controller** button.

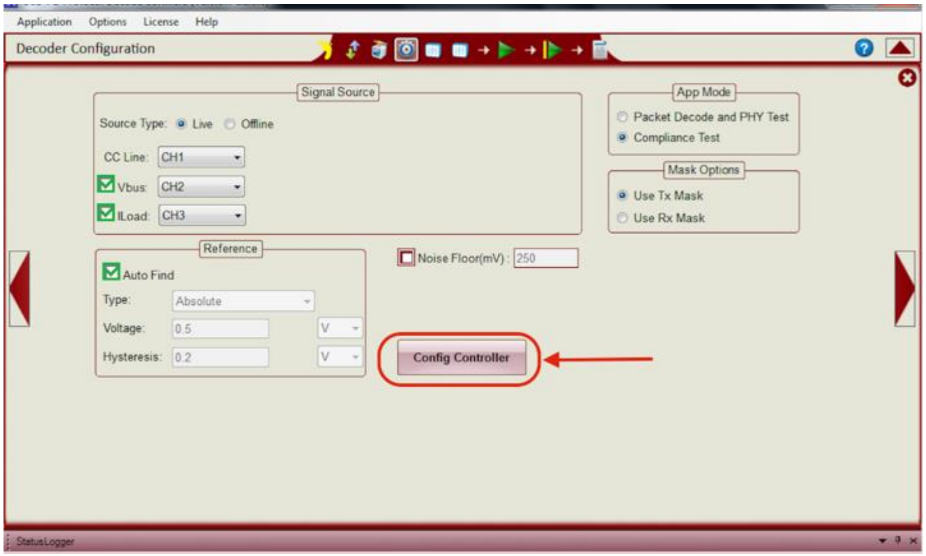


FIGURE 66: CONFIGURE CONTROLLER

10.1 Configuration Tab

Testing DUT for particular scenario can be performed using Configure controller. The functions that are provided in this utility by the application as explained below.

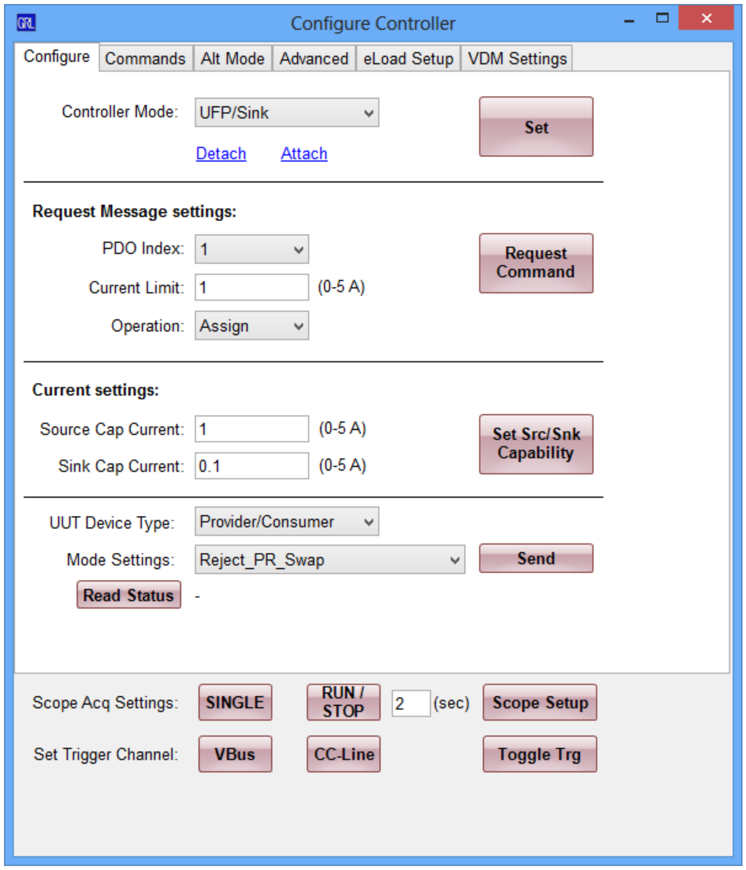


FIGURE 67: CONFIGURE CONTROLLER – CONFIGURE

1) Set Controller Mode. The Controller Mode drop down helps to set the controller's mode of operation.

1. Select the appropriate mode from below list:

   i) UFP/Sink
   ii) DFP/Source
   iii) DRP
   iv) Cable Tester

2. Click on Set button.

2) Request Message Settings. This field gives provision to assign the Request message settings which are sent from the Controller during PD Contract phase, and also to send a run-time Request message.

1. Assign PDO Index and Current limit. Choose either Assign or Send option in operation drop down to assign the Request message settings and to send the run-time command respectively.
2. Set Current Settings. This field helps to assign the current parameter value in Source and Sink Capability message send from Controller.

3) Select UUT device type.

1. Select the appropriate mode from below list:

   i) Consumer Only
   ii) Consumer/Provider

iii) Provider/Consumer
iv) Provider Only
v) Cable
vi) DRP
vii) Alternate mode

2. Click on Send button.

4) Mode Settings: The drop down list of this field can be used for configuring the Controller with any specific data for checking the behavior of DUT. For example, if the Controller should not accept the PR_SWAP command received from the DUT, it can be configured by selecting "Reject PR_SWAP" from drop down list, and can be applied to the Controller by pressing **Send** button. Table 1 shows details about how each command can be used.

TABLE 1: MODE SETTINGS

Mode Setting	Command Description
Reject PR_SWAP	If PR_SWAP command to be rejected
Send PR_SWAP	To initiate PR_SWAP command
Accept_PR_SWAP	Accept PR_SWAP
Send_Accept_PR_SWAP	Initiate PR_SWAP & Accept if PR_SWAP received
Send_PR_Swap_DONT_Send_First_PS_RDY	Initiate PR_SWAP & Don't Send PS_RDY
HARD_RESET	Send Hard Reset to DUT
CABLE_RESET	Send Cable Reset command to DUT
PHY_RESET	Reset PHY layer of the Controller
BIST Carrier Mode2	Send BIST Carrier Mode 2 command to DUT
Vbus_CAPACITANCE_DEFAULT	All capacitance is m
Vbus_CAPACITANCE_1MF	1uF Capacitance is applied on Vbus pin
Vbus_CAPACITANCE_10MF	10uF Capacitance is applied on Vbus pin
Vbus_CAPACITANCE_100MF	100uF Capacitance is applied on Vbus pin
RP_36K_900mA	Assert 36K Rp resistance
RP_12K_1500mA	Assert 12K Rp resistance
RP_4_7K_3000mA	Assert 4.7K Rp resistance
VDMConfig_TesterSource_ACK	Update Controller with the VDM Source Data
VDMConfig_TesterSink_ACK	Update Controller with the VDM Sink ACK Data
DPAltMode_Config	Configure controller with VDM message to respond to any DUT
DPAltMode_Macbook	Configure controller with VDM message to respond to Macbook
ERROR_Clear	Clear all the error inserted
ERROR_CRC_Before_Encode	Insert Corrupt CRC data before 4B/5B encoding while transmitting packet from Controller
ERROR_CRC_After_Encode	Insert Corrupt CRC data after 4B/5B encoding while transmitting packet from Controller
ERROR_Payload_Before_Encode	Insert Corrupt payload data before 4B/5B encoding while transmitting packet from Controller
ERROR_Payload_After_Encode	Insert Corrupt payload data after 4B/5B encoding while transmitting packet from Controller
Simulate Attach	Simulate Attaching Type-C connector without manual intervention
Simulate Detach	Simulate Detach of Type-C connector without manual intervention
VDM_ID_INIT	Configure the Controller with the VDM Discover ID initialize data
VDM_SVID_INIT	Configure the Controller with the VDM Discover SVID data

Mode Setting	Command Description
VDM_MODE_INIT	Configure the Controller with the VDM Discover Mode data
SOFT_RESET	Send Soft Reset to DUT
INIT_Src_Cap	Configure Controller with the Source Capability PDO
Vbus_OFF	Disconnect Vbus from the Type-C connector on the controller
Vbus_5V	Connect 5V Vbus supply to Type-C Connection on the controller
Vbus_12V	Connect 12V Vbus supply to Type-C Connection on the controller
Vbus_20V	Connect 20V Vbus supply to Type-C Connection on the controller
Set_Src_Cap1	Configure controller with the 5V, 900ma PDO
Set_Src_Cap2	Configure controller with the 12V, 1.5A PDO
Set_Src_Cap3	Configure controller with the 20V, 3.0A PDO
Enable eLoad Mo	Enable E-Load Connected to the Controller
Disable eLoad Mo	Disable E-Load Connected to the Controller
Enable VDM	Enable VDM, So controller will respond to VDM messages
Disable VDM	Disable VDM, So controller will respond with NAK for VDM messages
Reject_DR_SWAP	Configure controller to reject DR swap if received from DUT
Accept_DR_SWAP	Configure controller to Accept DR swap if received from DUT
Send_Accept_DR_SWAP	Send DR_SWAP or Accept DR_SWAP
Tester_Reset	Reset the Controller

10.2 Commands Tab

The Command tab gives provision to send the run-time messages from Controller after successful PD Contract between Controller and connected device. Choose the required message type given in Figure 68 and click on Send button to send the run-time messages from Controller.

The commands that can be sent from this tab for observing the behavior of the DUT are as follows:

1) Set SOP Type. The SOP Type drop down allows user to select the SOP type in the message sent from Controller. It includes SOP, SOP’ and SOP”.
2) Set SVID. The SVID field allows user to set the SVID value of the mode related messages sent from Controller. VDM Mode Initiator, VDM Enter Mode Initiator and VDM Exit mode Initiator are mode related messages.
3) Power, Data and Vconn swap can initiate by selecting appropriate radio button in the command tab.
4) Reset such as Hard Reset, Cable Reset and Soft reset can be sent from controller by selecting the radio button in the command tab.

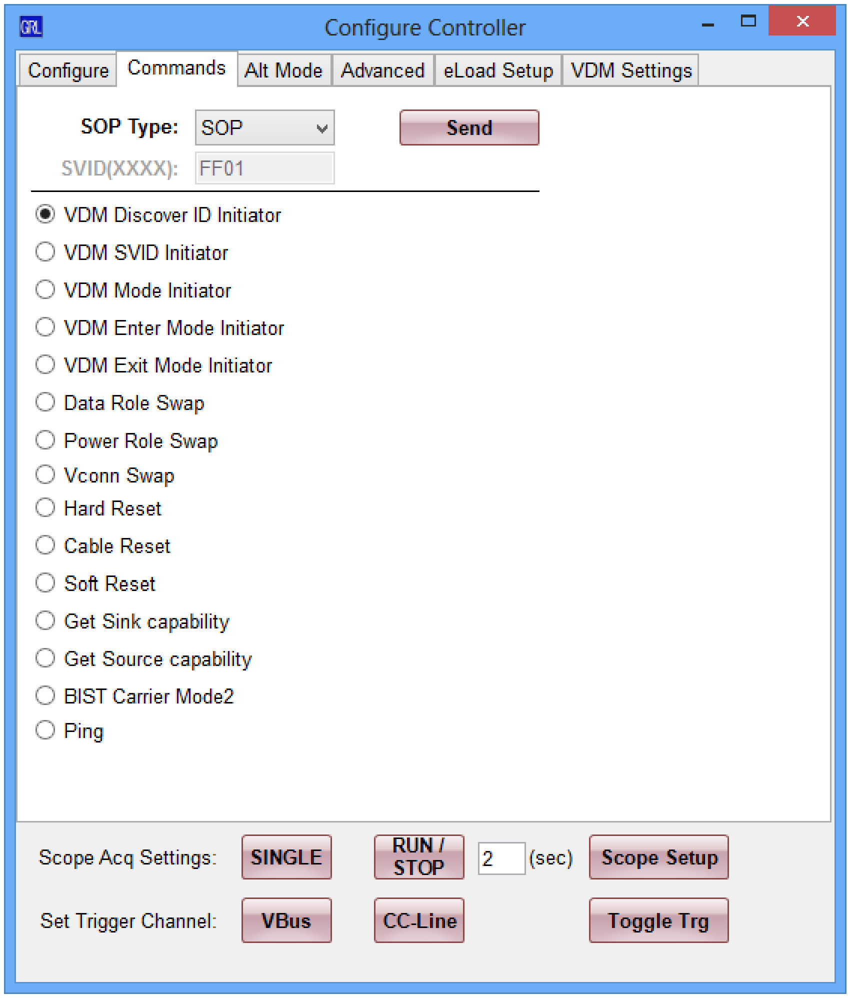


FIGURE 68. CONFIGURE CONTROLLER- COMMANDS TAB

5) Capability command like Get Sink Capability and Source capability can be sent from this tab.
6) Ping command also can be sent to DUT by selecting the ping radio button.
7) After selecting the required command as mentioned above, need to send button for sending command

10.3 Alt Mode Tab

The feature in this tab is used for testing DUT in the Alternate Mode. Refer to Section 6 for more detailed description of what configuration GRL-USB-PD-C1 can support and test.

10.4 Advanced Tab

The Advanced Tab in the Configure Controller has advance feature such as managing delay, Swap and Trigger as shown in the figure below.

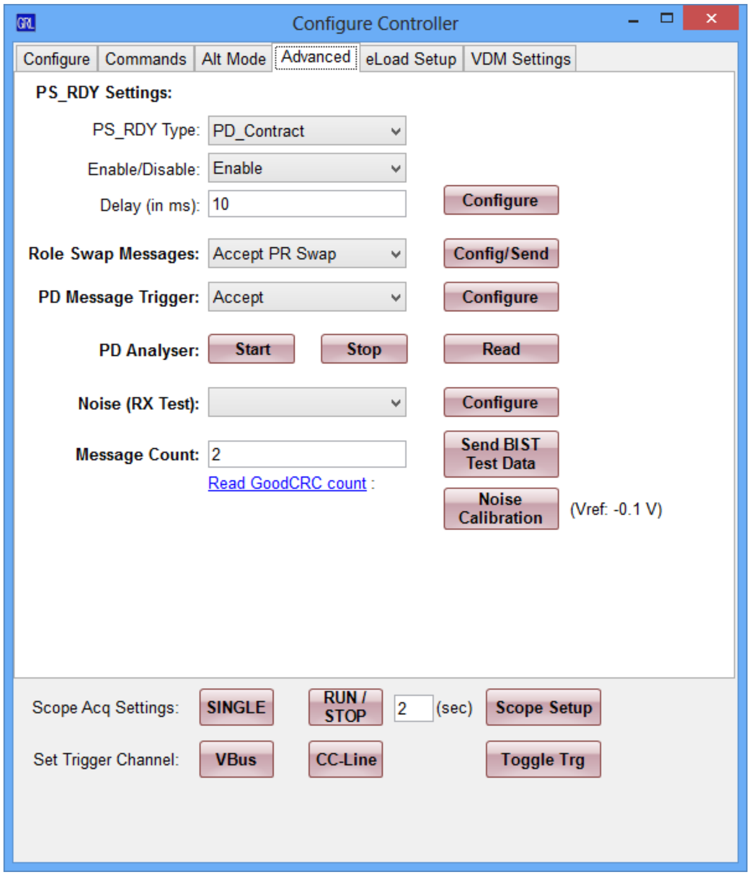


FIGURE 69: CONFIGURE CONTROLLER- ADVANCED TAB

1) PS_RDY Settings: This feature used when the user wants to have controlled PS_RDY message being sent during PD contract or during PR_SWAP. PS_RDY can be configured to be sent, or not sent, by selecting Enable/Disable dropdown list. For enabled PS_RDY, a sequence delay can be inserted to ensure that the Controller is sending PS_RDY only after the delay configured in the Delay field has expired.
2) Role Swap Messages: This field is used to test the Role Swap handling behavior, to change whether to select Accept Role swap or Reject or Send Role swap messages. Using these settings, the DUT can be tested to see how it responds based on the configuration.
3) PD Message Trigger: This feature is used for triggering a pulse from the front panel connector before any of the listed messages in the dropdown list are sent from the Controller.

4) PD Analyzer: This is used for capturing CC Line message transactions, without probing the CC Line on the Scope.

5) Noise (RX Test): This is used for disabling or enabling any one of 4 different noise features supported by the Controller.

6) Message Count: This field is used to set number of BIST Test data messages which need to be sent from the Controller upon clicking Send BIST Test Data.

7) Read GoodCRC Count: Clicking this will give total number of GoodCRC received from DUT for the actual sent BIST Test Data, after setting Message count and sending BIST Test Data.

8) Noise Calibration: This is used to calibrate the voltage reference of the Noise board. This should be done whenever the Controller is used for the first time. The calibrated voltage reference value of the connected Controller will be retained in the software. Upon changing the Controller, the user is recommended to calibrate the new Controller again.

10.5 eLoad Setup Tab

eLoad setup tab in the configure controller is used for setting the eLoad current and turning ON or Off of eLoad.

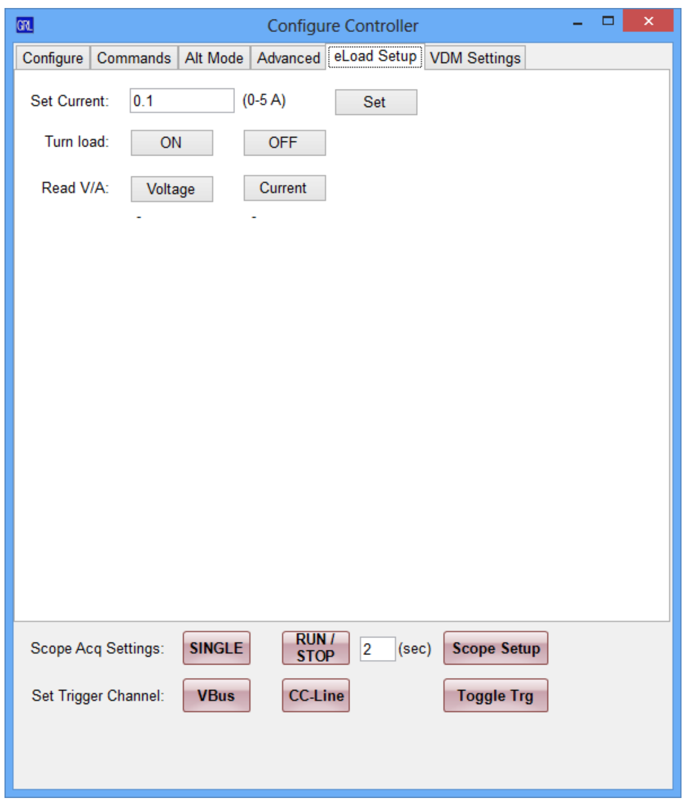


FIGURE 70: CONFIGURE CONTROLLER- ELOAD SETUP TAB

1) Set Current: This field used to set the current that an eLoad can draw from the DUT.

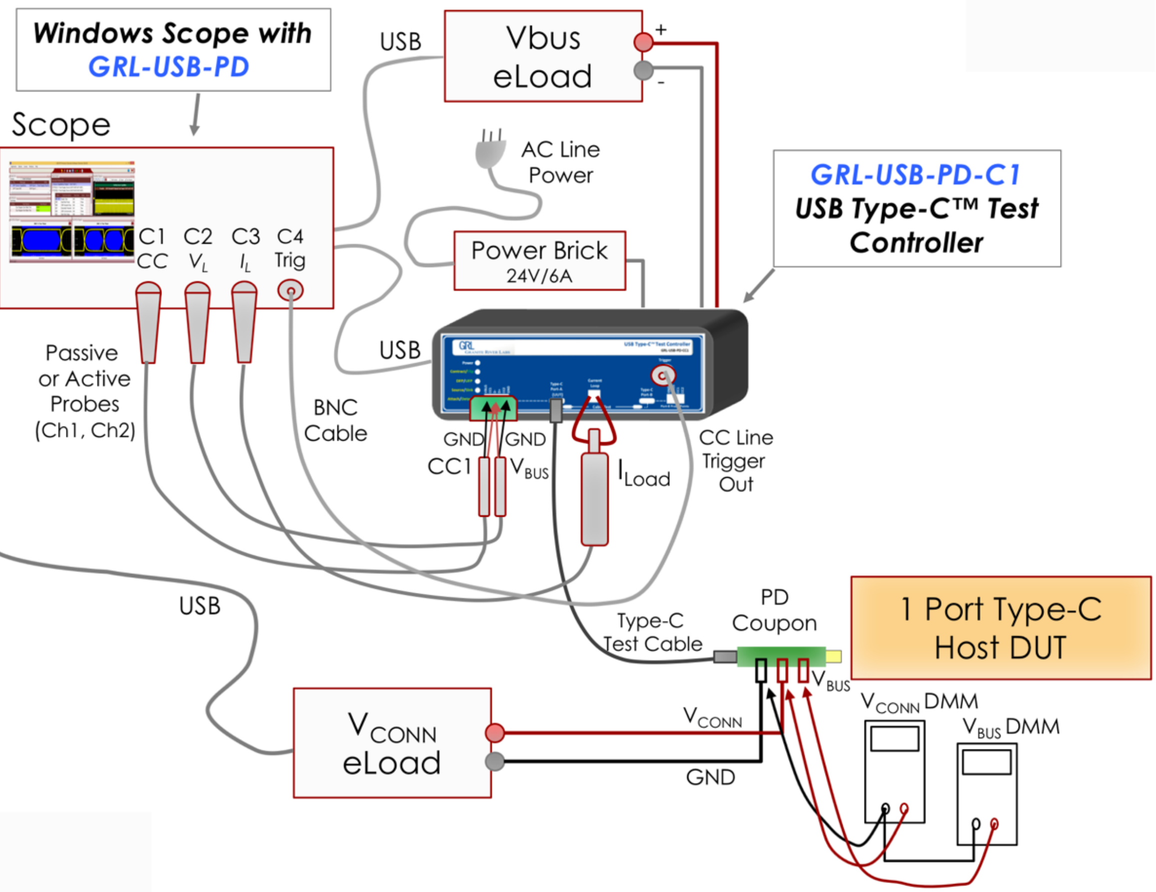
2) Turn load: Used to Turn On or off the eLoad.

3) Read V/A: Used to read the configured Voltage and Current of the eLoad.

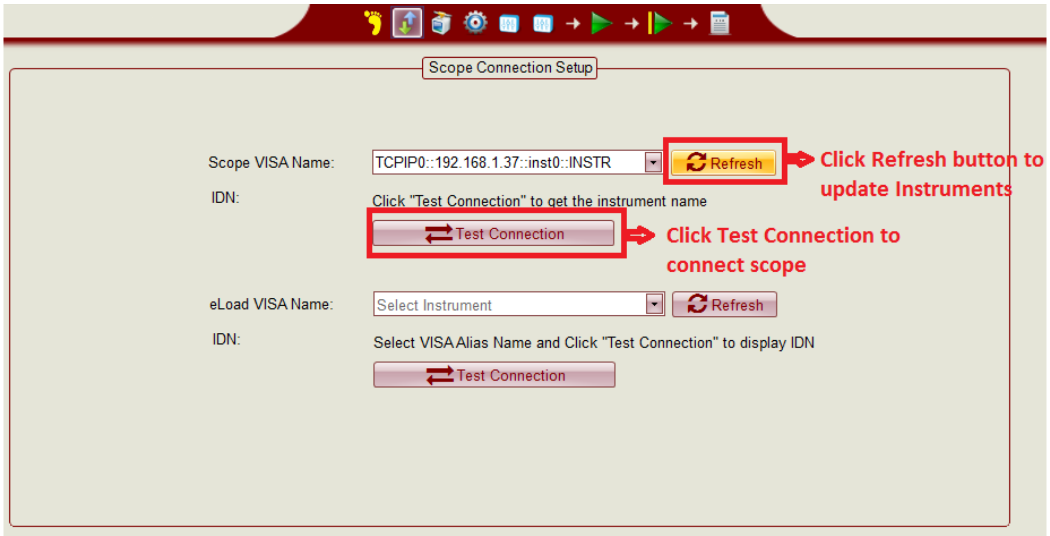
10.6 Power Testing Tab

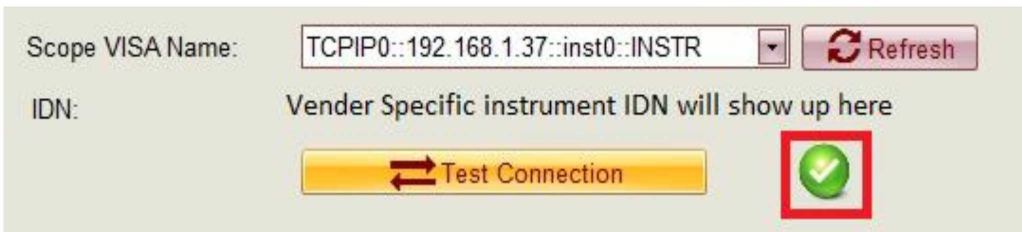
Power Test is required for the Multiple Port Devices. Based on the device capabilities for each power profile the configured power will be loaded from VBus and a constant of 1.5 Watt power will be loaded from Vconn. In case of Multi-port device Vconn and Vbus power will be loaded simultaneously from all the power ports.

Step 1: Make sure that the setup for power testing is as shown below.



Step2: Click Refresh button in Oscilloscope Configuration panel and connect Scope as shown in below figure.



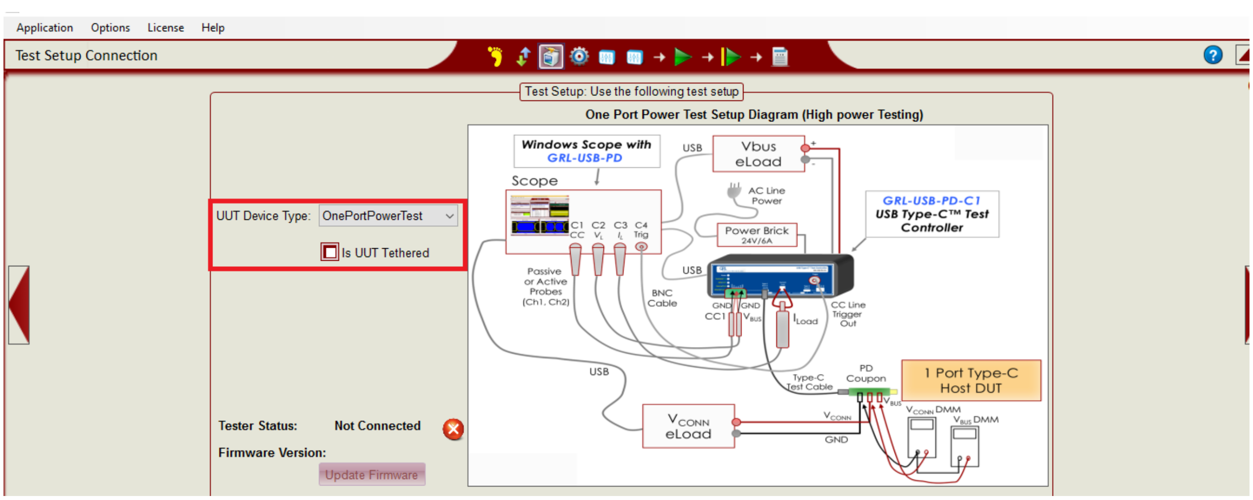


Step3: Select UUT device type as OnePortPowerTest in Test Setup connection panel.

Note:

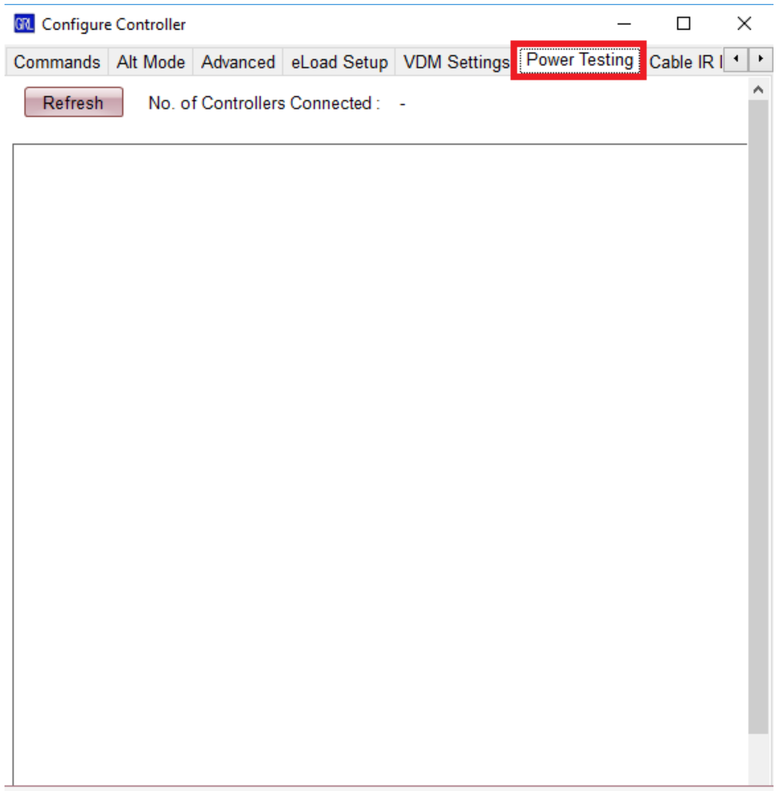
For single- Port Power Testing select OnePortPowerTest,

For dual- Port Power Testing select TwoPortPowerTest.

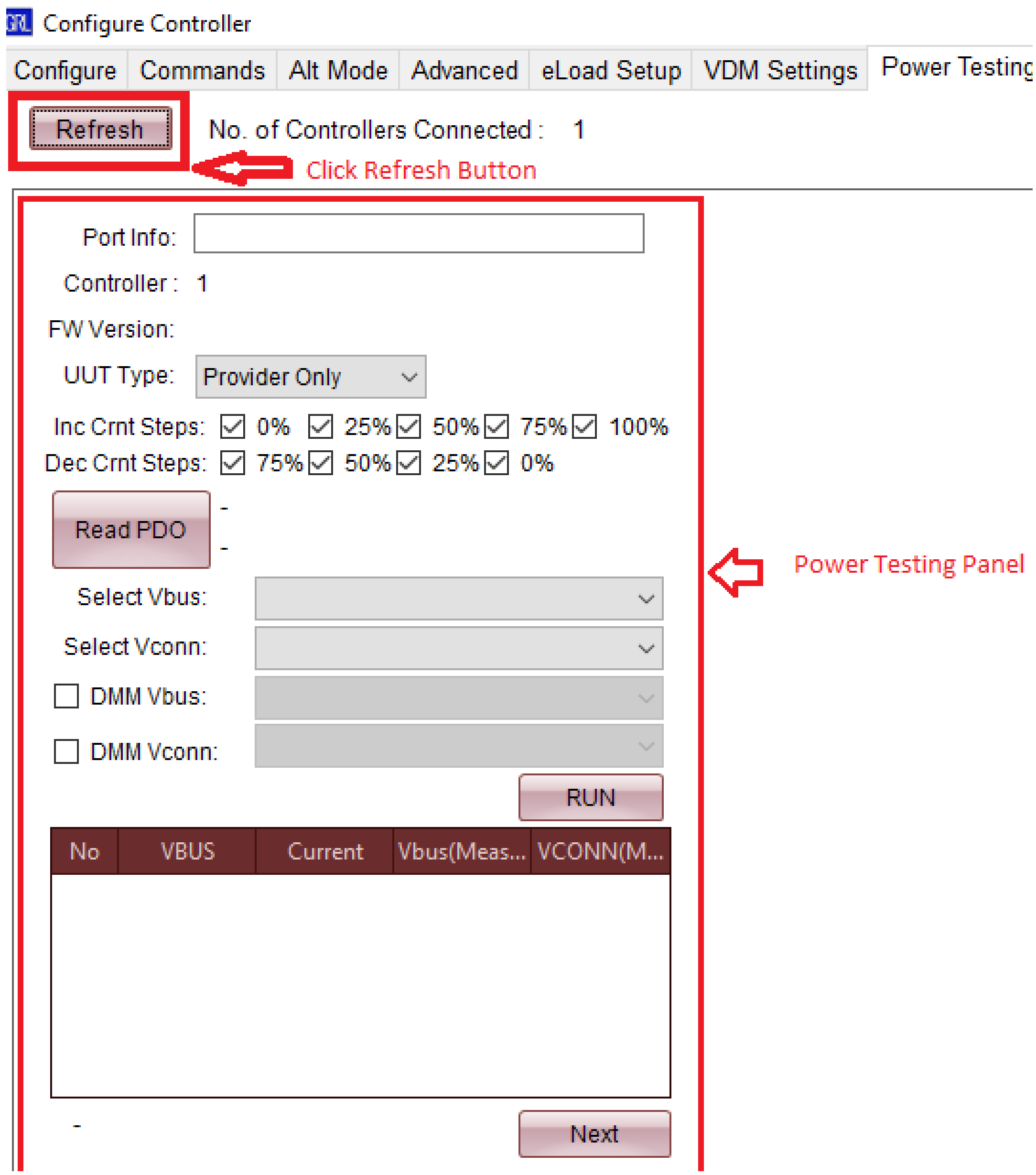


Step4: Open Config Controller Window in Decoder Configuration Tab.

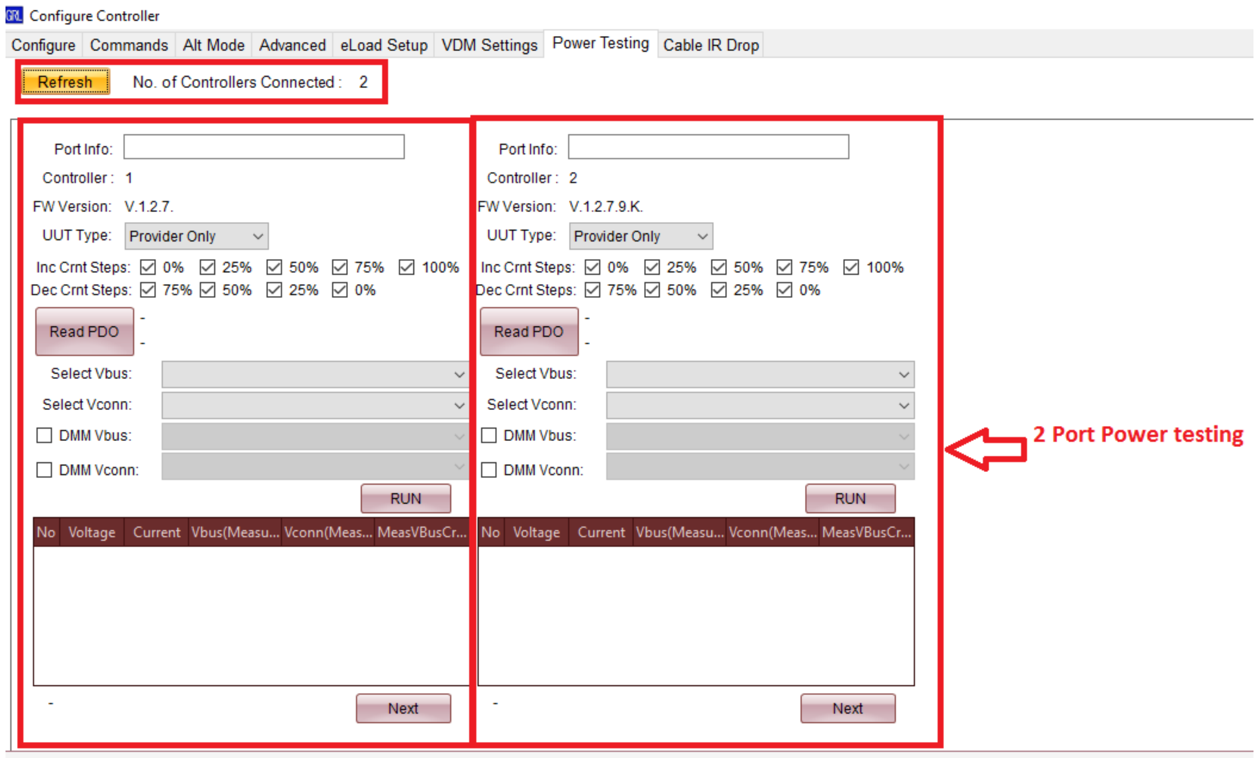
Click on Refresh Button in the Power Testing Tab.



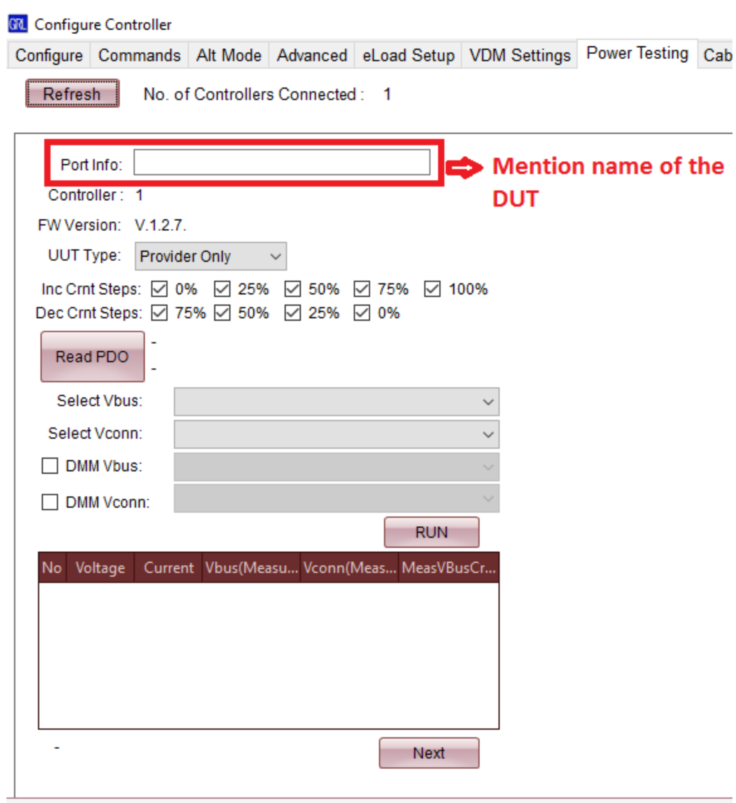
The Power Testing Tab values will be displayed based on the number of controllers connected. For single port power testing one controller is connected and panel will get updated as shown in below figure.



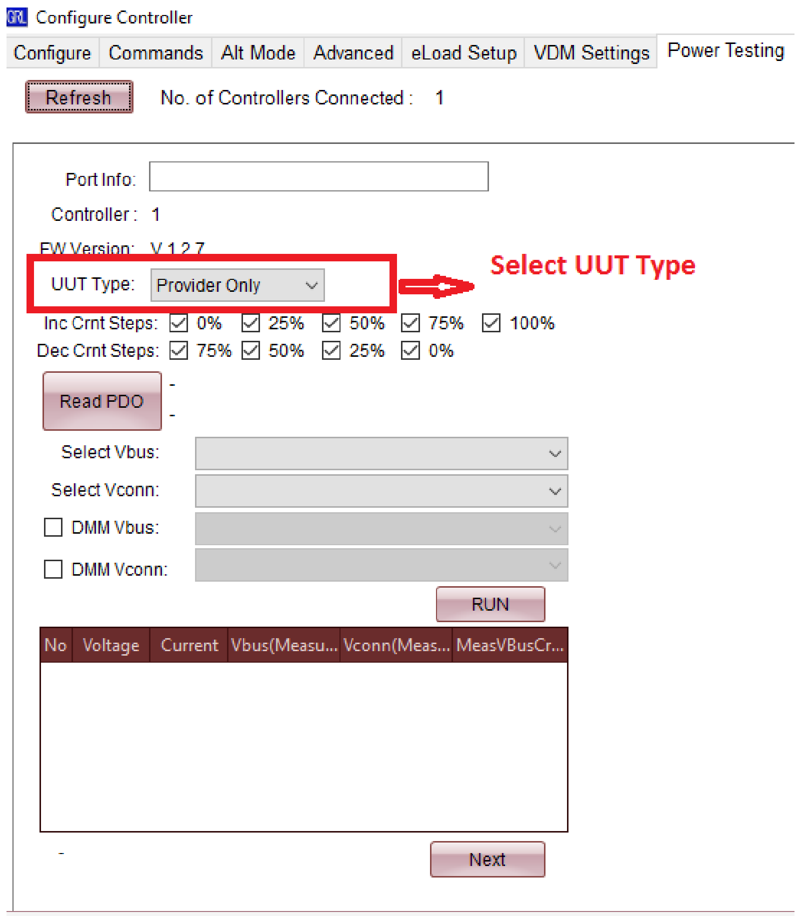
For dual-Port Power testing two controllers must be connected. The Panels are updated after clicking Refresh button.



Step 6: Enter the DUT name as Port Information.



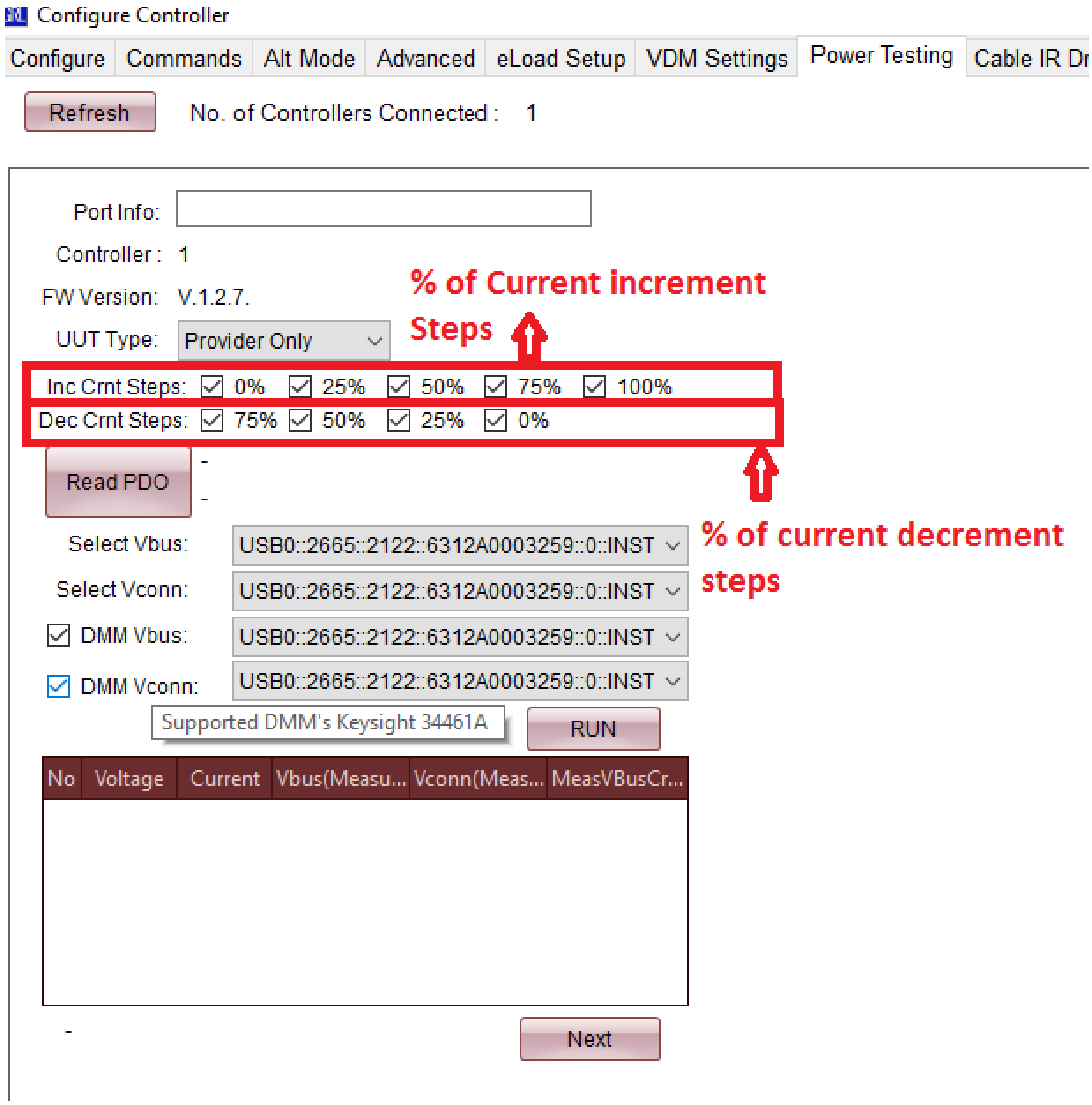
Step 7: Select UUT Type in the UUT drop down box.



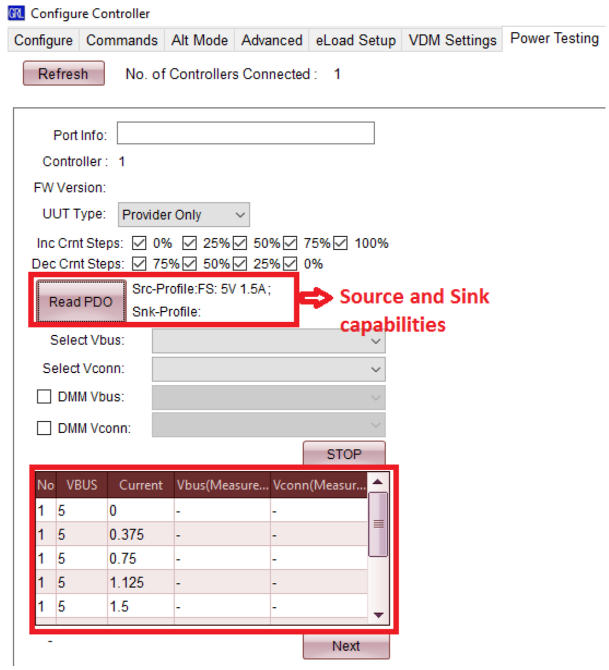
Step 8: Select Check boxes with respect to Current increment and decrement steps.

For example if 0% and 100% are selected as incremental steps the PDO Object's minimum and maximum current values would be altered to 0 % and 100% of PD Object's current value.

If 0%, 50% and 100% are selected as incremental steps then PD Object's current incremental steps will be minimum , half of the PD Object's current and maximum current.

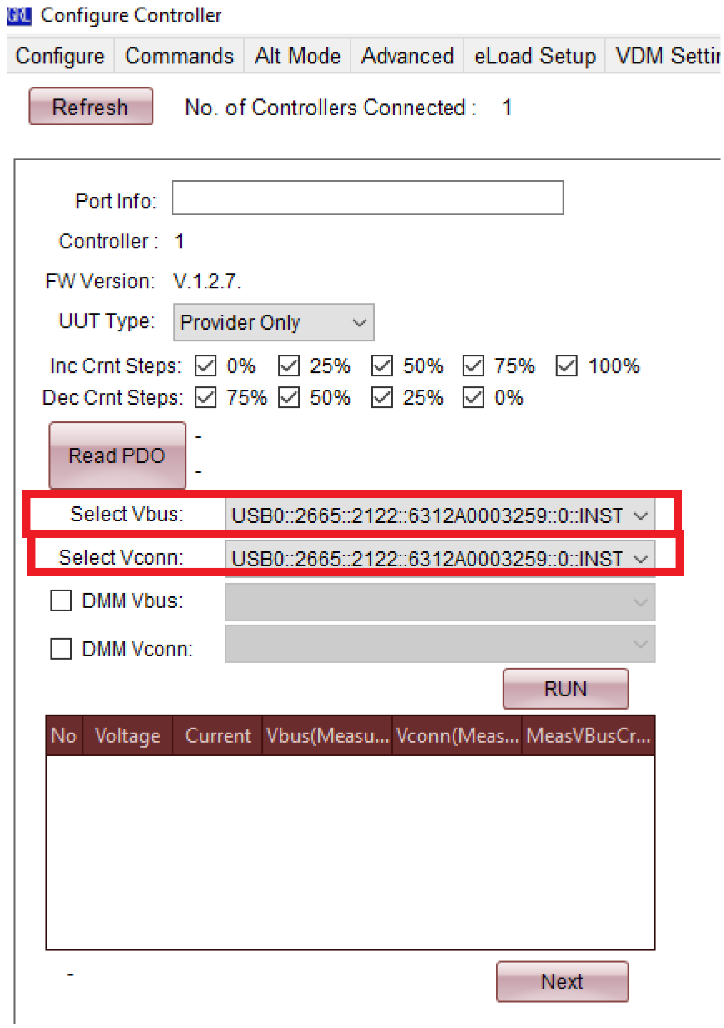


Step 9: Click Read PDO button as shown in below figure.

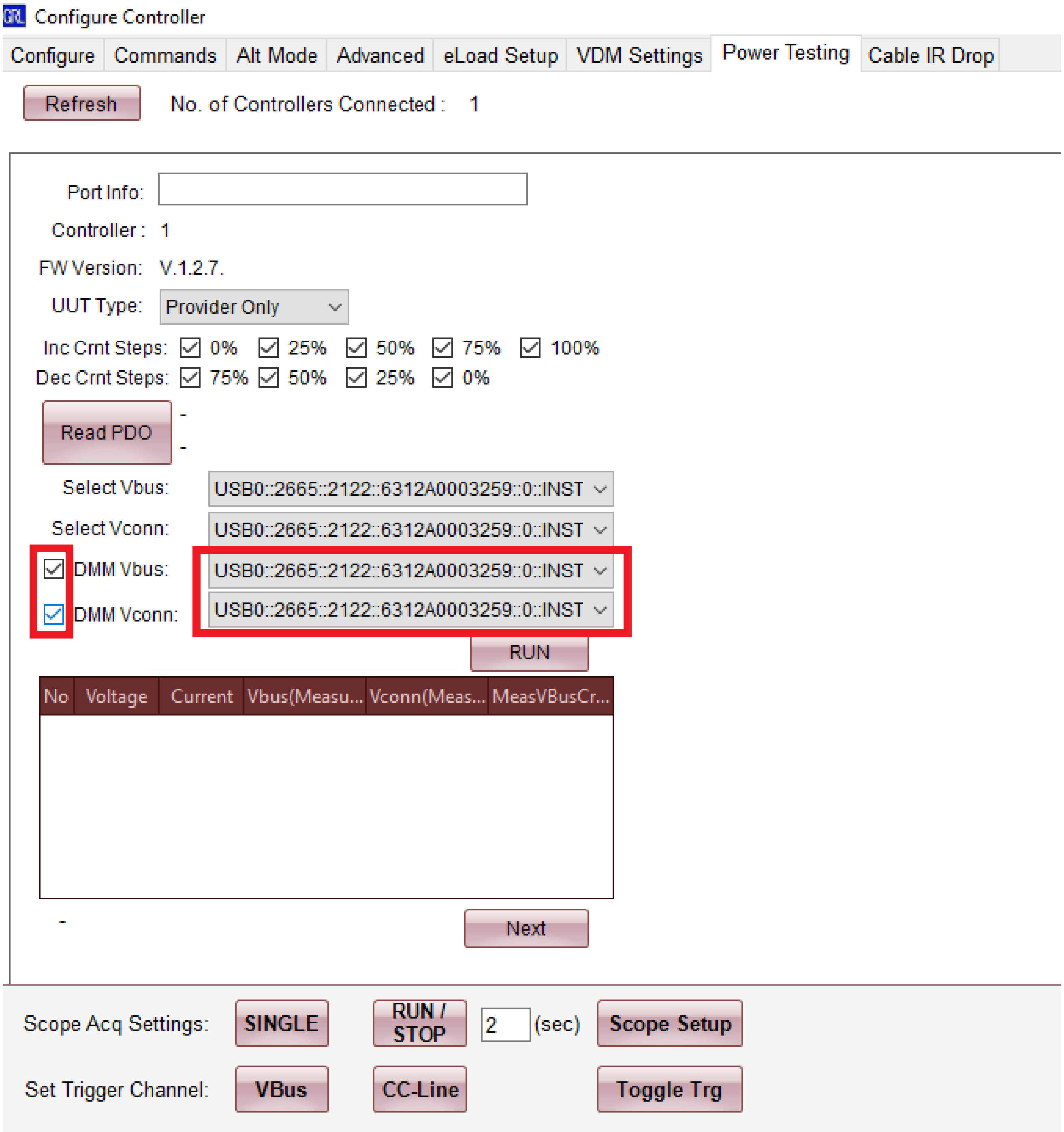


Step 10: Select eLoad connected to Vbus in ‘Select Vbus’ drop- down list.

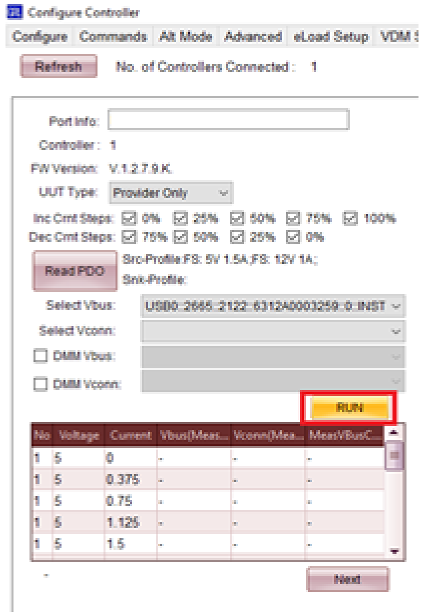
Select eLoad connected to Vconn in ‘Select Vconn’ drop-down list. As shown in below figure.



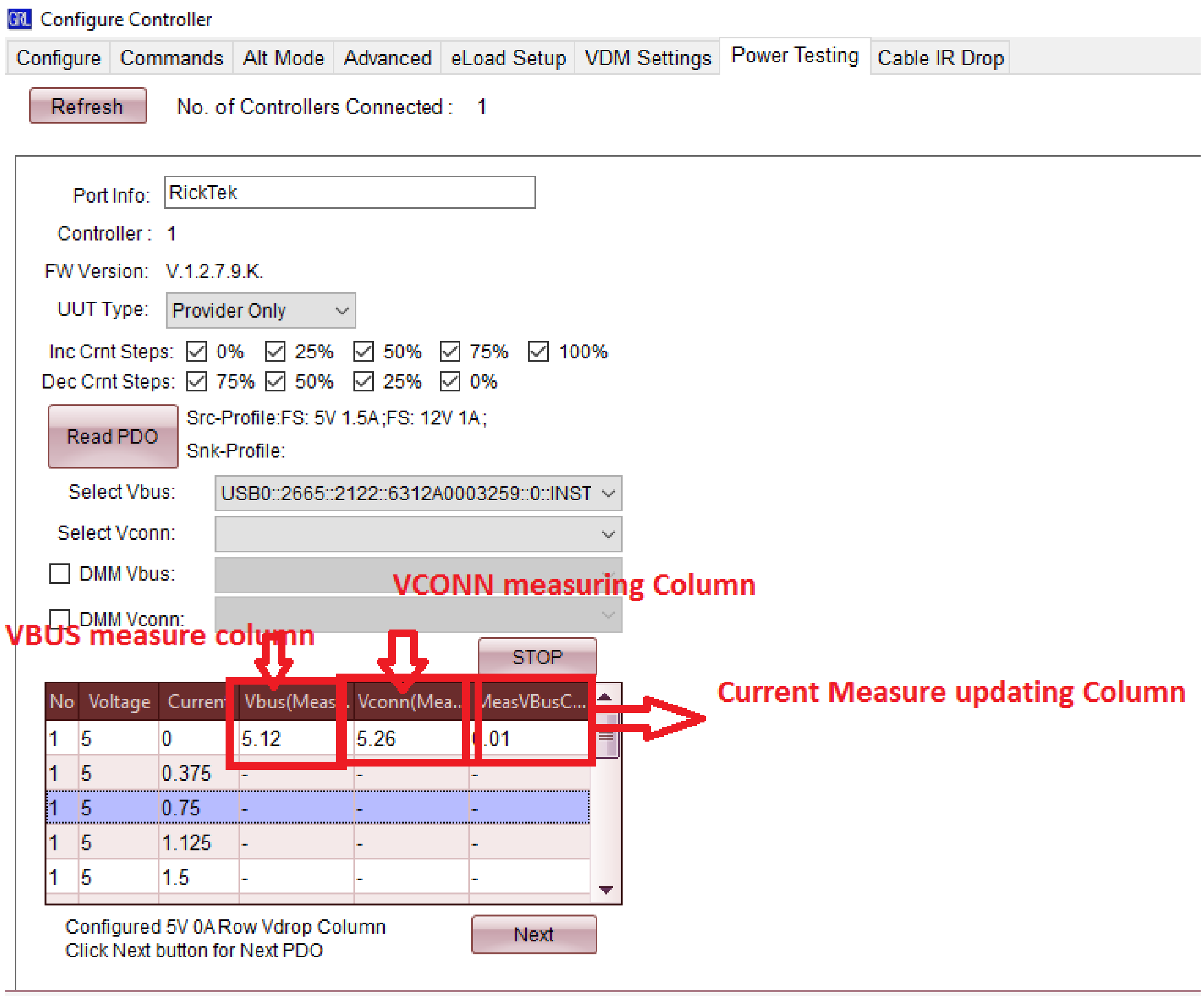
Step 11: If Digital Millimeter is connected for Vbus and Vconn, select checkbox of DMM for Vbus and Vconn and set the DMM's VISA identifier respectively. As shown in below figure.



Step12: After Selecting eLoad for Vbus and Vconn, Select the DMM(Digital Multi Meter) for Vbus and Vconn. Click Run Button.

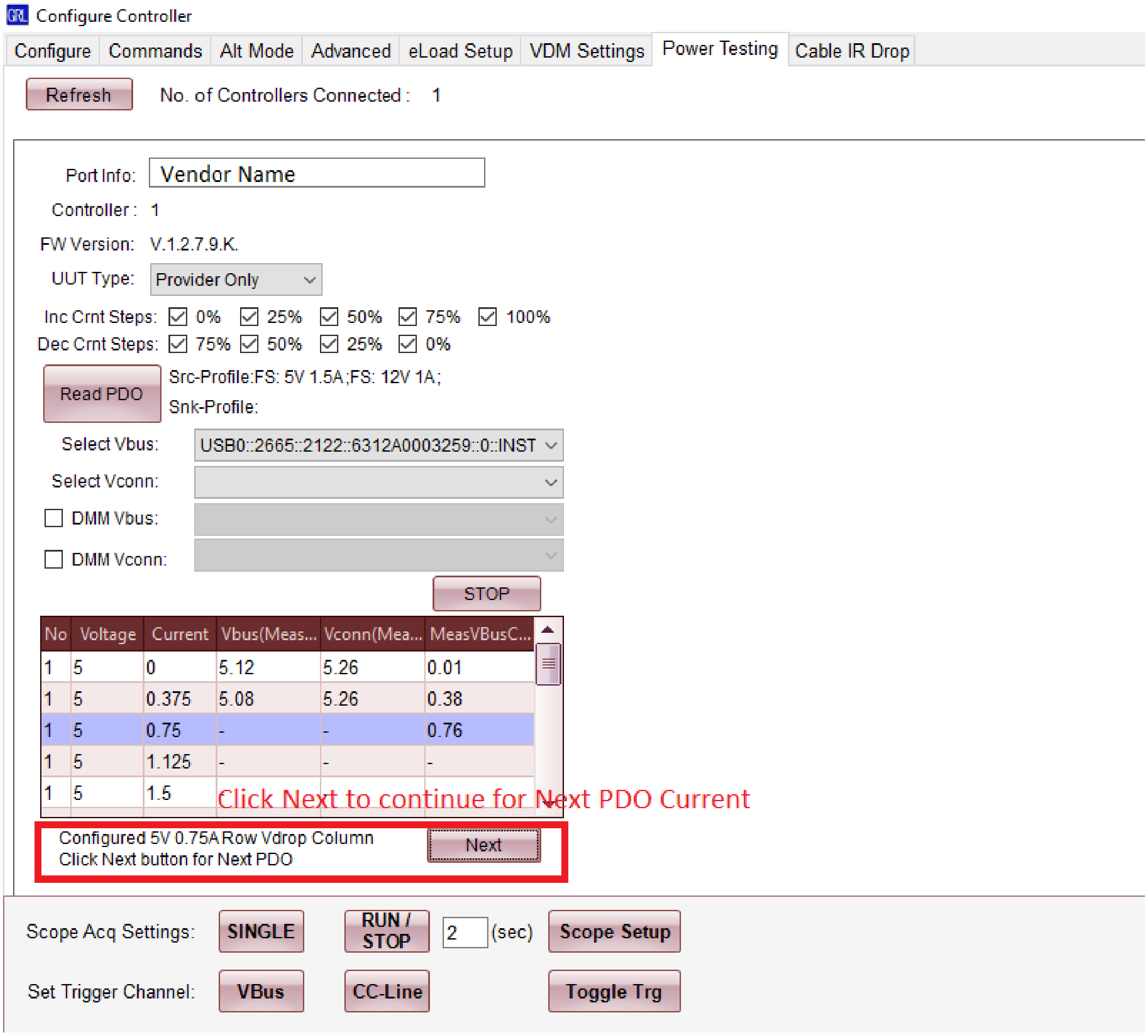


Step 13: In the case where DMM is used to measure Vbus and Vconn, the measured values are displayed in Vbus column and Vconn column as shown below.

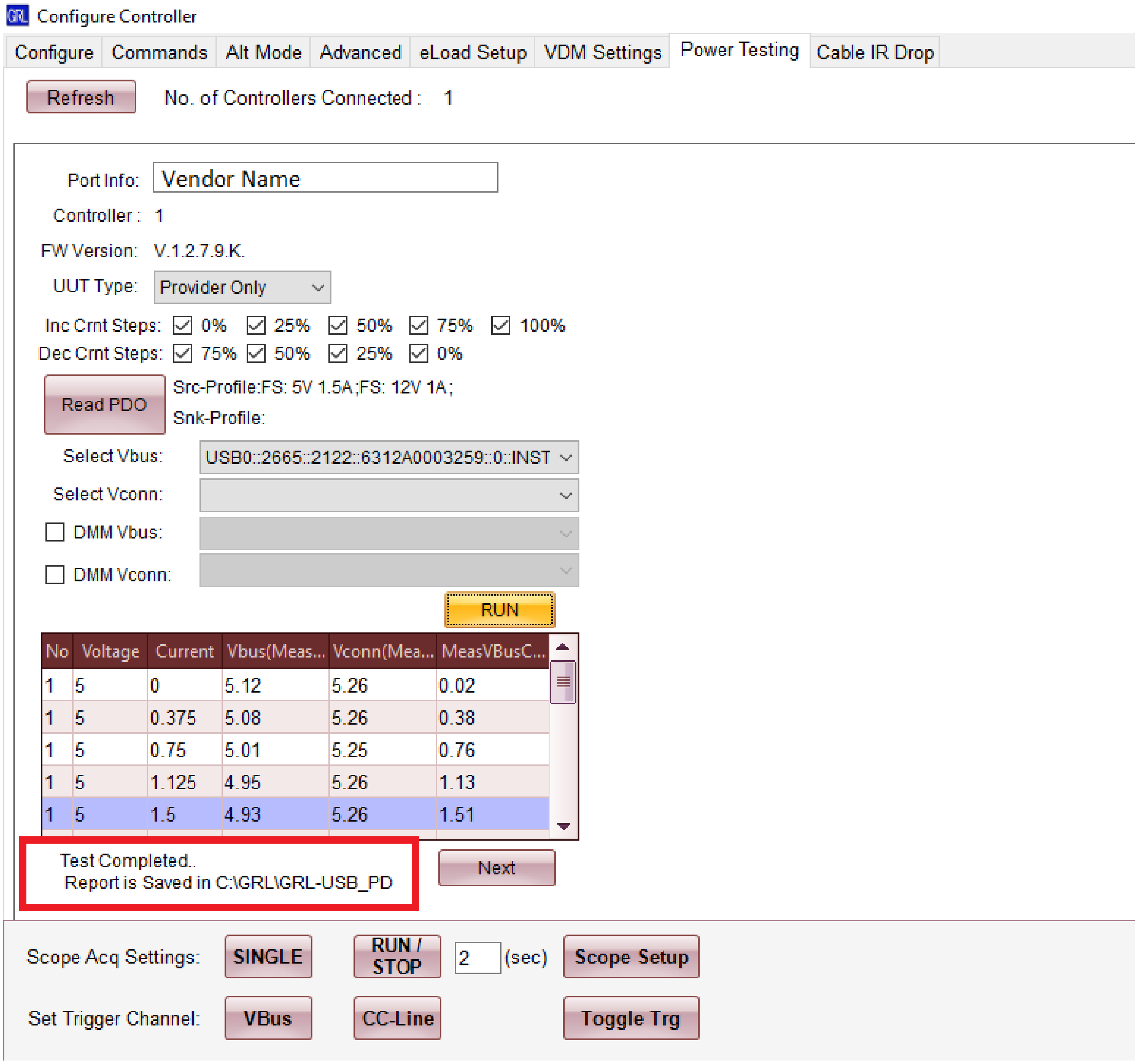


Note: In the case where DMM is not connected for Vbus or Vconn then we need to measure voltage using multi-meter or from scope and update values in respective column.

Step14: After updating the Vbus and Vconn values, Click Next button as shown in Figure.



Step 15: After measuring all the current values for all the PDO's, check the report in C:\GRL\GRL-USB_PD\ based on DUT's name and current timing.

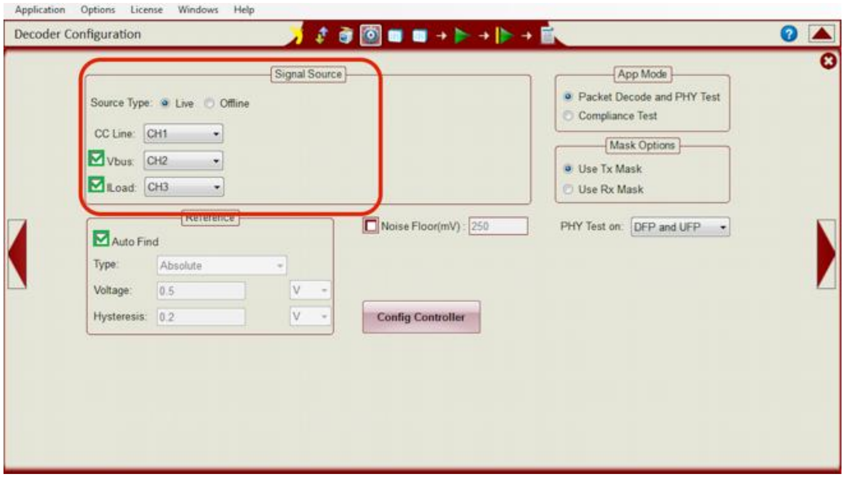


11 Appendix C: Packet Decode and PHY Testing

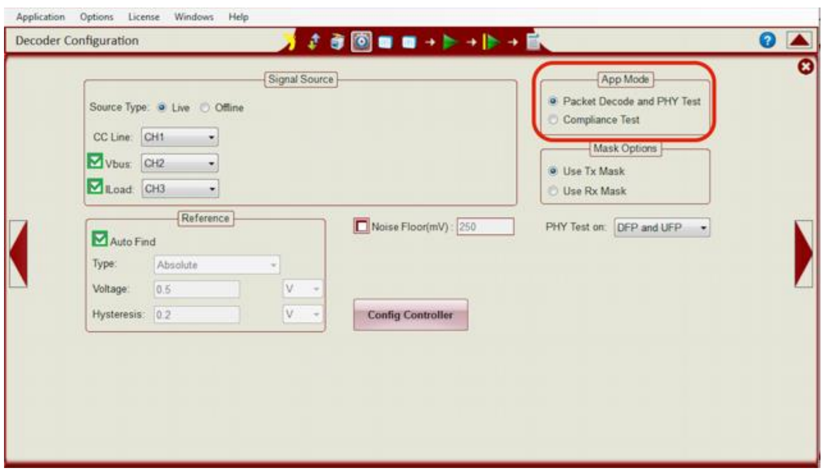
11.1 Decoding and Analyzing a Captured Waveform using GRL-USB-PD Software

This section shows how to use GRL-USB-PD Software to decode a packets and using the Signal View window to analyze a waveform. This is done by decoding the waveform after it is captured on the scope. This can be done on a live waveform of saved waveform using the same procedure. It is often useful to decode and debug physical layer signaling and timing issues.

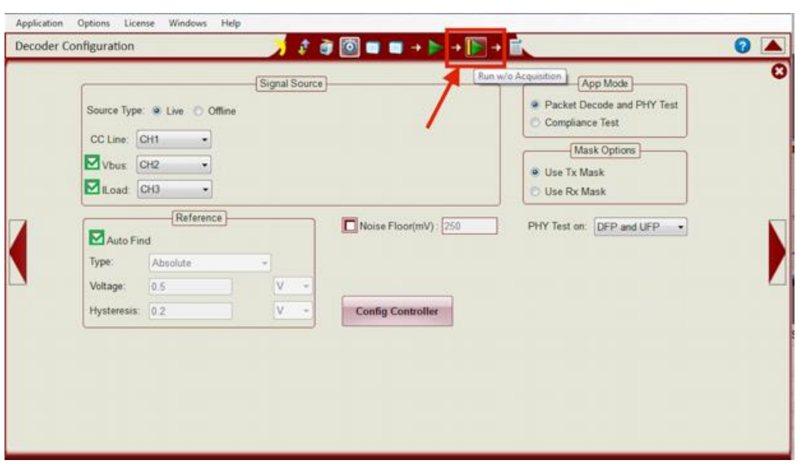
1) Capture the CC line signal on Channel 1 using the methodology outlined in Section 4 or some other means. The signal captured signal can be **live** on the Scope or recalled by selecting **Offline** and navigating to the desired waveform.



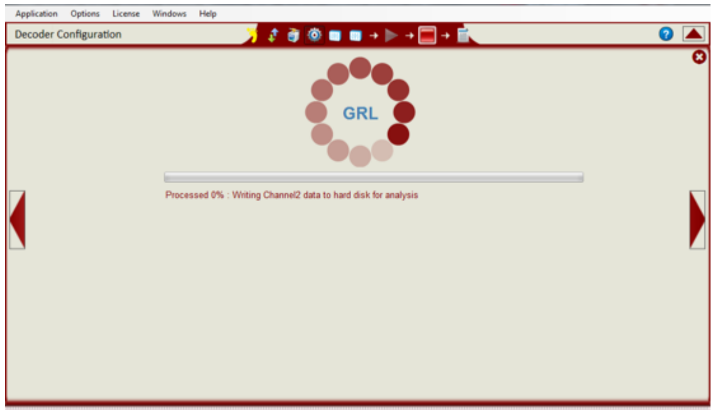
2) Select Packet Decode and PHY Test selection under App Mode.



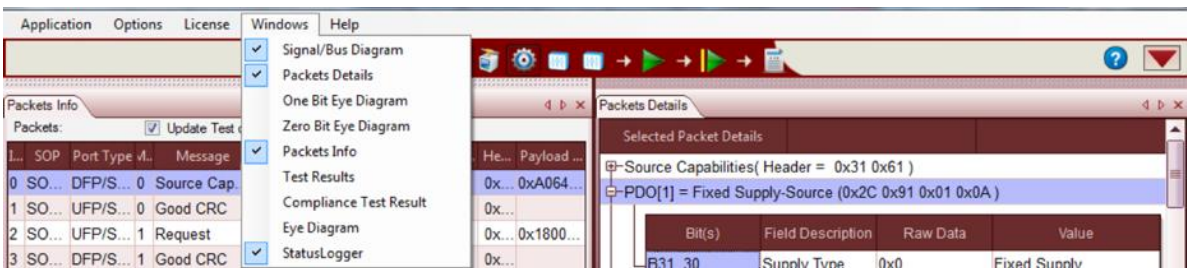
3) Press the Run w/o Acquisition button.



4) This will decode and analyze the waveform that has been captured on Ch1 or the Offline waveform selected.



5) One the analysis is complete; configure the windows as follows to optimize for Protocol Decoding. Go to the Windows menu and select **Signal/Bus Diagram**, **Packets Decode and Packets Info**.

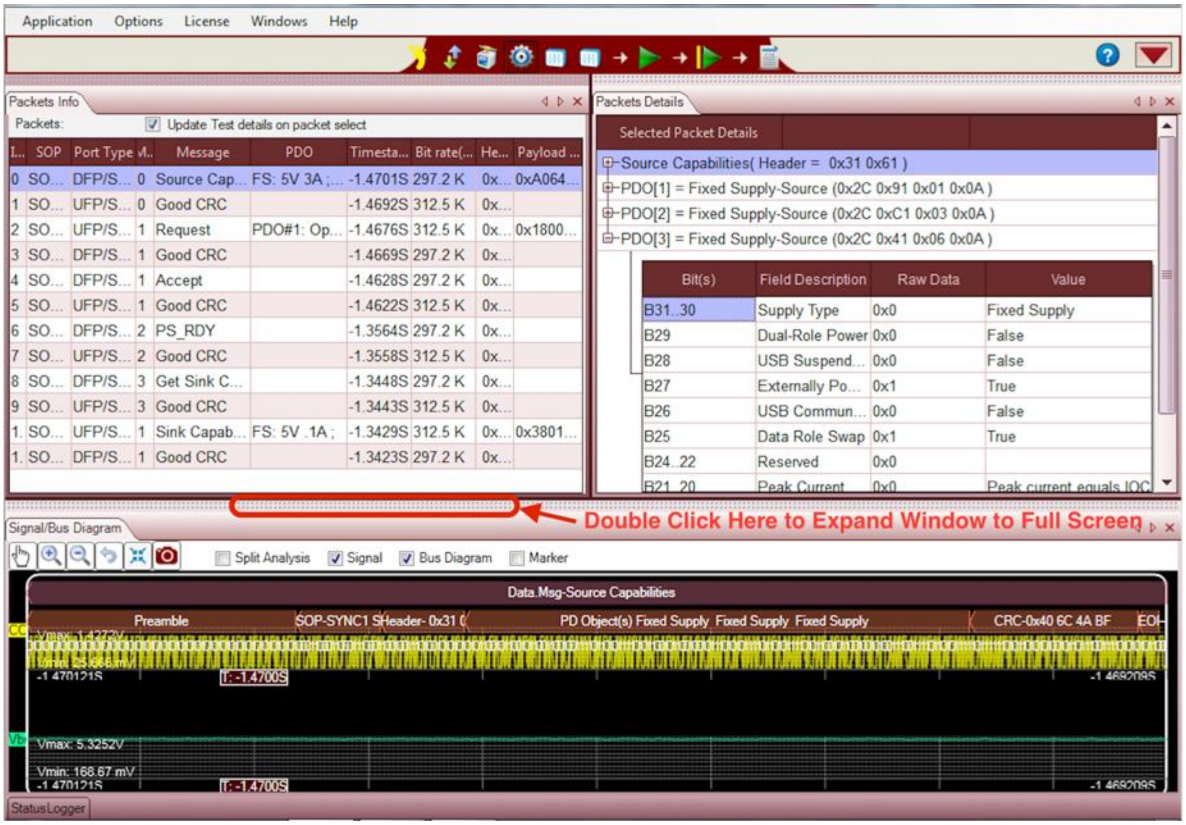


6) The resulting display will look like the following.

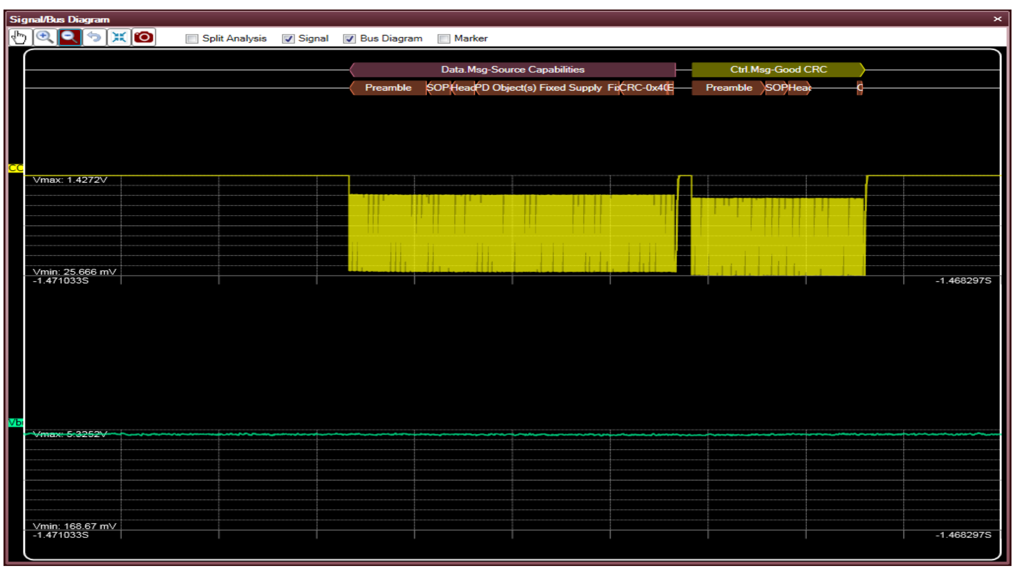
The Packets Info Window – shows all the packets (Byte Level) that have been captured in the acquisition. Click on the Packet you would like to analyze further.

The Packets Details Window – Shows detailed (Bit Level) decode of the selected packet, for example, the PDO information of the selected Source Capabilities Packet.

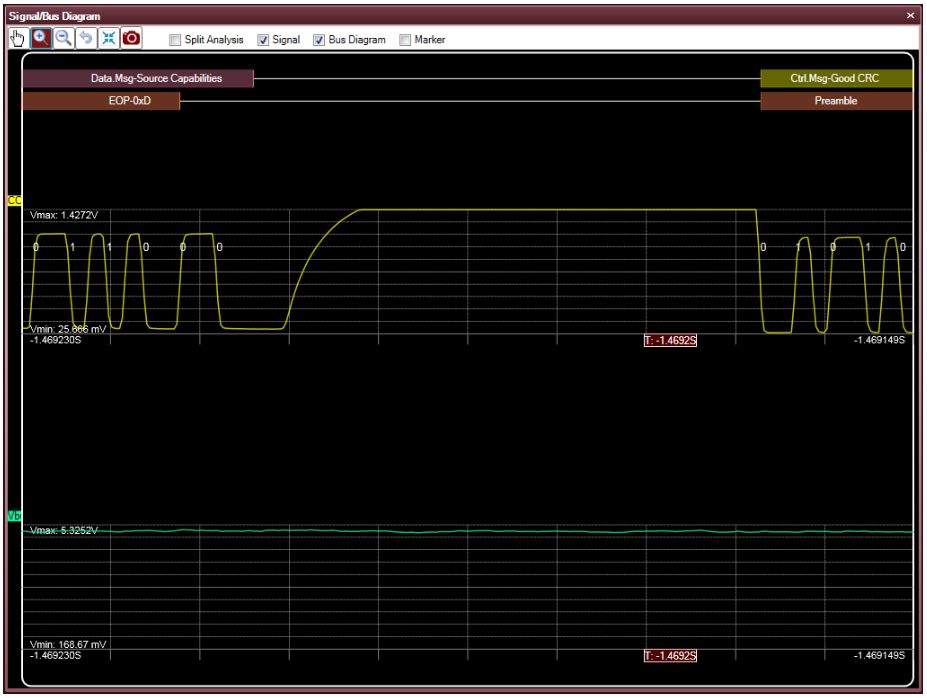
Signal/Bus Diagram – Shows the waveform of the captured signals and the BMC Decoded packet information. This can be used for debug purposes.



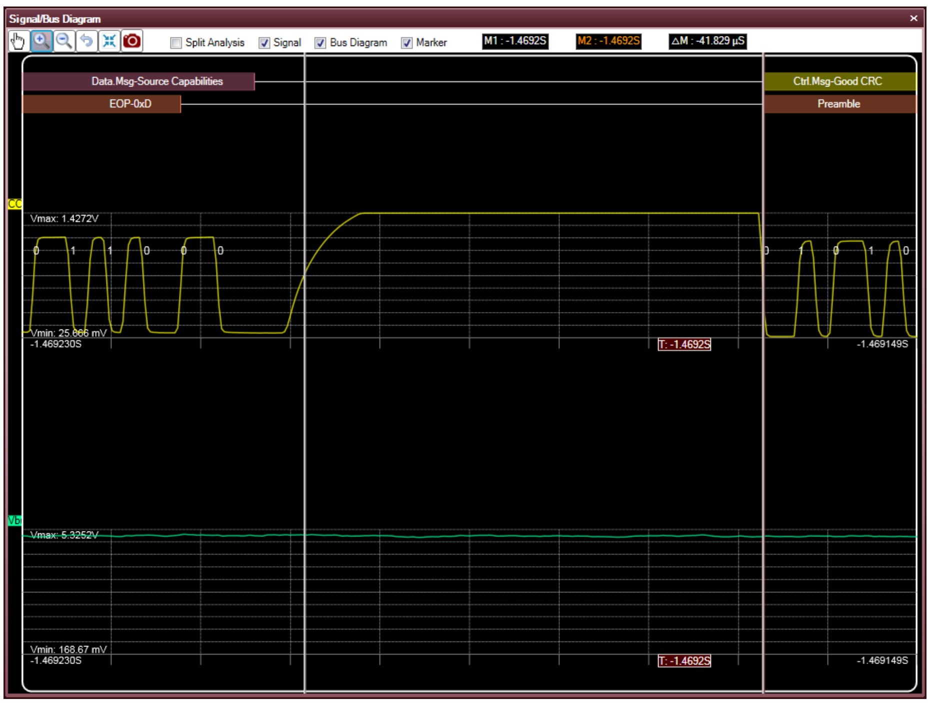
7) To Expend the Signal/Bus Diagram to full screen, double click on the double bars on the top of the Window. This 'un-docks' the window to full screen.



8) Zoom can be used to zoom into waveform detail and how it relates to the PD messaging.

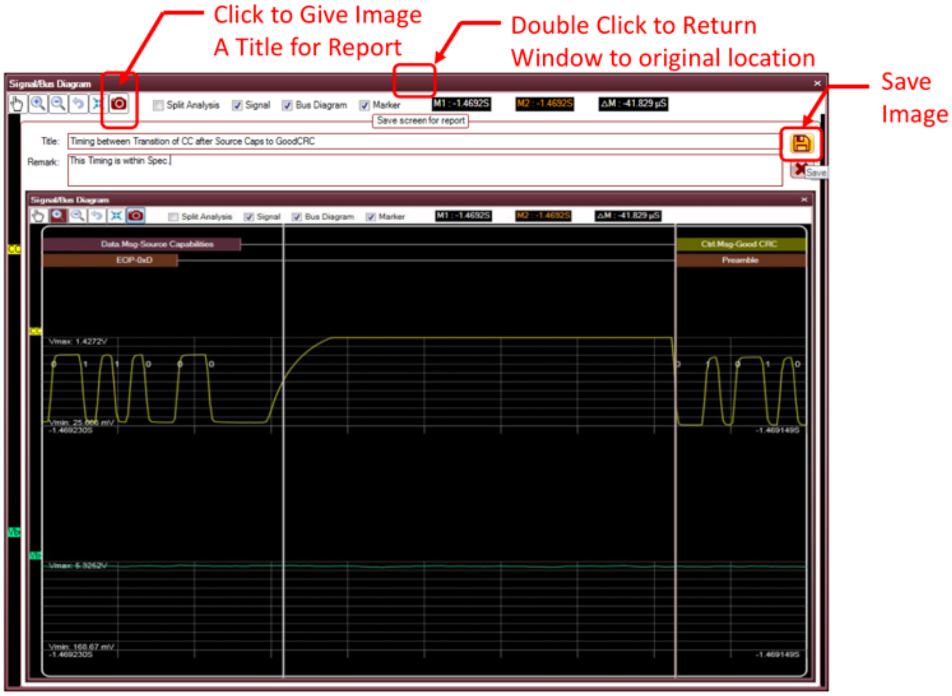


9) Markers can be used to make timing measurements on the view.

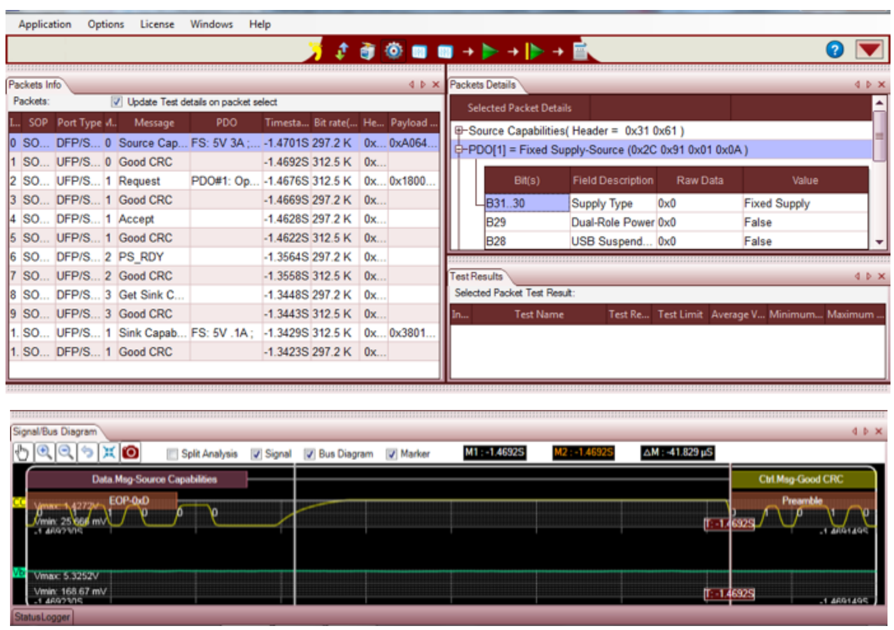


10) Select the Camera icon to give the image a **Title** and **Remark** for a report.

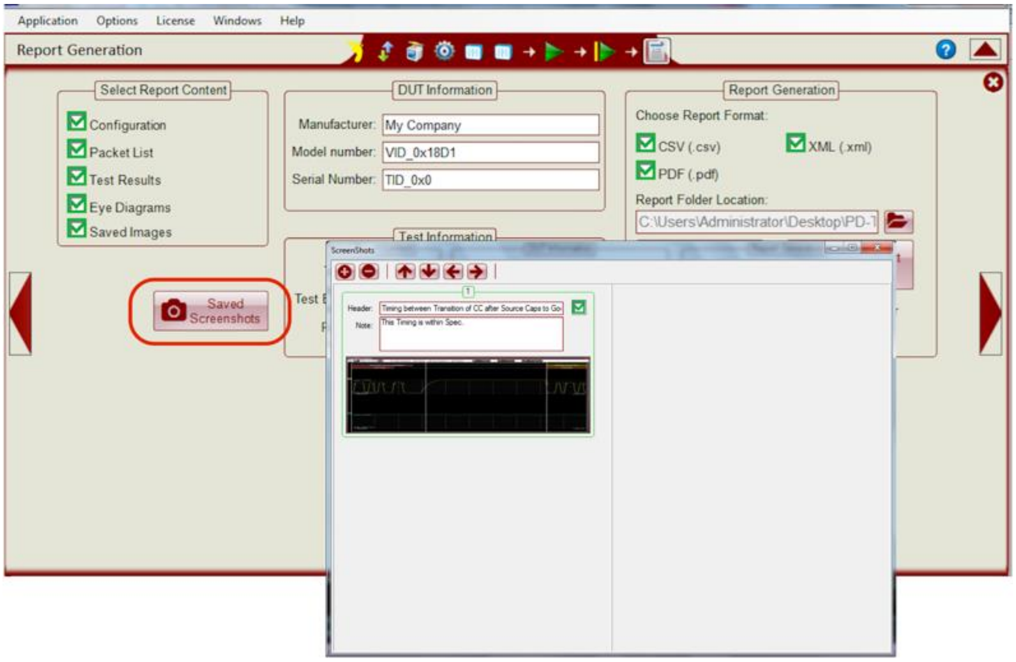
11) Press the floppy drive icon to **save** the Image.



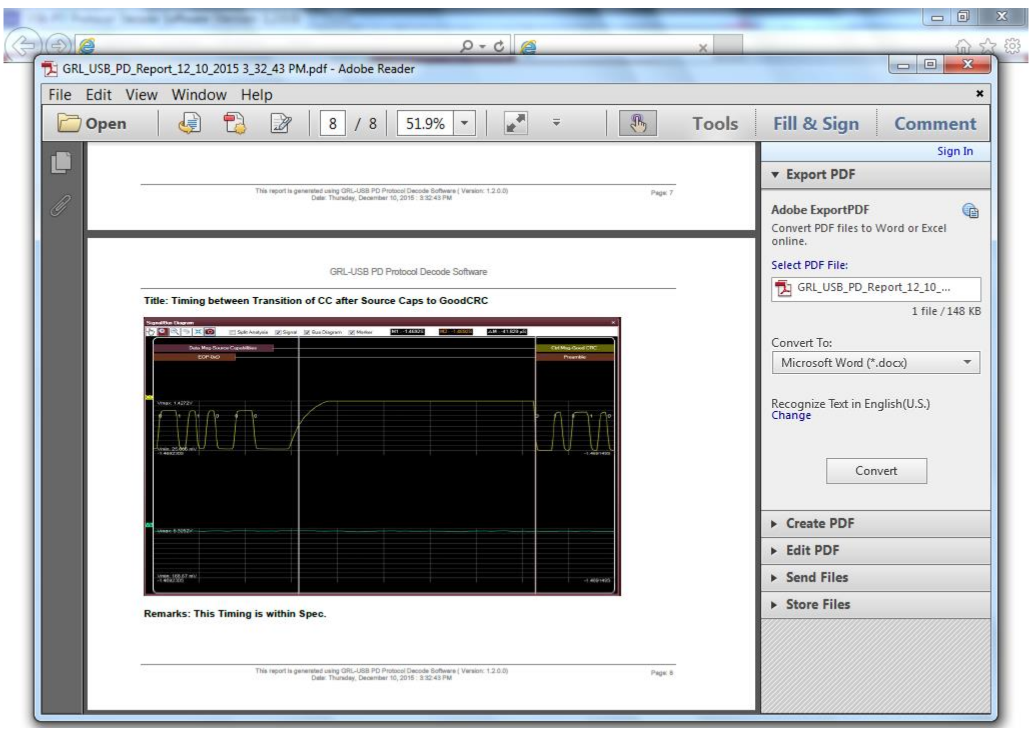
12) Double Click on the Window's title bar to reduce the window back to its original size docked into in the application.



13) In the report generator window, you can Select the Images you want to have added to the report.



14) When the report is created, the saved screenshots with Title and Remarks are added to the end of the report.



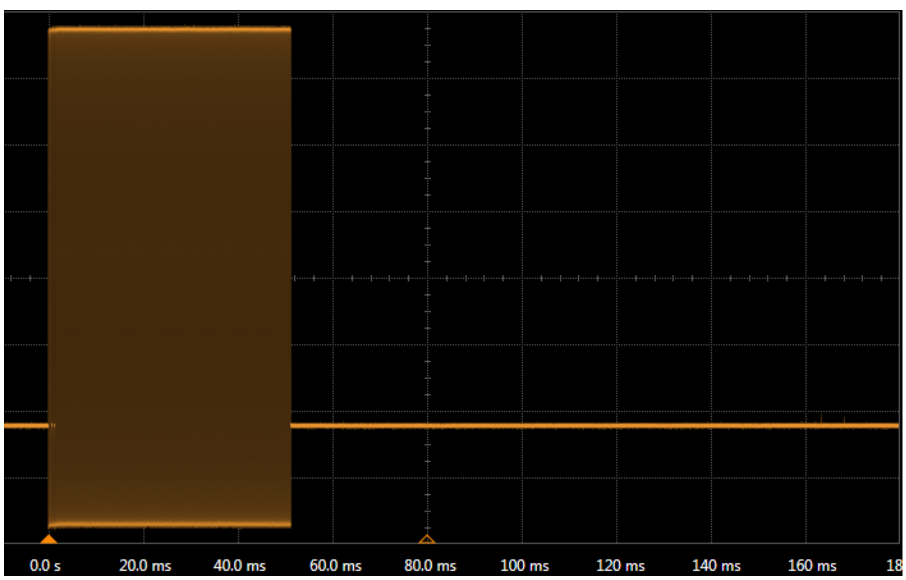
11.2 BMC-PHY Test Method using GRL-USB-PD Software

This section shows how to use GRL-USB-PD Software is used to perform Eye Diagram and BMC-PHY measurement testing on a BIST pattern. This test is done as part of Compliance testing, but the software can also be used to analyze the Eye Diagram and measurements in more detail.

1) Capture a USB-PD BIST Packet using the oscilloscope. Settings of the oscilloscope are as follows:

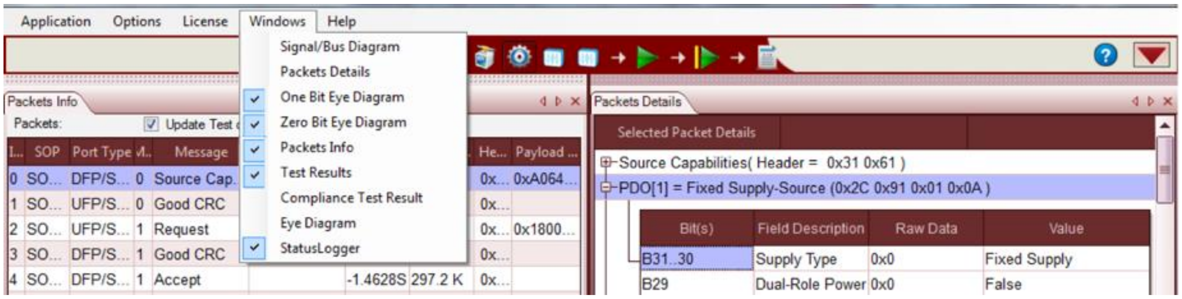
1. Scope BW limited as follows:
    i) > 100 MHz so not to introduce measurement errors in the Rise/Fall Measurements.
    ii) < 500 MHz as passive probes are limited to 500MHz BW and additional BW with introduce unwanted noise.
2. Scope Sample Rate sufficient to capture >5 sample points on 300nS rise time signal (50MS/sec recommended).
3. Scope Record Length to capture > 100mS of BIST data. The specification limit for BIST pattern length is 60mS.
4. Oscilloscope Acquisition Mode set to High Res Mode to minimize noise.
5. CC Signal captured using as much of the oscilloscope's A/D range between V_{HIGH} and V_{LOW} (>7 Divisions) to minimize quantization errors on the scope.
6. Scope set to trigger to capture the full BIST Signal including header and BIST Carrier 2 content.

The captured waveform below shows typical waveform with BIST initiation packet from the link partner (GRL-USB-PD-C1 test controller for example) and the BIST response packet from the DUT.

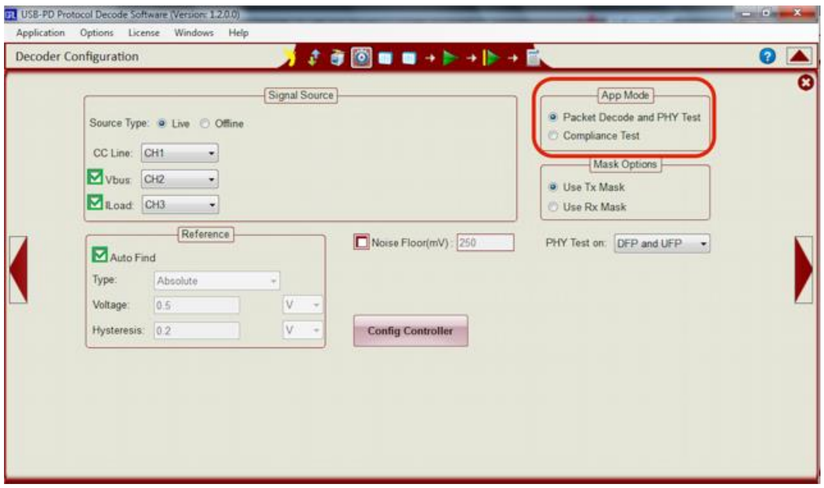


2) Run GRL-USB-PD software on the oscilloscope.

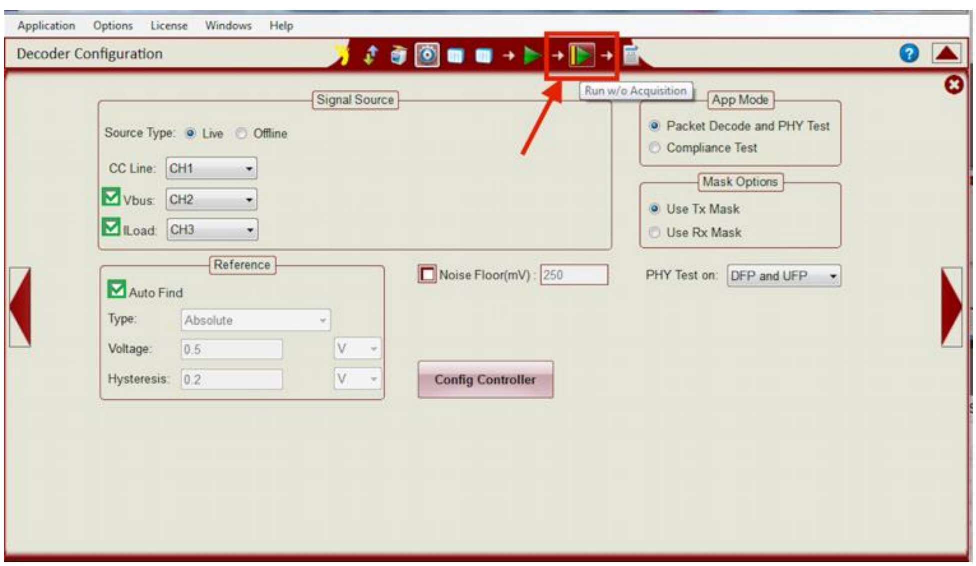
1. The following shows the **View** selections optimized for PHY-BMC signal analysis.



2. Select Packet Decode and PHY Test selection under App Mode.



3. Press the Run w/o Acquisition button.



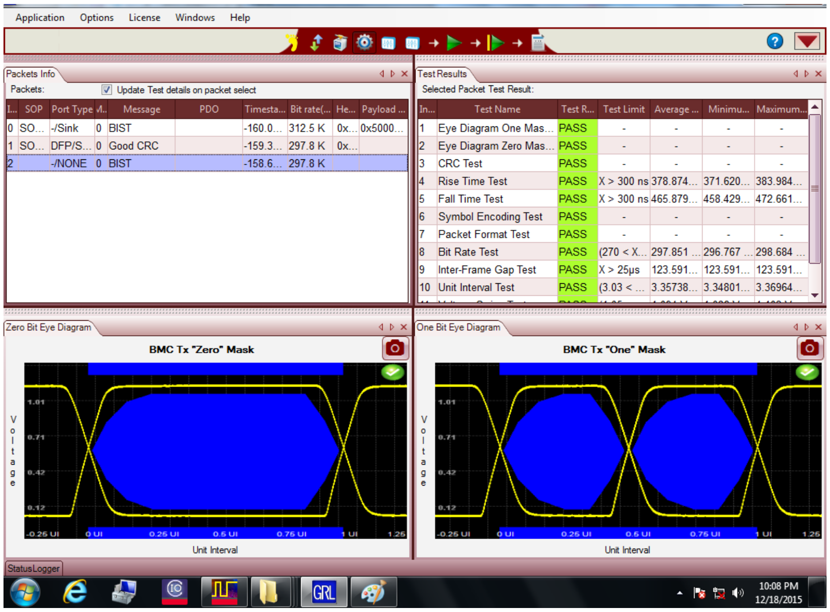
4. The GRL-USB-PD software post processes the waveform.

   i) The timing reference (clock recovery) of the BMC Signal is performed per Section 5.4 of the USB Power Delivery Test Plan.

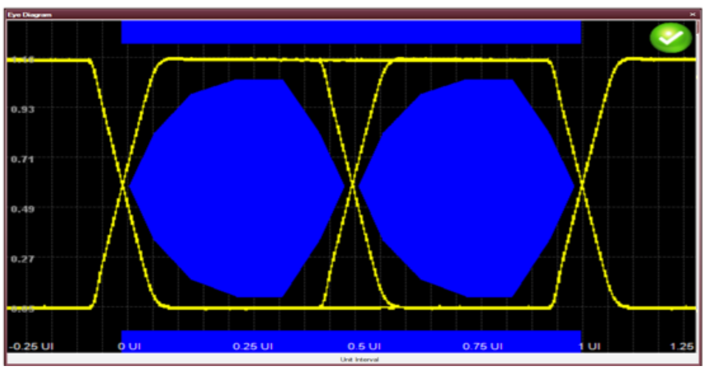
5. Select the BIST Response Packet, which is Packet 3 in the Packet Info list.

i) Packet 1 – BIST Request Packet from tester.
ii) Packet 2 – Good CRC from DUT
iii) Packet 3 – Header + BIST Carrier 2 Packet from DUT.

6. Refer to Section 5.9 of the USB-PD Specification for proper signal definition.
7. Make sure the **Update Test details on packet select** checkbox are selected.



In this screenshot, the 'One Eye' and 'Zero Eye' Windows are selected. In this case BMC logic '1s' are separated from BMC logic '0s', and plotted on the individual masks as defined in Section 5.8.3.2 of the USB Power Delivery Specification. If 'Tethered Device' is selected in the Device Type menu, which means that the DUT has an attached cable, then the Rx Masks are used. If not, then the TX Masks are used, and a USB Type-C Test Cable of short length is used for testing.



In this screenshot, the 'Eye Diagram' Window is selected. In this case the Eye diagrams for BMC logic '0' and BMC logic '1' are overlaid so all of the BIST Carrier2 signal is captured in a single picture. This is the Compliance requirement as described in Section 5.4 of the USB PD Test Plan.

3) The Test Results Window shows the PHY measurements made on the BIST Packet. PHY measurements in this section are defined in Chapter 5 of the USB-PD Specification.

11.3 RX Mask Test Method using GRL-USB PD Software

For Rx Mask testing in Packet Decode Mode following steps have to be followed.

1. Use Config Controller and configure the DUT to generate BIST Carrier Mode 2 command with load on Vbus.

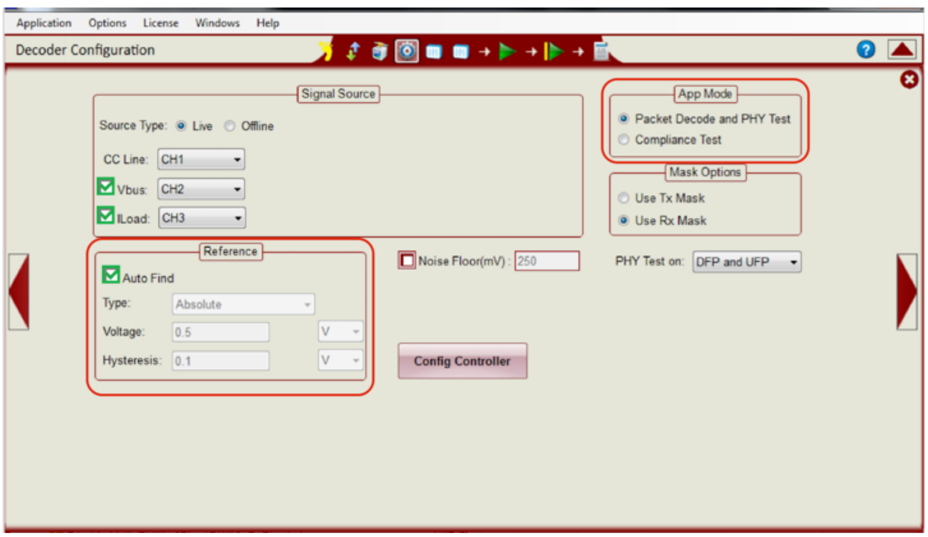
2. Capture the Signal in the Oscilloscope and save the waveform

3. Select Packet Decode Mode with RX testing Enabled and run the Mask test.

12 Appendix D: Reference Level Adjustment

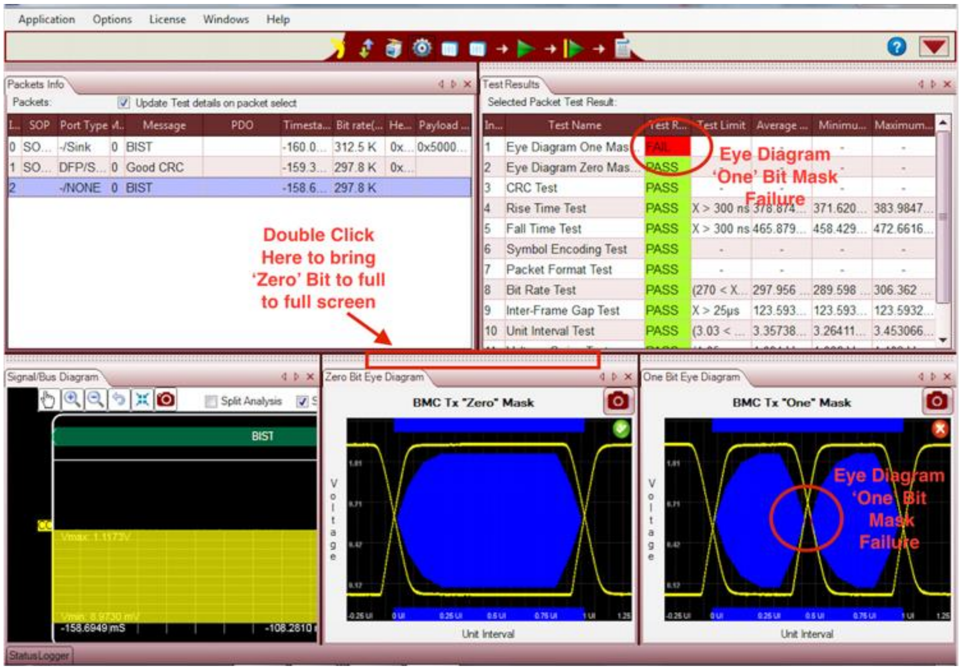
12.1 Using Ref Level Adjustment to Correct Clock Recovery Errors

This section shows how to use the **Reference** level feature in the decoder configuration menu to optimize the clock recovery for BMC-Eye Diagram testing.



The default mode is **Auto Find**. With Auto Find, the Vertical Reference level used for clock recovery on the eye diagram is [V_{HIGH} –V_{LOW}] /2. This works well for BMC Transmitters that have balanced Rise/Fall times and Crossing Voltage of the BMC Logic 0 is at the midpoint of the signal swing. In some cases, however, imbalance in Rise/Fall time can cause the crossing voltage to be above or below the mid level. In this case, the Eye diagram will exhibit crossing voltages well above the masks mid-level, and the eye diagram may look to not be properly time aligned (resembling 'jitter' on the edges of the BMC Logic0 signal). In this case, the reference level can sometimes be adjusted to correct this clock recovery error and make an otherwise Failing eye to instead Pass the Eye Mask test. The following shows an example of how to use this adjustment.

In this example we start with a BIST Compliance result that Fails the Mask just slightly during the BMC ‘1’ transition in the middle of the mask.



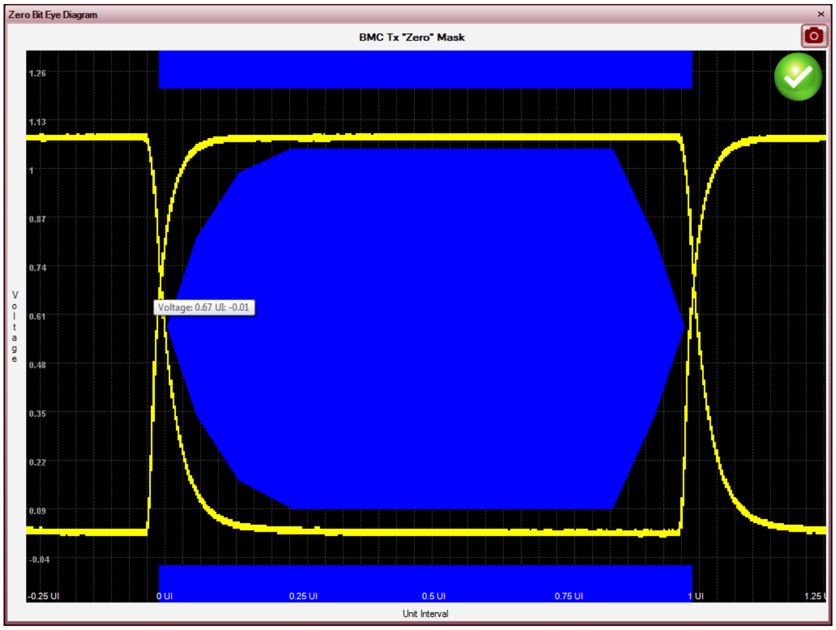
To correct this clock recovery error, do the following:

1) To perform this adjustment, make sure you are in the **Compliance Test to Packet Decode and PHY Test** in the **Decode Configuration** Menu.

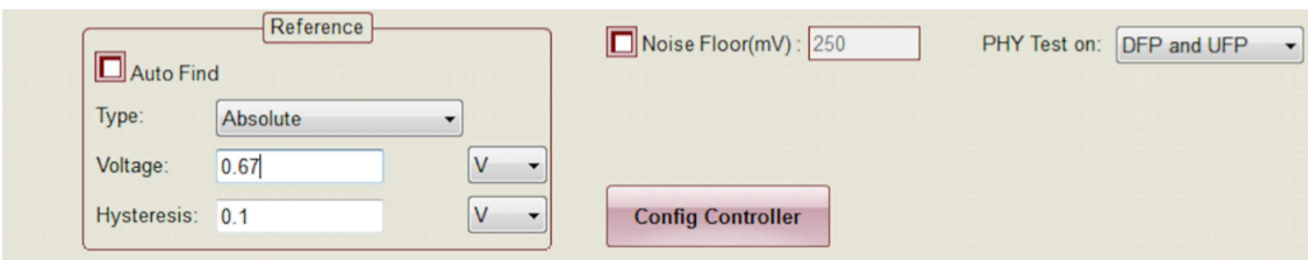
2) Double Click on the Double Dotted line on the **BMC TX ‘Zero’ Mask Plot** to expand it to full screen.

1. Note that while the failure occurred on the ‘One’ Bit Mask, the Clock Recovery is done on the ‘Zero’ bit mask, so the reference level adjustment will be determined on the ‘Zero’ Mask Plot.

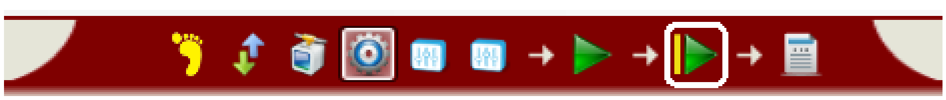
3) Use the mouse over feature in the Plot Window to determine the Voltage level where the ‘Zero’ Bit Rise/Fall transitions cross. In this case the voltage is **0.67V**.



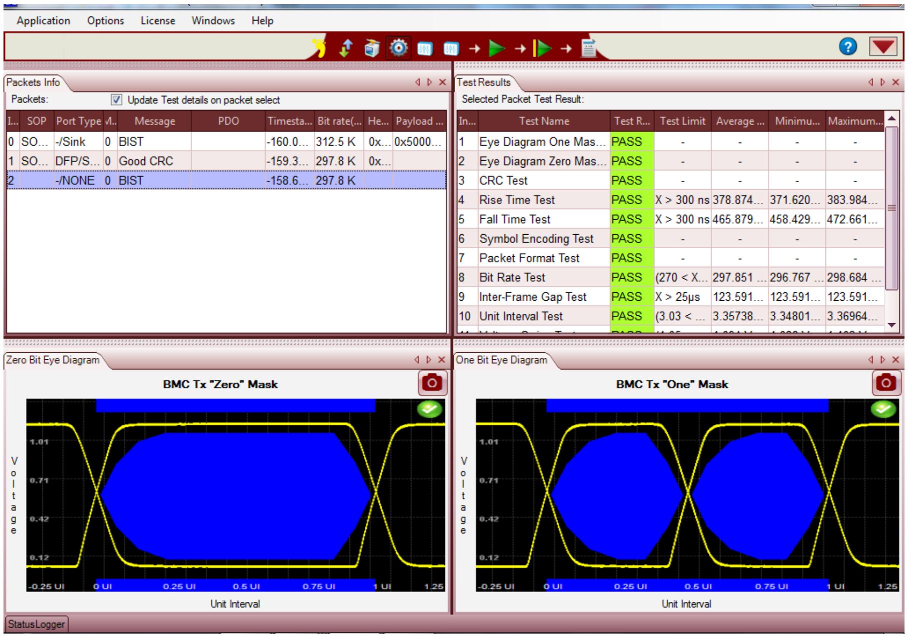
4) Return to the Decoder Configuration menu.
5) Uncheck the Auto Find Box.
6) Enter the measured crossing voltage above from Step 3 into the Voltage box.



7) Press the Run without Acquisition button on the top of the software GUI to re-run the same waveform with the new reference level setting.



8) The result of the new test is a Passing Eye result with the Clock recovery corrected.

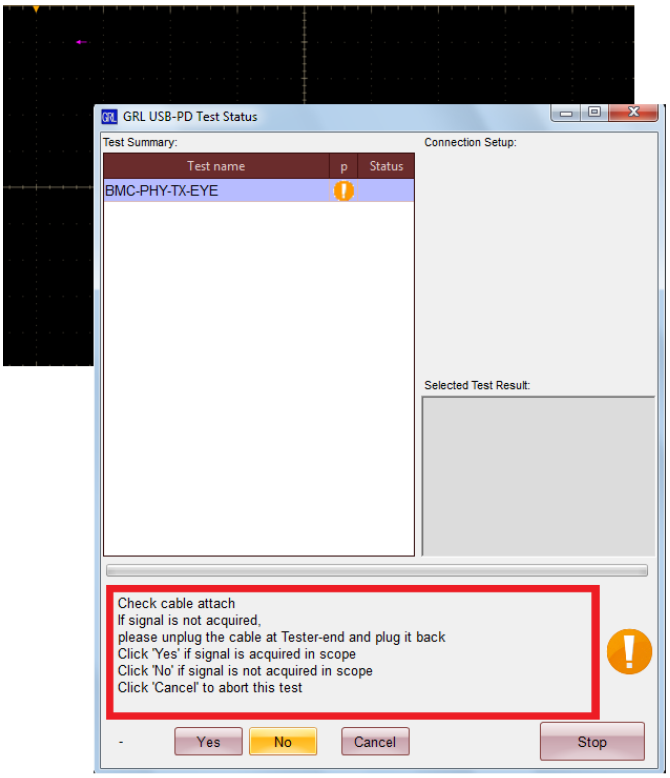


13 Appendix E: Troubleshooting Techniques

This section describes some known techniques for troubleshooting.

13.1 Recovering from Scope Not Triggering on Expected Signal

While testing, sequencing between the UUT and the controller can in some cases get out of sync. This can result in the scope not triggering on the proper signal. The following screenshot shows what might happen if this occur. The scope trigger is armed, but no signal is present on the line to trigger on.



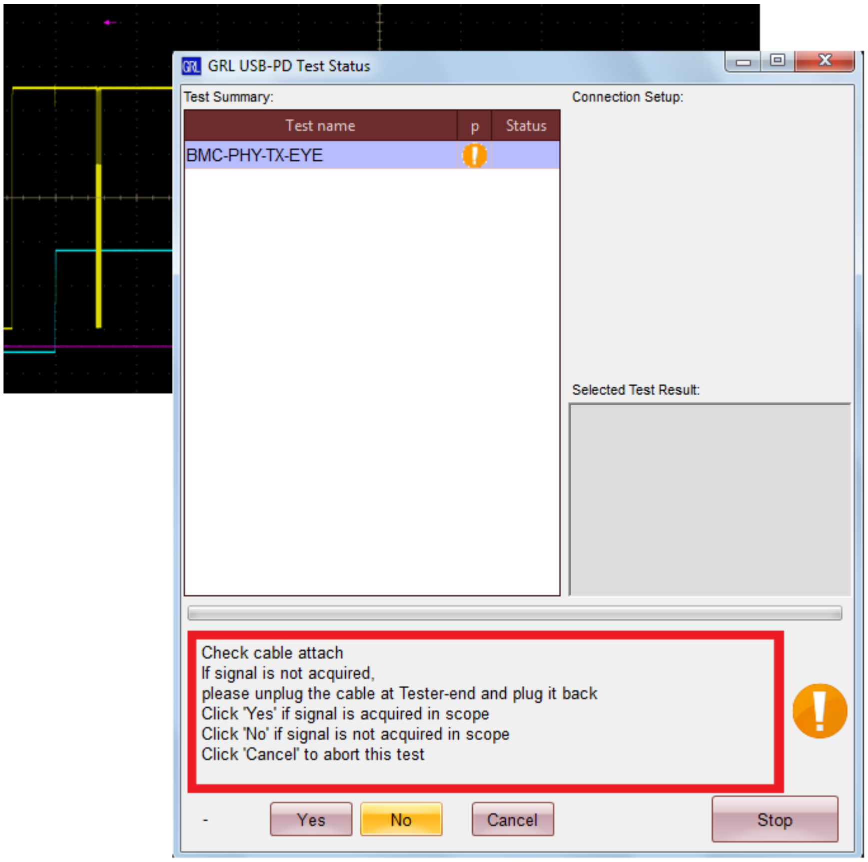
When this occurs, do the following:

1. Disconnect the DUT from the Controller.
2. Power cycle the Controller by switching the controller ‘Off’ and then ‘On’ again.
3. Reset the DUT by cycling its power.
4. Connect the DUT to the Controller.
5. Press OK

This should recover and result in getting the proper signal for Cable Detach<>Attach as described in Section 5.

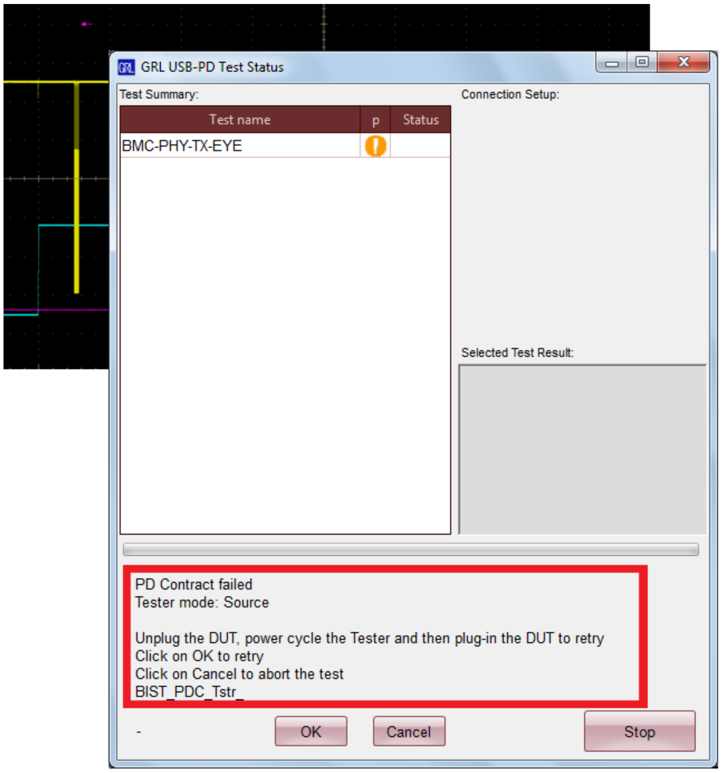
13.2 Wrong Signal Captured Automatically Recovered in Software

Another possible issue that can occur during testing is that an unexpected signal is captured for the test being performed. In this case the software automatically recovers. When this happens, the following signal is displayed and a message to check cable attach is presented. However, the repeating signal does not represent a valid PD contract.

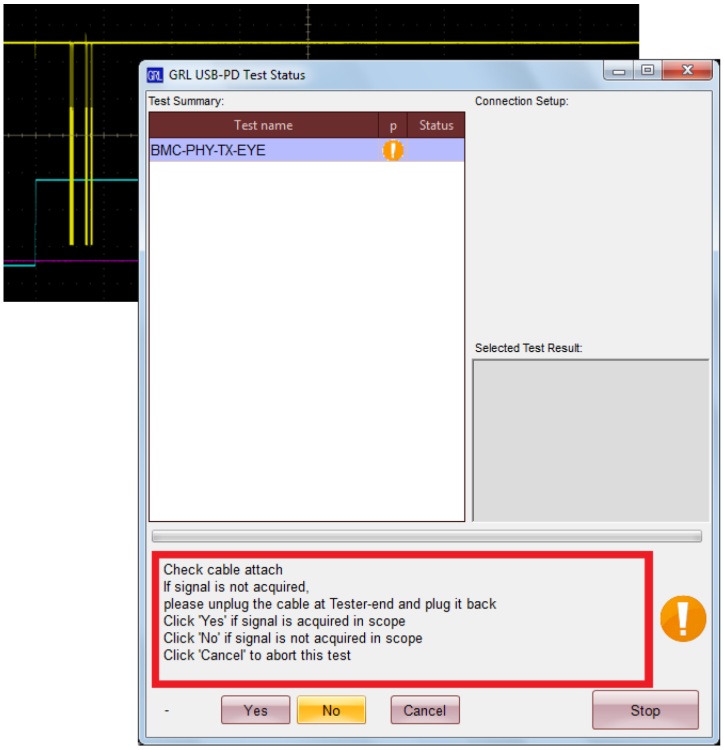


When this occurs, do the following:

1. Press Yes.
2. The software will automatically retry, however, on the retry it determines that the controller is not getting the proper response, so it provides the following message.



3. Follow the onscreen instructions:
    a. Unplug the DUT.
    b. Power cycle the Controller by switching the controller 'Off' and then 'On' again.
    c. Power cycle the DUT
    d. Plug Cable between DUT and Controller.
    e. Press OK.
4. When recovered the proper PD Contract is captured by the Scope trigger.



5. Press Yes to proceed with testing.

14 Appendix F: Test Descriptions

The following sections describe in detail each of the tests from Section 12 of the USBPD Compliance Specification.

For each category of UUT, there is a primary list of tests which shall be performed.

It is a requirement that the names of the tests, and the corresponding failure names be included in any test reports. Test Reference Numbers may also be included in reports. The report generated by GRL-USB-PD software includes all tests run on the UUT and the Pass/Fail disposition of each test. Optionally, waveforms may also be saved with the test report for future analysis and debug.

14.1 Power Rules Tests

The Power Rules Test verifies that the DUT meets its advertised Power Rating. When performing Get Capabilities on the DUT, the DUT advertises to the tester its maximum Power Rating through a combination of PDOs (Voltage and current combinations).

The Power Rules tests check compliance to Sections 10.2 and 10.3 of the Power Delivery Specification.

For Providers, the following rules must be followed for the 'declared' power rating from the vendor.

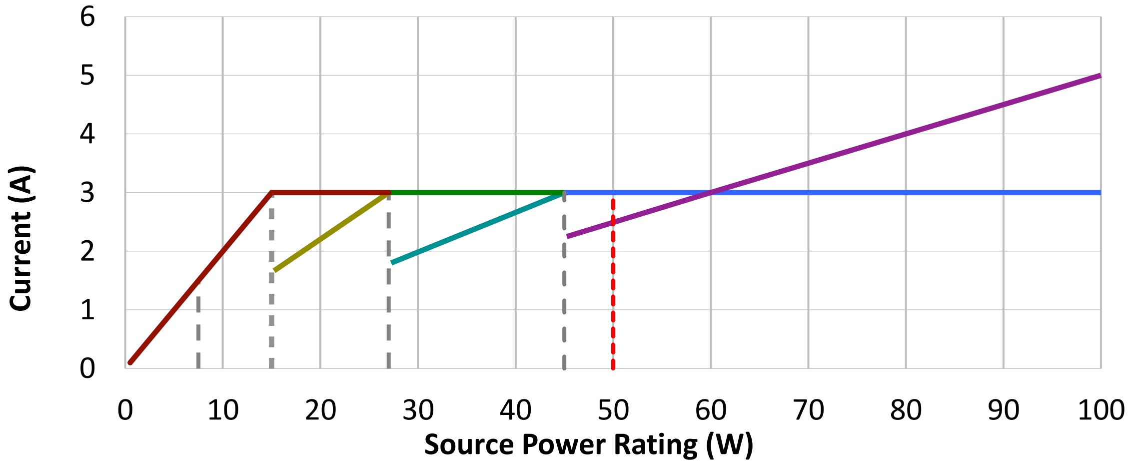


FIGURE 71: POWER SOURCE RATING GRAPH

For example, if an adapter with a rating at 50W. The adapter is required to support 20V at 2.5A, 15V at 3A, 9V at 3A and 5V at 3A.

12.1.1 PDSPEC 10.10.2 SRC-POW-RULE Source Power Rules

Status	Primary Test
Purpose	To ensure the Source PD Power (PDP) of UUT specified in watts explicitly defines the voltages and currents at each voltage the UUT supports. Also, to ensure that UUT with a large PDP are always capable of providing the power to devices designed with a smaller PDP
Critical for Safety	
Applies to	DRP, Provider, Provider/Consumer or Consumer/Provider
Description	The Tester verifies the voltage and current values in source capability message sent from UUT with normative voltages and currents in table 10-2 in PD specification for the PD Power specified by vendor.
Test setup	Protocol Tester.
Ping Policy	n/a
Preconditions	The UUT vendor is assumed to have provided Source PD Power (PDP).
Test Condition	For a Provider, the PDO defines how much current can be sourced to a sink at each advertised voltage. The DUT can support more voltages than the spec requires, but the minimum voltages supported must include the standard voltages defined in the spec.
Assertions Tested	n/a
Parameters Tested	Advertised voltage and current
Pass /Fail Criteria	For a Provider: If the DUTs advertised PDOs do not match the required voltage levels for its max advertised power rating, the DUT will Fail. If the DUTs advertised PDOs do not match it's Vendor Information File (VIF), the DUT will Fail. If the DUTs fails to provide 100% of the current advertised in the PDO while performing Provider Power Tests, the DUT will Fail
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.

2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. During the following, if Ping messages are received from the UUT, check that Ping messages timing meets requirements in PROT-PROC-PING.
4. The Tester gets the UUT into PD Mode (PROC-PD-MODE), initially requesting PDO#1 at 100mA.
5. Verify that the voltage and current values advertised by UUT (through Source Capabilities message) are meeting the normative voltage and current values given in table 10-2 of USB PD Specification for the PD Power specified by the vendor.
6. Emulate a Tester end detach.

12.1.2 PDSPEC 10.10.2 SNK-POW-RULE Sink Power Rules

Status	Primary Test
Purpose	To ensure that the UUT with Sink PD Power (PDP) operate or charge from source that have a PD Power greater than its own PD Power. To ensure that the UUT with Sink PD Power (PDP) either operate, charge or indicate a capability mismatch from Sources that have a PDP lesser than UUT’s PD Power and greater than equal to 0.5W
Critical for Safety	
Applies to	DRP, Consumer, Provider/Consumer or Consumer/Provider
Description	The Tester verifies the UUT operation with the source which has PD Power anything greater than 0.5W.
Test setup	Protocol Tester.
Ping Policy	n/a

Preconditions	The UUT vendor is assumed to have provided Sink PD Power (PDP).
Test Condition	For a Consumer, the PDO defines how much current will be sinked for a source at each voltage. The DUT can operate at other voltages, but the DUT shall not sink more than its max current at each standard voltage.
Assertions Tested	n/a
Parameters Tested	n/a
Pass/Fail Criteria	For a Consumer: If the DUTs advertised PDOs do not match the required current levels for its max advertised power rating, the DUT will Fail. If the DUTs advertised PDOs do not match its Vendor Information File (VIF), the DUT will Fail. If the DUTs fail to consume more than 100% of its advertised current draw at any supported voltage, the DUT will Fail.
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. During the following, if Ping messages are received from the UUT, check that Ping messages timing meets requirements in PROT-PROC-PING.
4. The Tester gets the UUT into PD Mode (PROC-PD-MODE), initially advertising source power greater than the UUT's Sink PD Power.
5. Verify that the UUT sends Request message with voltage and current values assigned within in the limit specified by vendor (Sink PD Power).
6. Emulate a Tester end detach.
7. The Tester gets the UUT into PD Mode (PROC-PD-MODE), initially advertising source power lesser than the UUT's Sink PD Power and greater than 0.5W.
8. Verify that the UUT sends Request message with voltage and current values assigned within in the limit specified by vendor (Sink PD Power) and capability mismatch flag set to 1 in Request message.
9. Emulate a Tester end detach.

14.2 Cable Markers - Primary Tests

14.2.1 Physical Layer – Transmit

It is normally not required to repeat these tests for SOP". The results from SOP' will suffice.

14.2.1.1 TDA.1.1.1.1.1: CAB-PHY-TX-EYE

TDA.1.1.1.1.2: CAB-DP-PHY-TX-EYE Cable Transmitter Eye Diagram Test (SOP Prime or Double Prime)

Status	CAB-PHY-TX-EYE
Test Title	Transmitter Eye Diagram Test (SOP Prime or Double Prime)
Status	Primary Test
Purpose	To confirm that the transmitted data fulfills the eye diagram mask requirements in Figures 5-23 and 5-24 of the specification. Also checks that Cable UUT correctly implements BIST Carrier Mode 2. It is normally not required to repeat this test for SOP". The results from SOP' will suffice.
Critical for Safety	
Applies to	Electronically Marked C-Cable
Description	The Protocol Tester sends a BIST request to a Cable UUT specifying 'BIST Carrier Mode 2'. The Cable UUT will then transmit a continuous string of BMC encoded alternating "1"s and “0”s in accordance with Section 5.9.4. The eye pattern is measured using the method specified below.
Test setup	Protocol Tester, plus oscilloscope function.
Preconditions	
Assertions Tested	5.8.3.2.1#1, 5.8.3.5#1, 5.9.4#1, 6.4.3#7, 6.4.3.6#1, 6.4.3.6#2, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

This test must be performed twice. Once with VCONN at 5V, and once with VCONN at 3V.

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections

of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The Tester applies VBUS, VCONN, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) to one cable end. The capacitive load of the tester is as close to 400pF as practical.
3. The Tester sends a BIST request to the Cable UUT, specifying 'BIST Carrier Mode 2', and checks for a valid and correctly timed protocol response [CAB_PHY_TX_EYE_1].
4. Check that the UUT is transmitting a continuous string of alternating '0' and '1' bits. This functional check shall be sufficiently accurate to ensure that the desired BIST continuous test pattern is present, and not one of the other four, nor a non-continuous transmission mode [CAB_PHY_TX_EYE_2]. The method used for this is left to the discretion of the test equipment vendor. The detailed parameters of the mode will be measured below.
5. Feed the output of the UUT into an oscilloscope type function.
6. Produce an Eye Diagram, using the method specified in section BMC-ALG-CLK-RECOV, and check that the parameters meet the requirements of Figures 5-23 and 5-24 of the Specification [CAB_PHY_TX_EYE_3].
7. Check that the continuous test pattern stops within tBISTContMode max (60ms) of starting [CAB_PHY_TX_ EYE _4].
8. Check that the rise/fall times meet the specification in Table 5-25 [CAB_PHY_TX_ EYE _5].
9. Reset Cable UUT by simulating a tester end cable detaches, in order to guarantee exiting the BIST Mode.
10. Repeat test using the other end of the cable.

14.2.1.2 TDA.1.1.1.2.1 CAB-PHY-TX-BIT

14.2.1.3 TDA.1.1.1.2.2: CAB-DP-PHY-TX-BIT

Cable Transmit Bit Rate and Bit Rate Drift (SOP Prime or Double Prime)

Test Name	CAB-PHY-TX-BIT
Test Title	Cable Transmit Bit Rate and Bit Rate Drift (SOP Prime or Double Prime)
Status	Primary Test
Purpose	The Protocol Tester sends a BIST request to a Cable UUT specifying 'BIST Carrier Mode 2'. The Cable UUT will then transmit a continuous string of alternating "1"s and “0”s. The data being transmitted are fed into a clock/data recovery function, and the output of this into a frequency counter function. During one or more period’s equivalent to the longest possible packet length, the bit rate is measured according to section??? And Table? This is validated against pBitRate and fBitRate
Critical for Safety	
Applies to	Electronically Marked C-Cable

Description	The Protocol Tester sends a BIST request to a Cable UUT specifying 'BIST Carrier Mode 2'. The Cable UUT will then transmit a continuous string of alternating "1"s and "0"s. The data being transmitted are fed into a clock/data recovery function, and the output of this into a frequency counter function. During one or more period's equivalent to the longest possible packet length, the bit rate is measured according to section??? And Table? This is validated against pBitRate and fBitRate.
Test setup	Protocol Tester, plus clock/data recovery function, plus counter/timer function. The Cable UUT is connected by one chosen end to the tester, the other end is left unconnected. The test is repeated using the other cable end.
Preconditions	
Assertions Tested	5.8.1.2.1#1, 5.8.1.2.1#2, 5.9.4#1, 6.4.3#7, 6.4.3.6#2 Plus assertions in any appropriate secondary checks. Parameters
Parameters Tested	pBitRate, fBitRate.
Checklist References	

This test must be performed twice. Once with VCONN at 5V, and once with VCONN at 3V

Note: The sample data collected for this test is likely to be the same data collected during the Tx Eye Diagram test CAB-PHY-TX-EYE. Combining these tests is valid if the Tester Vendor considers this appropriate.

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The Tester applies VBUS, VCONN, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) to one cable end.
3. The Tester sends a BIST request to the Cable UUT, specifying 'BIST Carrier Mode 2', and checks for a valid and correctly timed protocol response [CAB_PHY_TX_BIT_1].
4. Check that the UUT is transmitting a continuous string of alternating '0' and '1' bits. This functional check shall be sufficiently accurate to ensure that the desired BIST continuous test pattern is present, and not one of the other four, nor a non-continuous transmission mode

[CAB_PHY_TX_BIT_2]. The method used for this is left to the discretion of the test equipment vendor. The detailed parameters of the mode will be measured below.

5. Use a clock/data recovery function to monitor the signal during the next step. The measurement shall be made using the positive bit edge at the start of a group of four modulated "0101" bits as the significant reference points. (The first zero is therefore a high level.) This reduces the effect of:
   a) Different rise and fall wave forms
   b) Different rise times dependent on value of previous bit.
6. Ensure that at least 32 bits have been detected before starting measurement. The first bit to be included starts at a reference point as defined above, and is referred to below as data bit 0.
7. Measure the bit rate during a 32 bit period. Calculate this as 32, divided by the total period between 9 reference points.
8. Do this from data bit 0 to data bit 31, and then from data bit 4 to data bit 35, and repeat until there are 256 bit rate measurements.
9. The bit rate measured from data bit 0 to data bit 31 is taken as the measured fBitRate.
10. Calculate pBitRate as the largest deviation from fBitRate divided by fBitRate, expressed as a percentage.
11. Check that the lowest and highest bit rate values measured fall within fBitRate (270-330 kbps) [CAB_PHY_TX_BIT_3], and that pBitRate (less than 0.25%) is within permitted range [CAB_PHY_TX_BIT_4].
12. Check that the continuous test pattern stops within tBISTContMode max (60ms) of starting [CAB_PHY_TX_BIT_5].
13. Reset Cable UUT by simulating a tester end cable detaches, in order to guarantee exiting the BIST Mode.
14. Repeat test using the other end of the cable.

14.2.2 Physical Layer – Receive

It is normally not required to repeat this test for SOP". The results from SOP' will suffice.

14.2.2.1 TDA.1.1.2.1.1: CAB-PHY-RX-BUSIDL

TDA.1.1.2.1.2: CAB-DP-PHY-RX-BUSIDL Cable Bus Idle Detection Test (SOP Prime or Double Prime)

Test Name	CAB-PHY-RX-BUSIDL
Test Title	Cable Bus Idle Detection (SOP Prime or Double Prime)
Status	Primary Test
Purpose	Confirm that the UUT accurately recognizes the Bus Idle Condition, and does not interpret valid noise interference as a false Bus Idle Condition.
Critical for Safety	No

Applies to	Electronically Marked C-Cable
Description	Messages are sent to the Cable UUT under conditions which check the receiver's ability to detect Bus Idle. In steps 1-5, the tester verifies that if the bus is not idle, the UUT does not send a GoodCRC. It achieves this by sending valid transitions during the time window during which the GoodCRC is allowed to be sent. In steps 6-8, the tester verifies that expected levels of noise on the CC line do not prevent the UUT from detecting Bus Idle. It achieves this by sending noise during a time window, and ensuring that the last part of a GoodCRC is sent, but not a complete GoodCRC.
Test setup	Protocol Tester with programmable transmit signal waveform.
Preconditions	
Assertions Tested	5.8.1.4#4, 6.4.3#7, 6.4.3#10, 6.4.3.9#1, 5.7#1, 5.7#2, 5.8.3.2.2#7, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

This test must be performed twice. Once with VCONN at 5V, and once with VCONN at 3V.

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The Tester applies VBUS, VCONN, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) to one cable end.
3. The Protocol Tester sends a BIST request to the Cable UUT, specifying 'BIST Test Data', and checks for a valid and correctly timed protocol response [CAB_PHY_RX_BUSIDL_1]. This shows that the basic test mechanism is working and prevents the UUT from sending any other messages during the following steps.

4 Send BIST Test Data message, disable Tester receiver and then immediately continue sending data zeros for 195us, then open receiver. (This step prevents the UUT from sending a GoodCRC, because the CC line will not be idle during the time in which it is valid to start sending one.)

5 Listen for data from UUT. There must be nothing for 10 ms [CAB_PHY_RX_BUSIDL_2]. If we see a GoodCRC message ending, or a complete GoodCRC, the UUT is deemed to have failed the test. *See Figure below for explanation.*

6 Send BIST Test Data message, disable tester receiver then continue sending noise (see definition below) for 195+237+6.6us=438.6us, then open receiver. We are expecting the UUT to ignore the noise, and respond with a GoodCRC, so we should detect the end of an already started GoodCRC. The time chosen to re-enable the receiver is a point in time during which a legally timed GoodCRC will be encountered at a point after the start of its SOP and before the end of the CRC, regardless of whether this message is sent at the earliest possible opportunity at the fastest rate allowed, or at the latest opportunity at the slowest rate possible.

7 Listen for data from other end - check that we see data present, but do not receive a valid GoodCRC [CAB_PHY_RX_BUSIDL_3]. If we see a GoodCRC it means that it was started later than permitted, for whatever reason. If we see no data then it means that the UUT incorrectly saw the noise as an interfering signal and did not transmit the GoodCRC.

8 Reset Cable UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.

9 Repeat test using the other end of the cable.

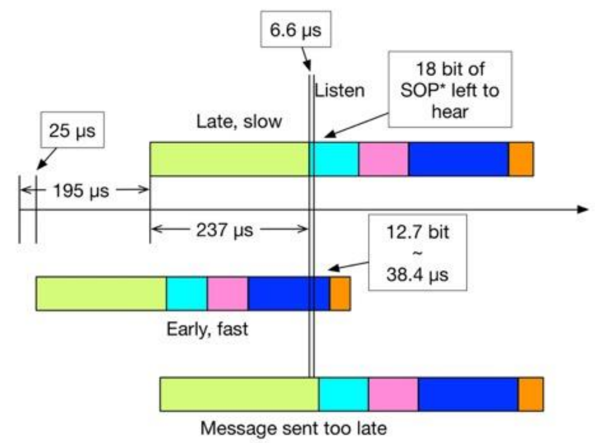


FIGURE 72: BUS IDLE DETECTION TIMINGS

14.2.2.1.1 Timing details

- 237us is the longest time required to send a preamble.
- 6.6us is a margin to ensure not seeing SOP.
- Message could be over in 25us + 149 bits at fastest speed = 472us (leaves minimum 38.4us or 12.7 bits)

14.2.2.1.2 Definition of Noise

- The noise signal shall be transmitted by the same transmit amplifier as the preceding signal, remaining at the same output impedance, to ensure the correct level.
- It shall be a square wave at a frequency of 600 kHz.

- It shall have an amplitude of 250mV p/p, biased around 0.55V.

14.2.2.2 TDA 1.1.2.1.2 CAB-DP-PHY-RX-BUSIDL

TDA.1.1.2.2.2: CAB-DP-PHY-RX-INT-REJ

Cable Receive Interference Rejection Test (SOP Prime or Double Prime)

Test Name	CAB-DP-PHY-RX-BUSIDL
Test Title	Cable Bus Idle Detection (SOP Prime or Double Prime)
Status	Primary Test
Purpose	Checks the ability of the receiver to correctly receive signals which are degraded by the worst case aggressor signal, and both the zero offset and worst case offset in the appropriate direction, whilst the bitrate is also set to both minimum and maximum extremes. The test applies equally to SOP' and, for cables with an SOP" controller present, to SOP".
Critical for Safety	No
Applies to	Electronically Marked C-Cable
Description	Messages are sent to the Cable UUT under conditions which check the receiver's ability to detect Bus Idle. See additional details in Section 14.2.2.1.
Test setup	Protocol Tester with programmable transmit signal waveform.
Preconditions	
Assertions Tested	6.4.3#10, 5.8.1.1#1, 5.8.3.4.1#1, 5.8.3.6#1, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

14.2.2.3 TDA 1.1.2.2.1

14.2.2.4 CAB-PHY-RX-INT-REJ Cable Receiver Interference Rejection Test

TDA 1.1.2.2.2 CAB-DP-PHY-RX-INT-REJ Cable Receiver Interference Rejection Test

Test Name	CAB-PHY-RX-INT_REJ
Test Title	Cable Receiver Interference Rejection (SOP Prime or Double Prime)
Status	Primary Test
Purpose	Checks the ability of the receiver to correctly receive signals which are degraded by the worst case aggressor signal, and both the zero offset and worst case offset in the appropriate direction, whilst the bitrate is also set to both minimum and maximum extremes.

	The test applies equally to SOP' and, for cables with an SOP" controller present, to SOP".
Critical for Safety	No
Applies to	Electronically Marked C-Cable
Description	The Protocol Tester uses BIST Test Data messages, in the presence of injected interference. The UUT is required to respond with GoodCRC messages, without missing any.
Test setup	USB PD Tester (with ability to add an aggressor signal and an offset to the data signal, while sending minimum and maximum permitted bitrates).
Preconditions	
Assertions Tested	6.4.3#10, 5.8.1.1#1, 5.8.3.4.1#1, 5.8.3.6#1, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

This test must be performed twice. Once with VCONN at 5V, and once with VCONN at 3V.

This is achieved by using a short cable, and artificially adding an aggressor signal to the transmitted signal. The tester will add voltage offset, corresponding to ground differential, artificially to the signal.

The basic signal transmitted will represent the minimum swing likely to reach the receiver.

The aggressor signal will be a non-synchronized square wave at maximum defined noise level (see table below for parameters)..

Test Procedure

1. Test Procedure During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.

2. The Tester applies VBUS, VCONN, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) to one cable end.
3. The Protocol Tester sends a BIST request to the Cable UUT (with incremented MessageID as normal*), specifying 'BIST Test Data', and checks for a valid and correctly timed protocol response [CAB_PHY_RX_INT_REJ_1]. This shows that the basic test mechanism is working and prevents the UUT from sending any other messages during the following steps.
4. Wait 15ms to ensure that the UUT understands it is in a BIST test mode, and should not initiate any message sequences*.

5. In the following step, send BIST Test Data message using the signal and the distortions defined in Tx Group 1 below.
6. Send the 'BIST Test Data' message (without incrementing MessageID*) 13362 times to validate BER, and check that the UUT fails to respond with GoodCRC no more 0 times [CAB_PHY_RX_INT_REJ_2]. n=4502*(1024/345).
7. In the following step, send BIST Test Data message using the signal and the distortions defined in Tx Group 2 below.
8. Send the 'BIST Test Data' message (without incrementing MessageID) 13362 times to validate BER, and check that the UUT fails to respond with GoodCRC no more 0 times [CAB_PHY_RX_INT_REJ_3]. n=4502*(1024/345).
9. In the following step, send BIST Test Data message using the signal and the distortions defined in Tx Group 3 below.
10. Send the 'BIST Test Data' message (without incrementing MessageID) 13362 times to validate BER, and check that the UUT fails to respond with GoodCRC no more 0 times [CAB_PHY_RX_INT_REJ_3]. n=4502*(1024/345).
11. Reset Cable UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.
12. Repeat test using the other end of the cable.

Note: The Signaling Groups shown in Table 2 are from Revision 0.908 of the USB Power Delivery Compliance Test Specification. These represent testing at the most recent USB Workshops. The Receiver Interference definition in Revision 1.0 of the CTS is under development.

TABLE 2: GROUP 1/2/3 SIGNAL SPECIFICATIONS

	Nominal Signal	Group 1 Signal	Group 2 Signal	Group 3 Signal
High Level (nom)	1100 mV	1200 mV	790 mV	1290 mV
Low Level (nom)	25 mV	0 mV	-250 mV	250 mV
Bit Rate	300 kb/s	270 kb/s	330 kb/s	330 kb/s
Noise Period **	N/A	608 ns	608 ns	608 ns
Noise Amplitude **	0 mV p/p	100 mV p/p	100 mV p/p	100 mV p/p
Rise/Fall Time	735 ns	735 ns	735 ns	735 ns

Notes on Table 2:

1) The signal rise and fall time shall be increased till the eye of Nominal Signal well touches the Tx Eye Mask. The same rise and fall time shall be used for Group 1, 2, and 3 Signal.
2) The nature of this test is to send a BIST Test Data message repeatedly, with minimum delay between the GoodCRC response from the UUT and the next BIST Test Data message from the tester. There would be a potential for a UUT not to be able to deal with messages of such frequency if the test were not implemented exactly as described above. The first BIST Test Data message must have an incremented MessageID so that the UUT recognizes it as a significant message, and stops originating its own traffic. The 15ms delay before further messages ensures that the UUT has had time to recognize the message. The fact that the MessageID is then not incremented is specified so that the UUT Protocol Engine will not pass the messages up to the Policy Engine, but **will** respond with GoodCRC. This behavior is specified in the PD Specification.

14.2.3 Physical Layer – Miscellaneous

It is normally not required to repeat this test for SOP". The results from SOP' will suffice.

14.2.3.1 TDA.1.1.3.1.1 CAB-PHY-TERM Cable Termination Impedance Test

Test Name	CAB-PHY-TERM
Test Title	Cable Termination Impedance (SOP Prime or Double Prime)
Status	Primary Test
Purpose	To confirm that a UUT has a valid impedance when not transmitting. The test applies equally to SOP' and, for cables with an SOP” controller present, to SOP".
Critical for Safety	
Applies to	Electronically Marked C-Cable

Description	The Protocol Tester chooses a time when the UUT is not transmitting, and measures the impedance of the receiver using a voltage source and resistor.
Test setup	Protocol Tester with voltage generator, resistor, and voltage measurement function.
Preconditions	
Assertions Tested	6.4.3#10, 6.4.3.9#1, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

This test must be performed twice. Once with VCONN at 5V, and once with VCONN at 3V.

Note: It is not practical to directly measure the input impedance of the receiver in the UUT (required to be >= 1 MΩ), as it is masked by the Rp / Rd resistors. Instead we will assume the presence of these resistors and measure that the resulting resistance falls within a valid range.

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The Tester applies VBUS, VCONN, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) to one cable end.
3. The Protocol Tester sends a BIST request to the Cable UUT, specifying 'BIST Test Data', and checks for a valid and correctly timed protocol response [CAB_PHY_TERM_1]. This shows that the basic test mechanism is working and prevents the UUT from sending any other messages during the following steps.
4. Check that the voltage on the CC line falls within the expected range, knowing the value of these resistors [CAB_PHY_TERM_2].
5. Reset Cable UUT by simulating a tester end cable detaches, in order to guarantee exiting the BIST Mode. Verify that UUT does not modify voltage levels in any received message waveform when VCONN is off
6. The Tester applies VBUS, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) [but not VCONN] to one cable end.
7. Check that signal voltages on the CC line of -300mV and 1500mV are not modified at the receiver input by more than the tester tolerances may produce. The actual test method is left to the discretion of the implementer.

8. Reset Cable UUT by simulating a tester end cable detaches, in order to guarantee exiting the BIST Mode. Verify that UUT does not modify voltage levels in any received message waveform when VCONN is on
9. Repeat the last 3 steps, but with VCONN applied.
10. Repeat test using the other end of the cable.

14.2.3.2 TDA 1.1.3.1.2 CAB-DP-PHY-TERM DP Cable Termination Impedance Test

Refer TDA 1.1.3.1.1

14.2.3.3 TDA.1.1.3.2.1 CAB-PHY-MSG Cable PHY Level Message Test

Test Name	CAB-PHY-MSG
Test Title	Cable PHY Level Message (SOP Prime or Double Prime)
Status	Primary Test
Purpose	To validate the PHY level behavior of message exchanges. To confirm the PHY level behavior of the UUT in relation to Cable Reset and Hard Reset. The test applies equally to SOP' and, for cables with an SOP” controller present, to SOP".
Critical for Safety	
Applies to	Electronically Marked C-Cable
Description	The Protocol Tester sends a sequence of messages both correct and with deliberate errors and validates the correct behavior in each case. Protocol Tester sends Hard Reset and Cable Reset messages to the Cable UUT, and confirms correct operation by the UUT. While running the test for SOP', SOP' is referred to as the Primary SOP type and SOP" as the alternative SOP type. While running the test for SOP", SOP" is referred to as the Primary SOP type and SOP' as the alternative SOP type.
Test setup	Protocol Tester with control over low level packet generation.

Preconditions	
Assertions Tested	5.6.1.2.1#2, 5.6.1.2.1#4, 5.6.1.2.2#1, 5.6.1.2.2#3, 5.6.1.2.3#3, 5.6.1.2.3#5, 5.6.1.3#1, 5.6.1.5#4, 5.6.3#1, 6.2.1.3#1, 6.2.1.3#2, 6.3.1#2, 6.4.3.9#1, 6.4.4.3.4#8, 6.6.1#4, 6.6.1#5, 6.6.1.1#1, 6.6.1.2#2, 6.8.2.3.1#2 plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

This test must be performed twice. Once with VCONN at 5V, and once with VCONN at 3V

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.

   The following messages are sent using the Primary SOP type unless otherwise stated.

   1. The Tester applies VBUS, VCONN, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) to one cable end. .
   2. Send a BIST Test Data message to the Cable. Check that it responds with a GoodCRC [CAB_PHY_MSG_1].
   3. Send a BIST Test Data message to the Cable using SOP. Check that it only responds if the vendor information states that it will [CAB_PHY_MSG_2].
   4. Send a BIST Test Data message to the Cable using the alternative SOP type. Check that it only responds if the vendor information states that it will [CAB_PHY_MSG_3].
   5. Send a BIST Test Data message to the Cable using Debug_SOP'. Check that it only responds if the vendor information states that it will [CAB_PHY_MSG_4].
   6. Send a BIST Test Data message to the Cable using Debug_SOP''. Check that it only responds if the vendor information states that it will [CAB_PHY_MSG_5].
   7. Reset Cable UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.

   In the following the Tester will send 'Enter Mode Initiator' messages with an SVID not recognized by the UUT, and an Object position of 1. The UUT is expected to respond with GoodCRC and 'Enter Mode NAK', if the message is recognized. This particular message is used as it is equally valid for SOP' and SOP'' in a Cable.

8. The Tester applies VBUS, VCONN, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) to one cable end.
9. In each of the following steps the Tester will send an Enter Mode Initiator message to the Cable UUT and check the cable's response is correct.
10. Send the normal error-free version of the message. Check that an Enter Mode NAK is received [CAB_PHY_MSG_6].
11. Check that GoodCRC is not received and that no Enter Mode NAK is received, from the Cable if a message is sent, with the CRC deliberately corrupted before 4b5b encoding [CAB_PHY_MSG_7].
12. Check that GoodCRC is not received and that no Enter Mode NAK is received, from the Cable if a message is sent, with the CRC deliberately corrupted after 4b5b encoding [CAB_PHY_MSG_8].
13. Check that GoodCRC is not received and that no Enter Mode NAK is received, from the Cable if a message is sent with the payload, deliberately corrupted before 4b5b encoding but after being used for the CRC generation [CAB_PHY_MSG_9].
14. Check that GoodCRC is not received and that no Enter Mode NAK is received, from the Cable if a message is sent with the payload, deliberately corrupted after 4b5b encoding [CAB_PHY_MSG_10].
15. Check that GoodCRC is not received and that no Enter Mode NAK is received, from the Cable if a message is sent containing a reserved 5-bit code used in place of a valid hex code [CAB_PHY_MSG_11].
16. Reset Cable UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.

Procedure for Determining if the Cable UUT Recognizes Hard Reset, Cable Reset and Soft Reset, and acts on them correctly

17. The Tester applies VBUS, VCONN, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) to one cable end. Confirm that out-going Message ID is initialized correctly
18. Send an Enter Mode Initiator message to the UUT (using MessageID = 000b). Check that UUT sends an Enter Mode NAK message, and check that the MessageID in that message header is 000b [CAB_PHY_MSG_12]. Confirm that out-going Message ID is incremented correctly
19. Send an Enter Mode Initiator message to the UUT (using an incremented MessageID). Check that UUT sends an Enter Mode NAK message, and check that the MessageID in that message header is also incremented [CAB_PHY_MSG_13].
20. Repeat previous step until MessageIDs (sent and received) reach 001b for the second time.
21. - For the first pass through this test, send a Cable Reset message.

- For the second pass through this test, send a Hard Reset message.

- For the third pass through this test, send a Soft Reset Message. Check that an Accept message is received with MessageID = 000b [CAB_PHY_MSG_14].

Confirm that out-going Message ID is reset correctly

22. Send an Enter Mode Initiator message to the UUT (using MessageID = 000b), or 001b in the case of Soft Reset). Check that UUT sends an Enter Mode NAK message, and check that the MessageID in that message header is 000b, or 001b in the case of Soft Reset.

Cable Reset: [CAB_PHY_MSG_15],

Hard Reset: [CAB_PHY_MSG_16],

Soft Reset: [CAB_PHY_MSG_17].

Confirm that repeated incoming Message ID is ignored

23. Send an Enter Mode Initiator message to the UUT (using MessageID = 000b). Check that UUT does not send a response (other than GoodCRC) [CAB_PHY_MSG_18].

24. Send an Enter Mode Initiator message to the UUT (using an incremented MessageID). Check that UUT sends an Enter Mode NAK message, and check that the MessageID in that message header is also incremented [CAB_PHY_MSG_19].

25. Repeat previous step until MessageID (sent) reaches 000b for the second time. - For the first pass through this test, send a Cable Reset message. - For the second pass through this test, send a Hard Reset message.

Confirm that repeated incoming Message ID is not ignored for Soft Reset

- For the third pass through this test, send a Soft Reset Message. Check that an Accept message is received with MessageID = 000b [CAB_PHY_MSG_20].

Confirm that incoming Message ID is reset correctly

26. Send an Enter Mode Initiator message to the UUT (using MessageID = 000b, or 001b in the case of Soft Reset). Check that UUT sends an Enter Mode NAK message, and check that the MessageID in that message header is 000b, or 001b in the case of Soft Reset. Cable Reset: [CAB_PHY_MSG_21], Hard Reset: [CAB_PHY_MSG_22], Soft Reset: [CAB_PHY_MSG_23].

27. Reset Cable UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.

28. Repeat the test using the appropriate versions of steps 22 and 26.

Confirm that the CRC is correctly verified according to the rules in Chapter 5 of the PD Specification

29. The Tester applies VBUS, VCONN, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) to one cable end.

30. The Tester constructs and sends a message consisting of:

a. preamble

b. SOP

c. header, indicating anything BUT Soft Reset or Ping

d. payload, consisting of a number of bytes not being a multiple of 4, and not being related to the number of PDOs specified in the header

e. CRC

f. EOP

31. Check that the message is acknowledged by a GoodCRC message.

32. Reset Cable UUT by simulating a tester end cable detach.

33. Repeat test using the other end of the cable. Check that both ends respond with the same information.

14.2.3.4 TDA 1.1.3.2.2 CAB-DP-PHY-MSG DP Cable PHY Level Message Test

See Section 14.2.3.3.

14.2.4 Protocol Specific

14.2.4.1 TDA 1.2.1 CAB-PROT-DISCOV Cable ID Checks

Test Name	CAB-PROT_DISCOV
Test Title	Cable ID Check
Status	Primary Test
Purpose	To perform the appropriate protocol checks relating a Cable Discovery sequence.
Critical for Safety	
Applies to	Electronically Marked C-Cable
Description	This test performs a Discovery procedure for a cable, using SOP' and then if necessary SOP" messages.
Test setup	The Cable UUT is connected by one chosen end to the tester, the other end is left unconnected.
Preconditions	
Assertions Tested	5.6.1.2.2#1, 6.2.1.7#2, 6.4.4.2#1, 6.4.4.3#1, 6.4.4.3.4#8, 6.4.4.3.4#15, 6.4.4.4#3, 6.5.13#1, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

This test must be performed twice. Once with VCONN at 5V, and once with VCONN at 3V.

Test Procedure1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.

2. The Tester applies VBUS, VCONN, Rp (4.7kΩ to 3.3V) and Rd (5.1kΩ to 0V) to one cable end.

3. Wait for tVCONNStable max (100ms) before sending any messages.

4. During the following, respond to any messages received and behave accordingly. Check the appropriateness of such messages.

If the VIF claims that this is a Rev 2.0 cable

5.Send a Discover ID Initiator to the Cable UUT, using SOP', with the Specification Revision set to Rev 3.0.

6. Check that the Cable UUT responds with a valid Discover ID ACK message, using SOP' , and with the Specification Revision set to Rev 2.0. [CAB_PROT_DISCOV_1].

7. Send a Discover ID Initiator to the Cable UUT, using SOP', with the Specification Revision set to reserved value 11b.

8. Check that the Cable UUT responds with a valid Discover ID ACK message, using SOP' , and with the Specification Revision set to Rev 2.0. [CAB_PROT_DISCOV_1].

If the VIF claims that this is a Rev 3.0 cable

9. Send a Discover ID Initiator to the Cable UUT, using SOP', with the Specification Revision set to reserved value 11b.

10. Check that the Cable UUT responds with a valid Discover ID ACK message, using SOP' , and with the Specification Revision set to Rev 2.0. [CAB_PROT_DISCOV_1].

From now on set the Specification Revision set to Rev 2.0

11. Send a Discover ID Initiator to the Cable UUT, using SOP'.

12. Check that the Cable UUT responds with a valid Discover ID ACK message, using SOP' [CAB_PROT_DISCOV_1]. If the Cable UUT responds with NAK it is deemed to have failed. If the Cable UUT responds with BUSY, then the Tester will make four further attempts, with a delay in between of tVDMBusy min (100ms) between each attempt. If the Cable UUT does not respond with ACK after one of these attempts, it is deemed to have failed, and is concluded by proceeding to the last step.

13. Check that the first bit of the preamble of this message is sent after tCableMessage min (750us) but before tVDMReceiverResponse max (15ms), after the last bit of the EOP of the GoodCRC [CAB_PROT_DISCOV_2]. Check that the values in the Discover ID ACK message meet the requirements of PROT-MSG-DATA-VDM-ID-ACK.

14. Send a Discover SVIDs Initiator to the Cable UUT, using SOP'.

15. Check that the Cable UUT responds with a valid Discover SVIDs ACK message or NAK message, using SOP' [CAB_PROT_DISCOV_3]. If the response is NAK, the test is concluded by proceeding to the last step. In the case of a NAK, if the UUT has indicated in its response to 'Discover ID' that it supports Modal Operation, then it is deemed to have failed. If the response is ACK, and the UUT has indicated in its response to 'Discover ID' that it does not support Modal Operation, then it is deemed to have failed. If the Cable UUT responds with BUSY, then the Tester will make four further attempts, with a delay in between of

tVDMBusy min (100ms) between each attempt. If the Cable UUT does not respond with ACK after one of these attempts, it is deemed to have failed.

16. Check that the first bit of the preamble of this message is sent after tCableMessage min (750us) but before tVDMReceiverResponse max (15ms), after the last bit of the EOP of the GoodCRC [CAB_PROT_DISCOV_4]. Check that the values in the Discover SVID ACK message meet the requirements of PROT-MSG-DATA-VDM-SVID-ACK.

17. If the Discover SVID ACK message indicates that there are further SVIDs to fetch, the sequence is repeated from [7] until there are no further SVIDs.

For each SVID:

18. Send a Discover Modes Initiator to the Cable UUT, using SOP'.

19. Check that the Cable UUT responds with a valid Discover Modes ACK message or NAK message, using SOP' [CAB_PROT_DISCOV_5]. If the Cable UUT responds with NAK it is deemed to have failed. If the Cable UUT responds with BUSY, then the Tester will make four further attempts, with a delay in between of tVDMBusy min (100ms) between each attempt. If the Cable UUT does not respond with ACK after one of these attempts, it is deemed to have failed.

20. Check that the first bit of the preamble of this message is sent after tCableMessage min (750us) but before tVDMReceiverResponse max (15ms), after the last bit of the EOP of the GoodCRC [CAB_PROT_DISCOV_6]. Check that the values in the Discover MODES ACK message meet the requirements of PROT-MSG-DATA-VDM-MODES-ACK.

For each of these Modes: In the following we attempt to enter, then exit each mode advertised. Some modes may not be enterable without first entering some other mode. It must be possible to enter at least one mode.

21. Send an Enter Mode Initiator to the Cable UUT, using SOP'.

22. Check that the Cable UUT responds with a valid Enter Mode ACK message or NAK message, using SOP' [CAB_PROT_DISCOV_7]. If the Cable UUT responds with BUSY, then the Tester will make four further attempts, with a delay in between of tVDMBusy min (100ms) between each attempt. If the Cable UUT does not respond with ACK or NAK after one of these attempts, it is deemed to have failed.

23. If the Enter Mode response was an ACK, send an Exit Modes Initiator to the Cable UUT, using SOP'.

24. Check that the Cable UUT responds with a valid Exit Modes ACK message, using SOP' [CAB_PROT_DISCOV_8]. If the response is NAK or BUSY, the test is deemed to have failed.

If the cable has an SOP'' Controller Present, then for each of these same Modes: In the following we attempt to enter, then exit each mode advertised. Some modes may not be enterable without first entering some other mode. It must be possible to enter at least one mode.

25. Send an Enter Mode Initiator to the Cable UUT, using SOP''.

26. Check that the Cable UUT responds with a valid Enter Mode ACK message or NAK message, using SOP' [CAB_PROT_DISCOV_7]. If the Cable UUT responds with BUSY, then the Tester will make four further attempts, with a delay in between of tVDMBusy min (100ms) between each attempt. If the Cable UUT does not respond with ACK or NAK after one of these attempts, it is deemed to have failed.

27. If the Enter Mode response was an ACK, send an Exit Modes Initiator to the Cable UUT, using SOP'.

28. Check that the Cable UUT responds with a valid Exit Modes ACK message, using SOP" [CAB_PROT_DISCOV_8]. If the response is NAK or BUSY, the test is deemed to have failed.

29. Reset Cable UUT by removing VCONN.

30. Repeat test using the other end of the cable.

14.3 Power Delivery Devices - Primary Tests

14.3.1 Physical Layer – Transmit

14.3.1.1 TDA 2.1.1.1 BMC-PHY-TX-EYE BMC Transmitter Eye Diagram Test

Test Name	BMC-PHY-TX-EYE
Test Title	Transmitter Eye Diagram Test
Status	Primary Test
Purpose	To confirm that the transmitted data fulfills the eye diagram mask requirements in Figures 5-23 and 5-24 of the specification. Also checks that UUT correctly implements BIST Carrier Mode 2.
Critical for Safety	
Applies to	Any PD Capable UUT except Cable
Description	The Protocol Tester sends a BIST request to a UUT specifying 'BIST Carrier Mode 2'. The UUT will then transmit a continuous string of BMC encoded alternating "1"s and “0”s in accordance with Section 5.9.4. The eye pattern is measured using the method specified below.
Test setup	Protocol Tester, plus oscilloscope function.
Ping Policy	Send no Pings

Preconditions	
Assertions Tested	5.8.2.5.2#1, 5.8.3.2.1#2, 5.8.3.2.1#3, 5.9.4#1, 6.4.3#7, 6.4.3.6#1, 6.4.3.6#2, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode (BMC-PROC-PD-MODE). Note that for a UUT behaving as a Sink, Rp is implemented as a 4.7kΩ resistor to 3.3V, to give the worst case pullup. The role chosen for the UUT is Sink whenever possible. The capacitive load of the tester is as close to 400pF as practical.
4. The Tester sends a BIST request to the UUT, specifying 'BIST Carrier Mode 2', and checks for a valid and correctly timed protocol response [BMC_PHY_TX_EYE_1].
5. Check that the UUT is transmitting a continuous string of alternating '0' and '1' bits. This functional check shall be sufficiently accurate to ensure that the desired BIST continuous test pattern is present, and not one of the other four, nor a non-continuous transmission mode [BMC_PHY_TX_EYE_2]. The method used for this is left to the discretion of the test equipment vendor. The detailed parameters of the mode will be measured below.
6. Feed the output of the UUT into an oscilloscope type function.
7. Produce an Eye Diagram, using the method specified in section BMC-ALG-CLK-RECOV, and check that the parameters meet the requirements of Figures 5-23 and 5-24 of the Specification [BMC_PHY_TX_EYE_3].
8. Check that the continuous test pattern stops within tBISTContMode max (60ms) of starting [BMC_PHY_TX_ EYE _4].
9. Check that the rise/fall times meet the specification in Table 5-25 [BMC_PHY_TX_ EYE _5].
10. Resets UUT by simulating a tester end cable detach in order to guarantee exiting the BIST Mode.

14.3.1.2 TDA 2.1.1.2 BMC-PHY-TX-BIT BMC Transmit Bit Rate and Bit Rate Drift Test

Test Name	BMC-PHY-TX-BIT
Test Title	Transmitter Bit Rate and Bit Rate Drift Test
Status	Primary Test
Purpose	To confirm that the drift in the transmitted bit rate of a UUT falls within acceptable limits. Also checks that UUT correctly implements BIST Carrier Mode 2.
Critical for Safety	
Applies to	Any PD Capable UUT except Cable
Description	The Protocol Tester sends a BIST request to a UUT specifying 'BIST Carrier Mode 2'. The UUT will then transmit a continuous string of alternating "1"s and "0"s. The data being transmitted are fed into a clock/data recovery function, and the output of this into a frequency counter function. During one or more periods equivalent to the longest possible packet length, the bit rate is measured according to Section 5.8.1.2.1 and Table 5-13 and Table 5-14. This is validated against pBitRate and fBitRate.
Test setup	Protocol Tester, plus clock/data recovery function, plus counter/timer function. The UUT is connected by one chosen end to the tester, the other end is left unconnected. The test is repeated using the other cable end.
Ping Policy	Send no Pings
Preconditions	
Assertions Tested	5.8.1.2.1#1, 5.8.1.2.1#2, 5.9.4#1, 6.4.3#7, 6.4.3.1#3, 6.4.3.9#1, 6.5.8.4#1, plus assertions in any appropriate secondary checks.
Parameters Tested	pBitRate, fBitRate.
Checklist References	

Note: The sample data collected for this test is likely to be the same data collected during the Tx Eye Diagram test BMC-PHY-TX-EYE. Combining these tests is valid if the Tester Vendor considers this appropriate.

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections

of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.

2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode (BMC-PROC-PD-MODE).
4. The Tester sends a BIST request to the UUT, specifying 'BIST Carrier Mode 2', and checks for a valid and correctly timed protocol response [BMC_PHY_TX_BIT_1].
5. Check that the UUT is transmitting a continuous string of alternating '0' and '1' bits. This functional check shall be sufficiently accurate to ensure that the desired BIST continuous test pattern is present, and not one of the other four, nor a non-continuous transmission mode [BMC_PHY_TX_BIT_2]. The method used for this is left to the discretion of the test equipment vendor. The detailed parameters of the mode will be measured below.
6. Use a clock/data recovery function to monitor the signal during the next step. The measurement shall be made using the positive bit edge at the start of a group of four modulated "0101" bits as the significant reference points. (The first zero is therefore a high level.) This reduces the effect of:
    a) Different rise and fall wave forms
    b) Different rise times dependent on value of previous bit.
7. Ensure that at least 32 bits have been detected before starting measurement. The first bit to be included starts at a reference point as defined above, and is referred to below as data bit 0.
8. Measure the bit rate during a 32 bit period. Calculate this as 32, divided by the total period between 9 reference points.
9. Do this from data bit 0 to data bit 31, then from data bit 4 to data bit 35, and repeat until there are 256 bit rate measurements.
10. The bit rate measured from data bit 0 to data bit 31 is taken as the measured fBitRate.
11. Calculate pBitRate as the largest deviation from fBitRate divided by fBitRate, expressed as a percentage.
12. Check that the lowest and highest bit rate values measured fall within fBitRate (270-330 kbps) [BMC_PHY_TX_BIT_3], and that pBitRate (less than 0.25%) is within permitted range [BMC_PHY_TX_BIT_4].
13. Check that the continuous test pattern stops within tBISTContMode max (60ms) of starting [BMC_PHY_TX_BIT_5].
14. Resets UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.

14.3.2 Physical Layer – Receive

14.3.2.1 TDA 2.1.2.1 BMC-PHY-RX-BUSIDL BMC Bus Idle Detection Test

Test Name	BMC-PHY-RX-BUSIDL
Test Title	Bus Idle Detection Test Test
Status	Primary Test
Purpose	Confirm that the UUT accurately recognizes the Bus Idle Condition, and does not interpret valid noise interference as a false Bus Idle Condition
Critical for Safety	No
Applies to	Any PD Capable UUT except Cable
Description	Messages are sent to the UUT under conditions which check the receiver's ability to detect Bus Idle. In steps 1-5, the tester verifies that if the bus is not idle, the UUT does not send a GoodCRC. It achieves this by sending valid transitions during the time window during which the GoodCRC is allowed to be sent. In steps 6-8, the tester verifies that expected levels of noise on the CC line do not prevent the UUT from detecting Bus Idle. It achieves this by sending noise during a time window, and ensuring that the last part of a GoodCRC is sent, but not a complete GoodCRC.
Test setup	Protocol Tester with programmable transmit signal waveform.
Ping Policy	Send no Pings.
Preconditions	
Assertions Tested	6.4.3#10, 6.4.3.9#1 plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable

then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.

3. The Tester gets the UUT into PD Mode (BMC-PROC-PD-MODE).
4. The Protocol Tester sends a BIST request to the UUT, specifying 'BIST Test Data', and checks for a valid and correctly timed protocol response [BMC_PHY_RX_BUSIDL_1]. *This shows that the basic test mechanism is working and prevents the UUT from sending any other messages during the following steps.*

5. Send BIST Test Data message, and then immediately continue sending data zeros for 195us, then open receiver. (This step prevents the UUT from sending a GoodCRC, because the CC line will not be idle during the time in which it is valid to start sending one.)
6. Listen for data from UUT. There must be nothing for 10 ms [BMC_PHY_RX_BUSIDL_2]. If we see a GoodCRC message ending, or a complete GoodCRC, the UUT is deemed to have failed the test.
   See Figure 72 for explanation.
7. Send BIST Test Data message, then continue sending noise (see definition below) for 195+237+6.6us=438.6us, then open receiver. We are expecting the UUT to ignore the noise, and respond with a GoodCRC, so we should detect the end of an already started GoodCRC.
   The time chosen to re-enable the receiver is a point in time during which a legally timed GoodCRC will be encountered at a point after the start of its SOP and before the end of the CRC, regardless of whether this message is sent at the earliest possible opportunity at the fastest rate allowed, or at the latest opportunity at the slowest rate possible.
8. Listen for data from other end - check that we see data present, but do not receive a valid GoodCRC [BMC_PHY_RX_BUSIDL_3]. If we see a GoodCRC it means that it was started later than permitted, for whatever reason.
   If we see no data, then it means that the UUT incorrectly saw the noise as an interfering signal and did not transmit the GoodCRC.
9. Reset UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.

14.3.2.1.1 Timing details

- 237us is the longest time required to send a preamble.
- 6.6us is a margin to ensure not seeing SOP.
- Message could be over in 25us + 149 bits at fastest speed = 472us (leaves minimum 38.4us or 12.7 bits)

14.3.2.1.2 Definition of Noise

- The noise signal shall be transmitted by the same transmit amplifier as the preceding signal, remaining at the same output impedance, to ensure the correct level.
- It shall be a square wave at a frequency of 600 kHz.
- It shall have amplitude of 250mV p/p, biased around 0.55V.

14.3.2.2 TDA 2.1.2.2 BMC-PHY-RX-INT-REJ BMC Receive Interference Rejection Test

Test Name	BMC-PHY-RX-INT-REJ
Test Title	Receive Interference Rejection Test
Status	Primary Test
Purpose	Checks the ability of the receiver to correctly receive signals which are degraded by the worst case aggressor signal, and both the zero offset and worst case offset in the appropriate direction, whilst the bitrate is also set to both minimum and maximum extremes.
Critical for Safety	No
Applies to	Any PD Capable UUT except Cable
Description	The Protocol Tester uses BIST Test Data messages, in the presence of injected interference. The UUT is required to respond with GoodCRC messages, without missing any.
Test setup	USB PD Tester (with ability to add an aggressor signal and an offset to the data signal, while sending minimum and maximum permitted bitrates).
Ping Policy	Send no Pings.
Preconditions	
Assertions Tested	5.8.2.6.4#2, 6.4.3#10, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

This is achieved by using a short cable, and artificially adding an aggressor signal to the transmitted signal. The tester will add voltage offset, corresponding to ground differential, artificially to the signal.

The basic signal transmitted will represent the minimum swing likely to reach the receiver.

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.

For a UUT which can be a Sink:

3. The Tester gets the UUT into PD Mode as a Sink (BMC-PROC-PD-MODE).
4. The Protocol Tester sends a BIST request to the UUT (with incremented MessageID as normal*), specifying 'BIST Test Data', and checks for a valid and correctly timed protocol response [BMC_PHY_RX_INT_REJ_1]. *This shows that the basic test mechanism is working and prevents the UUT from sending any other messages during the following steps.*
5. Wait 15ms to ensure that the UUT understands it is in a BIST test mode, and should not initiate any message sequences*.
6. In the following step, send BIST Test Data message using Group 1 Signal and the noise waveform generated from one of the three approaches described below.
7. Send the 'BIST Test Data' message (without incrementing MessageID*) 13362 times to validate BER, and check that the UUT fails to respond with GoodCRC no more 0 times [BMC_PHY_RX_INT_REJ_2]. *n=4502*(1024/345).*
8. In the following step, send BIST Test Data message using Group 2 Signal and the noise waveform generated from one of the three approaches described below.
9. Send the 'BIST Test Data' message (without incrementing MessageID*) 13362 times to validate BER, and check that the UUT fails to respond with GoodCRC no more 0 times [BMC_PHY_RX_INT_REJ_3]. *n=4502*(1024/345).*
10. Resets UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.

For a UUT which can be a Source:

11. The Tester gets the UUT into PD Mode as a Source (BMC-PROC-PD-MODE).
12. The Protocol Tester sends a BIST request to the UUT (with incremented MessageID as normal*), specifying 'BIST Test Data', and checks for a valid and correctly timed protocol response [BMC_PHY_RX_INT_REJ_4]. *This shows that the basic test mechanism is working and prevents the UUT from sending any other messages during the following steps.*
13. Wait 15ms to ensure that the UUT understands it is in a BIST test mode, and should not initiate any message sequences*.
14. In the following step, send BIST Test Data message using Group 1 Signal and the noise waveform generated from one of the three approaches described below.
15. Send the 'BIST Test Data' message (without incrementing MessageID*) 13362 times to validate BER, and check that the UUT fails to respond with GoodCRC no more 0 times [BMC_PHY_RX_INT_REJ_2]. *n=4502*(1024/345).*
16. In the following step, send BIST Test Data message using Group 3 Signal and the noise waveform generated from one of the three approaches described below.
17. Send the 'BIST Test Data' message (without incrementing MessageID*) 13362 times to validate BER, and check that the UUT fails to respond with GoodCRC no more 0 times [BMC_PHY_RX_INT_REJ_5]. *n=4502*(1024/345).*
18. Resets UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.

Note: The Signaling Groups shown in Table 3 are from Revision 0.908 of the USB Power Delivery Compliance Test Specification. These represent testing at the most recent USB Workshops. The Receiver Interference definition in Revision 1.0 of the CTS is under development.

TABLE 3: GROUP 1/2/3 SIGNAL SPECIFICATIONS

	Nominal Signal	**Group 1 Signal**	**Group 2 Signal**	**Group 3 Signal**
High Level (nom)	1100 mV	1200 mV	790 mV	1290 mV
Low Level (nom)	25 mV	0 mV	-250 mV	250 mV
Bit Rate	300 kb/s	270 kb/s	330 kb/s	330 kb/s
Noise Period **	N/A	608 ns	608 ns	608 ns
Noise Amplitude **	0 mV p/p	100 mV p/p	100 mV p/p	100 mV p/p
Rise/Fall Time	735 ns	735 ns	735 ns	735 ns

Notes on Table 3:

1) The signal rise and fall time shall be increased till the eye of Nominal Signal well touches the Tx Eye Mask. The same rise and fall time shall be used for Group 1, 2, and 3 Signal.
2) The nature of this test is to send a BIST Test Data message repeatedly, with minimum delay between the GoodCRC response from the UUT and the next BIST Test Data message from the tester. There would be a potential for a UUT not to be able to deal with messages of such frequency if the test were not implemented exactly as described above. The first BIST Test Data message must have an incremented MessageID so that the UUT recognizes it as a significant message, and stops originating its own traffic. The 15ms delay before further messages ensures that the UUT has had time to recognize the message. The fact that the MessageID is then not incremented is specified so that the UUT Protocol Engine will not pass the messages up to the Policy Engine, but **will** respond with GoodCRC. This behavior is specified in the PD Specification.

14.3.3 Physical Layer – Miscellaneous

14.3.3.1 TDA 2.1.3.1 BMC-PHY-TERM BMC Termination Impedance Test

Status	Primary Test
Purpose	To confirm that a UUT has a valid impedance when not transmitting.
Critical for Safety	
Applies to	Any PD Capable UUT except Cable
Description	The Protocol Tester chooses a time when the UUT is not transmitting, and measures the impedance of the receiver using a voltage source and resistor.
Test setup	Protocol Tester with voltage generator, resistor, and voltage measurement function.

Ping Policy	Send no Pings
Preconditions	
Assertions Tested	6.4.3#10, 6.4.3.9#1, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Note: It is not practical to directly measure the input impedance of the receiver in the UUT (required to be >= 1 MΩ), as it is masked by the Rp / Rd resistors. Instead we will assume the presence of these resistors and measure that the resulting resistance falls within a valid range.

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode (BMC-PROC-PD-MODE).
4. The Tester sends a BIST request to the UUT, specifying 'BIST Test Data', and checks for a valid and correctly timed protocol response [BMC_PHY_TERM_1]. This shows that the basic test mechanism is working and prevents the UUT from sending any other messages during the following steps.
5. Check that the voltage on the CC line falls within the expected range, knowing the range of values of the Rp and Rd resistors [BMC_PHY_TERM_2].
6. Reset UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode. Verify that UUT does not modify voltage levels in any received message waveform.
7. The Tester gets the UUT into PD Mode (BMC-PROC-PD-MODE).
8. The Tester sends a BIST request to the UUT, specifying 'BIST Test Data', and checks for a valid and correctly timed protocol response [BMC_PHY_TERM_1]. This shows that the basic test mechanism is working and prevents the UUT from sending any other messages during the following steps.
9. Check that signal voltages on the CC line of -300mV and 1500mV are not modified at the receiver input by more than the tester tolerances may produce. The actual test method is left to the discretion of the implementer.
10. Reset UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.

14.3.3.2 TDA 2.1.3.2 BMC-PHY-MSG BMC PHY Level Message Test

Status	Primary Test
Purpose	To validate the PHY level behavior of message exchanges. To confirm the PHY level behavior of the UUT in relation to Cable Reset and Hard Reset.
Critical for Safety	
Applies to	Any PD Capable UUT except Cable
Description	The Protocol Tester sends a sequence of messages both correct and with deliberate errors and validates the correct behavior in each case. Protocol Tester sends Hard Reset, Soft Reset and Cable Reset messages to the UUT, and confirms correct operation by the UUT.
Test setup	Protocol Tester with control over low level packet generation.
Ping Policy	Send no Pings
Preconditions	
Assertions Tested	5.3#1, 5.3#2, 5.5#1, 5.5#2, 5.6#1, 5.6.1.1#2, 5.6.1.1#3, 5.6.1.1#4, 5.6.1.2.2#5, 5.6.1.2.2#6, 5.6.1.2.3#7, 5.6.1.3#1, 5.6.1.5#4, 5.6.1.5#5, 5.6.3#1, 6.2.1.3#1,1.3#2, 6.3.1#2, 6.4.3.9#1, 6.6.1.1#1, 6.8.2.3.1#1, 8.3.3.8.1.2#1, 8.3.3.8.1.2#2, 8.3.3.9.1.1#2, 8.3.3.10.2.2#1, 8.3.3.10.2.2#2, 8.3.3.10.2.3#1, 8.3.3.10.2.3#2, 8.3.3.10.11.1#5 plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

1.During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections xof this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.

2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker. The following messages are sent using SOP unless otherwise stated.

3. The Tester gets the UUT into PD Mode (as a Sink if possible, otherwise as a Source) (BMCPROC-PD-MODE).

4. Send a BIST Test Data message to the UUT. Check that it responds with a GoodCRC [BMC_PHY_MSG_1].

5. If the UUT is a DFP, and vendor specifies that it will not respond to SOP', send a BIST Test Data message to the UUT using SOP' and check that it does not respond. If the UUT is a UFP, send a BIST Test Data message to the UUT using SOP' and check that it does not respond. If the UUT is a DFP, and vendor specifies that it will respond to SOP' skip this step. [BMC_PHY_MSG_2].

6. If the UUT is a DFP, and vendor specifies that it will not respond to SOP", send a BIST Test Data message to the UUT using SOP" and check that it does not respond. If the UUT is a UFP, send a BIST Test Data message to the UUT using SOP' and check that it does not respond. If the UUT is a DFP, and vendor specifies that it will respond to SOP" skip this step. [BMC_PHY_MSG_3].

7. Send a BIST Test Data message to the UUT using Debug_SOP'. Check that it does not respond, unless specified by vendor that it will [BMC_PHY_MSG_4].

8. Send a BIST Test Data message to the UUT using Debug_SOP". Check that it does not respond, unless specified by vendor that it will [BMC_PHY_MSG_5].

9. Reset UUT by simulating a tester end cable detach, in order to guarantee exiting the BIST Mode.

In each of the following steps referring to 'the message', the Tester will send a Get_Source_Cap message to the UUT if it is being tested as a Sink, or a Get_Sink_Cap message to the UUT if it is being tested as a Source, UUT and check the UUT's response is correct. We expect either a Reject message or an appropriate Capabilities message, if the message is recognized, otherwise no related response.

10. The Tester gets the UUT into PD Mode (as a Sink if possible, otherwise as a Source) (BMCPROC-PD-MODE).

11. Send the normal error-free version of the message. Check that a valid response message is received [BMC_PHY_MSG_6].

12. Check that GoodCRC is not received and that no response message is received, from the UUT if a message is sent, with the CRC deliberately corrupted before 4b5b encoding [BMC_PHY_MSG_7]. 13. Check that GoodCRC is not received and that no response message is received, from the UUT if a message is sent, with the CRC deliberately corrupted after 4b5b encoding [BMC_PHY_MSG_8].

14. Check that GoodCRC is not received and that no response message is received, from the UUT if a message is sent with the payload, deliberately corrupted before 4b5b encoding but after being used for the CRC generation [BMC_PHY_MSG_9].

15. Check that GoodCRC is not received and that no response message is received, from the UUT if a message is sent with the payload, deliberately corrupted after 4b5b encoding [BMC_PHY_MSG_10].

16. Check that GoodCRC is not received and that no response message is received, from the UUT if a message is sent containing a reserved 5-bit code used in place of a valid hex code [BMC_PHY_MSG_11]. [Note exactly which code]

17. Reset UUT by simulating a tester end cable detach, in order to start again from a known state.

Confirm that out-going Message ID is initialized correctly (on establish PD-Mode) Confirm that out-going Message ID is incremented correctly (on any message)

18. The Tester gets the UUT into PD Mode (as a Sink if possible, otherwise as a Source) (BMCPROC-PD-MODE].

19. Send an appropriate Get Capabilities message to the UUT. Check that UUT sends an appropriate response message.

20. During the previous two steps check that the MessageID contained in the messages from the UUT follow the rules about initial value [BMC_PHY_MSG_12] and incrementing [BMC_PHY_MSG_13].

Confirm that the UUT ignores Cable Reset (Skip to Step 27 if UUT can only behave as a Source)

21. Send an appropriate Get Capabilities message to the UUT. Check that UUT sends an appropriate response message.

22. Send a Cable Reset to the UUT.

23. Send an appropriate Get Capabilities message to the UUT. Check that UUT sends an appropriate response message.

24. Send a Cable Reset to the UUT.

25. Send an appropriate Get Capabilities message to the UUT. Check that UUT sends an appropriate response message.

26. Check that the MessageID in any messages received from the UUT (including unexpected ones) starting at step 20 are always incrementing [BMC_PHY_MSG_15].

27. Reset UUT by simulating a tester end cable detach, in order to start again from a known state.

Confirm that repeated incoming Message ID is ignored

28. The Tester gets the UUT into PD Mode (as a Sink if possible, otherwise as a Source) (BMCPROC-PD-MODE].

29. Send appropriate Get Capabilities message to the UUT with NO MessageID increment. Check that UUT does not send a response (other than GoodCRC). [BMC_PHY_MSG_18].

30. Reset UUT by simulating a tester end cable detach, in order to start again from a known state.

Confirm that out-going Message ID is reset correctly on Hard Reset

31. The Tester gets the UUT into PD Mode(as a Sink if possible, otherwise as a Source) (BMCPROC-PD-MODE].

32. The Tester sends Hard Reset to UUT.

33. Check that the UUT performs the correct steps to re-enter PD-MODE (whether it is a source or a sink). The tester automatically performs its role in this. [BMC_PHY_MSG_16]

34. Reset UUT by simulating a tester end cable detach, in order to start again from a known state.

Confirm that out-going Message ID is reset correctly on Soft Reset

35. The Tester gets the UUT into PD Mode (as a Sink if possible, otherwise as a Source) (BMCPROC-PD-MODE].

36. The Tester sends Soft Reset to UUT.

37. Check that the UUT sends an Accept message [BMC_PHY_MSG_14], and then performs the correct steps to re-cover from Soft Reset (whether it is a source or a sink). The tester automatically performs its role in this.

38. Reset UUT by simulating a tester end cable detach, in order to start again from a known state.

Confirm that the CRC is correctly verified according to the rules in Chapter 5 of the PD Specification 39. The Tester gets the UUT into PD Mode (as a Sink if possible, otherwise as a Source) (BMCPROC-PD-MODE].

40. The Tester sends a BIST Test Data message to the UUT. Check that it responds with a GoodCRC [BMC_PHY_MSG_1].

41. The Tester constructs and sends a message consisting of:

a. preamble

b. SOP

c. header, indicating anything BUT Soft Reset or Ping

d. payload, consisting of a number of bytes not being a multiple of 4, and not being related to the number of PDOs specified in the header

e. CRC

f. EOP

42. Check that the message is acknowledged by a GoodCRC message.

43. Reset UUT by simulating a tester end cable detach, in order to start again from a known state.

(Only if Testing to Rev 2.0) Confirm that a Rev 3.0 Extended Message is responded to with a GoodCRC

44. The Tester gets the UUT into PD Mode(as a Sink if possible, otherwise as a Source) (BMCPROC-PD-MODE].

45. The Tester sends a Get_Manufacturer_Info Extended message (with Rev 3.0)

46. Check that the message is acknowledged by a GoodCRC message.

47. Reset UUT by simulating a tester end cable detach, in order to start again from a known state.

14.3.4 Protocol Specific

14.3.4.1 TDA 2.2.1 BMC-PROT-SEQ-GETCAPS Get_Source_Cap and Get_Sink_Cap Test

Status	Primary Test
Purpose	To confirm that a UUT responds correctly to a Get_Source_Cap and Get_Sink_Cap request.
Critical for Safety	No
Applies to	Any PD Capable UUT except Cable
Description	A Get_Source_Cap message is sent to the UUT, to verify that it responds correctly. A Get_Sink_Cap message is sent to the UUT, to verify that it responds correctly.
Test setup	Protocol Tester
Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	6.3.7#1, 6.3.7#2, 6.3.8#1, 6.3.8#2, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

For UUT capable of being a provider

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode as a Source(PROC-PD-MODE).
4. Send Get_Source_Cap.
5. Check that a Reject message is received if the UUT is a Consumer only [BMC_PROT_SEQ_GETCAPS_1]. Else check that valid Source Capabilities are received. (If the UUT is currently a Source, a Request will be sent by the Tester.) [BMC_PROT_SEQ_GETCAPS_2]
6. Send Get_Sink_Cap.

7. Check that a Reject message is received if the UUT is a Provider only [BMC_PROT_SEQ_GETCAPS _3]. Else check that valid Sink Capabilities are received. [BMC_PROT_SEQ_GETCAPS _4]
8. Emulate a tester-end detach.

For UUT capable of being a consumer

9. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
10. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
11. The Tester gets the UUT into PD Mode as a Sink (PROC-PD-MODE).
12. Send Get_Source_Cap.
13. Check that a Reject message is received if the UUT is a Consumer only [BMC_PROT_SEQ_GETCAPS_1]. Else check that valid Source Capabilities are received. (If the UUT is currently a Source, a Request will be sent by the Tester.) [BMC_PROT_SEQ_GETCAPS_2]
14. Send Get_Sink_Cap.
15. Check that a Reject message is received if the UUT is a Provider only [BMC_PROT_SEQ_GETCAPS _3]. Else check that valid Sink Capabilities are received. [BMC_PROT_SEQ_GETCAPS _4]
16. Emulate a tester-end detach.

14.3.4.2 TDA 2.2.2.1 BMC-PROT-SEQ-CHKCAB-P-PC Check Cable Capabilities (3A Marked)

Status	Primary Test
Purpose	To confirm that a UUT does not offer more than 3A, on a 3A-only cable.
Critical for Safety	No
Applies to	DRP, Provider, or Provider/Consumer
Description	The Source Capabilities from the UUT are checked to ensure that the UUT does not offer more current than the connecting cable is capable of supporting. The UUT is also checked to confirm that it sends Discover ID to the cable (using SOP').

Test setup	Protocol Tester
Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	3.3.2#1, 6.4.4.2#1, 6.4.4.3.1#2, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

If the vendor declared source capabilities never exceed 3A, then the test is for information only. The following test is performed, either with an E-marked cable cable of supporting 3A only, or by using a special unmarked test cable, and simulating an E-marker in the Tester, supporting 3A only.

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 3A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 3A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode as a Source (PROC-PD-MODE).
4. Check that the UUT sends a DiscoverID message to the cable, using SOP'. [BMC_PROT_SEQ_CHKCAB_P_PC_1]
5. For a 'Fixed' or 'Variable' supply, check that none of the Source Capabilities offered exceeds 3A. For a 'Battery' supply check that the power offered does not exceed the max Voltage offered times 3A. [BMC_PROT_SEQ_CHKCAB_ P_PC _2]
6. Emulate a tester-end detach.

14.3.4.3 TDA 2.2.2.2 BMC-PROT-SEQ-NOMRK-P-PC Check Cable Capabilities (Unmarked)

Status	Primary Test
Purpose	To confirm that a UUT does not offer more than 3A, on an unmarked cable.
Critical for Safety	No
Applies to	DRP, Provider, or Provider/Consumer
Description	The Source Capabilities from the UUT are checked to ensure that the UUT does not offer more current than the connecting cable is capable of supporting. The UUT is also checked to confirm that it sends Discover ID to the cable (using SOP').
Test setup	Protocol Tester
Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	3.3.2#1, 6.4.4.2#1, 6.4.4.3.1#2, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

If the vendor declared source capabilities never exceed 3A, then the test is for information only. The following test is performed using a special unmarked test cable, and NOT simulating an E-marker in the Tester.

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 3A or 5A unmarked cable. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode as a Source (PROC-PD-MODE).
4. For a 'Fixed' or 'Variable' supply, check that none of the Source Capabilities offered exceeds 3A. For a 'Battery' supply check that the power offered does not exceed the max Voltage offered times 3A. [BMC_PROT_SEQ_NOMRK_P_PC _2]
5. Emulate a tester-end detach.

14.3.4.4 TDA 2.2.2.3 BMC-PROT-SEQ-CHKCAB-CP-ACC Check Cable Capabilities (3A Marked) After PR_Swap

Status	Primary Test
Purpose	To confirm that a UUT does not offer more than 3A, on a 3A-only cable, in a power swapped state.
Critical for Safety	No
Applies to	DRP, Consumer / Provider
Description	The Source Capabilities from the UUT are checked to ensure that the UUT does not offer more current than the connecting cable is capable of supporting. The UUT is also checked to confirm that it sends Discover ID to the cable (using SOP').
Test setup	Protocol Tester
Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	3.3.2#1, 6.4.4.2#1, 6.4.4.3.1#2, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

If the vendor declared source capabilities never exceed 3A, then the test is for information only. The following test is performed, either with an E-marked cable cable of supporting 3A only, or by using a special unmarked test cable, and simulating an E-marker in the Tester, supporting 3A only.

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 3A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 3A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode as a Sink (PROC-PD-MODE).

4. Change Tester from being a Source to being a Sink as follows:
    a. The Tester requests a power role swap (PROT-PROC-SWAP-TSTR), which may initially be declined with a Wait, while the UUT establishes what the Tester sink requirements are.
    b. After having been asked for and then having sent the Sink Capabilities, the Tester once again requests a role swap (PROT-PROC-SWAP-TSTR).
    c. As the vendor has stated that the PR_Swap will be accepted, and the correct condition is met, a failure to role swap at this point is deemed a test failure. [BMC_PROT_SEQ_CHKCAB_ CP_ACC _1]
5. Check that the UUT sends a DiscoverID message to the cable, using SOP'. [BMC_PROT_SEQ_CHKCAB_CP_ACC_2]
6. For a 'Fixed' or 'Variable' supply, check that none of the Source Capabilities offered exceeds 3A. For a 'Battery' supply check that the power offered does not exceed the max Voltage offered times 3A. [BMC_PROT_SEQ_CHKCAB_ CP_ACC _3]
7. Emulate a tester-end detach.

14.3.4.5 TDA 2.2.2.4 BMC-PROT-SEQ-CHKCAB-NOMRK-CP-ACC Check Cable Capabilities (Unmarked) After PR_Swap

Status	Primary Test
Purpose	To confirm that a UUT does not offer more than 3A, on an unmarked cable, in a power swapped state.
Critical for Safety	No
Applies to	DRP, Consumer / Provider
Description	The Source Capabilities from the UUT are checked to ensure that the UUT does not offer more current than the connecting cable is capable of supporting. The UUT is also checked to confirm that it sends Discover ID to the cable (using SOP').
Test setup	Protocol Tester
Ping Policy	Send Pings where possible

Preconditions	
Assertions Tested	3.3.2#1, 6.4.4.2#1, 6.4.4.3.1#2, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

If the vendor declared source capabilities never exceed 3A, then the test is for information only. The following test is performed using a special unmarked test cable, and NOT simulating an E-marker in the Tester.

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 3A or 5A unmarked cable. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode as a Sink (PROC-PD-MODE).
4. Change Tester from being a Source to being a Sink as follows:
    a. The Tester requests a power role swap (PROT-PROC-SWAP-TSTR), which may initially be declined with a Wait, while the UUT establishes what the Tester sink requirements are.
    b. After having been asked for and then having sent the Sink Capabilities, the Tester once again requests a role swap (PROT-PROC-SWAP-TSTR).
    c. As the vendor has stated that the PR_Swap will be accepted, and the correct condition is met, a failure to role swap at this point is deemed a test failure. [BMC_PROT_SEQ_NOMRK_CP_ACC _1]
5. For a 'Fixed' or 'Variable' supply, check that none of the Source Capabilities offered exceeds 3A. For a 'Battery' supply check that the power offered does not exceed the max Voltage offered times 3A. [BMC_PROT_SEQ_NOMRK_CP_ACC _3]
6. Emulate a tester-end detach.

14.3.4.6 TDA 2.2.3 BMC-PROT-SEQ-DRSWAP DR_Swap Test

Status	Primary Test
Purpose	To confirm that a UUT responds correctly to a DR_Swap request.
Critical for Safety	No
Applies to	Any PD Capable UUT except Cable

Description	A DR_Swap message is sent to the UUT, to verify that it responds correctly.
Test setup	Protocol Tester
Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	4.4.1#4, 6.3.10#6, 6.4.4.2#1, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. Set default tester response to PR_Swap to Reject.
Set default tester response to DR_Swap to Reject.
Set default tester response to VCONN_Swap to Reject.
4. The Tester gets the UUT into PD Mode as a Source (PROC-PD-MODE).
5. At the earliest possible stage the Tester requests a DR_Swap. The UUT may initially send a Wait and then perform other operations. The Tester continues, for up to 10 seconds, to request a DR_Swap, until either Reject or Accept is received.
6. Check that a Reject message is received from the UUT, if DR_Swap_to_UFP is not supported [BMC_PROT_SEQ_DRSWAP_1]. Else check that an Accept message is received from the UUT. [BMC_PROT_SEQ_ DRSWAP_2]
7. If the DR_Swap was rejected, then skip to step 10.
8. At the earliest possible stage the Tester requests a further DR_Swap. The UUT may initially send a Wait and then perform other operations. The Tester continues, for up to 10 seconds, to request a DR_Swap, until either Reject or Accept is received.
9. Check that a Reject message is received from the UUT, if DR_Swap_to_DFP is not supported [BMC_PROT_SEQ_DRSWAP_3]. Else check that an Accept message is received from the UUT. [BMC_PROT_SEQ_ DRSWAP_4]
10. Emulate a tester-end detach.

If UUT is able to start as Sink

11. The Tester gets the UUT into PD Mode as a Sink (PROC-PD-MODE).
12. At the earliest possible stage the Tester requests a DR_Swap. The UUT may initially send a Wait and then perform other operations. The Tester continues, for up to 10 seconds, to request a DR_Swap, until either Reject or Accept is received.
13. Check that a Reject message is received from the UUT, if DR_Swap_to_DFP is not supported [BMC_PROT_SEQ_DRSWAP_5]. Else check that an Accept message is received from the UUT. [BMC_PROT_SEQ_ DRSWAP_6]
14. If the DR_Swap was rejected, then skip to step 17.
15. At the earliest possible stage the Tester requests a further DR_Swap. The UUT may initially send a Wait and then perform other operations. The Tester continues, for up to 10 seconds, to request a DR_Swap, until either Reject or Accept is received.
16. Check that a Reject message is received from the UUT, if DR_Swap_to_UFP is not supported [BMC_PROT_SEQ_DRSWAP_7]. Else check that an Accept message is received from the UUT. [BMC_PROT_SEQ_ DRSWAP_8]
17. Emulate a tester-end detach.

14.3.4.7 TDA 2.2.4 BMC-PROT-SEQ-VCSWAP Vconn_Swap Test

Status	Primary Test
Purpose	To confirm that a UUT responds correctly to a Vconn_Swap request.
Critical for Safety	No
Applies to	Any PD Capable UUT except Cable
Description	A DR_Swap message is sent to the UUT, to verify that it responds correctly.
Test setup	Protocol Tester
Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	4.4.1#4, 6.3.10#6, 6.4.4.2#1, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown

above in 'Assertions Tested'. 2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.

3. Set default tester response to PR_Swap to Reject.

Set default tester response to DR_Swap to Accept.

Set default tester response to VCONN_Swap to Reject.

If UUT is able to start as Source

4. The Tester gets the UUT into PD Mode as a Source (PROC-PD-MODE), applying Ra to the remote end of the non-CC line.

5. Check that, if Type_C_Sources_VCONN is YES, then VCONN is present at the remote end of the non-CC line [BMC_PROT_SEQ_VCSWAP_6]. Check that, if Type_C_Sources_VCONN is NO, then VCONN is not present at the remote end of the non-CC line [BMC_PROT_SEQ_VCSWAP_6].

6. At the earliest possible stage the Tester requests a VCONN_Swap. The UUT may initially send a Wait and then perform other operations. The Tester continues, for up to 10 seconds, to request a VCONN_Swap, until either Reject or Accept is received.

7. Check that a Reject message is received from the UUT, if VCONN_Swap_to_Off is not supported [BMC_PROT_SEQ_ VCSWAP _1]. Else check that an Accept message is received from the UUT. [BMC_PROT_SEQ_ VCSWAP _2]

8. If the VCONN_Swap was rejected, then skip to step 15.

9. Send a PS_RDY message.

10. Check that VCONN is not present at the remote end of the non-CC line [BMC_PROT_SEQ_VCSWAP_7].

11. At the earliest possible stage the Tester requests a further VCONN _Swap. The UUT may initially send a Wait and then perform other operations. The Tester continues, for up to 10 seconds, to request a VCONN _Swap, until either Reject or Accept is received.

12. Check that a Reject message is received from the UUT, if VCONN_Swap_to_On is not supported [BMC_PROT_SEQ_ VCSWAP _3]. Else check that an Accept message is received from the UUT. [BMC_PROT_SEQ_ VCSWAP _4]

13. Check that a PS_RDY message is received from the UUT [BMC_PROT_SEQ_VCSWAP_5].

14. Check that VCONN is present at the remote end of the non-CC line [BMC_PROT_SEQ_VCSWAP_6].

15. Emulate a tester-end detach.

If UUT is able to start as sink

16. The Tester gets the UUT into PD Mode as a Sink (PROC-PD-MODE), applying Ra to the remote end of the non-CC line.

17. Check that VCONN is not present at the remote end of the non-CC line [BMC_PROT_SEQ_VCSWAP_7].

18. At the earliest possible stage the Tester requests a VCONN _Swap. The UUT may initially send a Wait and then perform other operations. The Tester continues, for up to 10 seconds, to request a VCONN _Swap, until either Reject or Accept is received.

19. Check that a Reject message is received from the UUT, if VCONN_Swap_to_On is not supported [BMC_PROT_SEQ_ VCSWAP _8]. Else check that can Accept message is received from the UUT. [BMC_PROT_SEQ_ VCSWAP _9]

20. If the VCONN_Swap was rejected, then skip to step 28.

21. Check that a PS_RDY message is received from the UUT [BMC_PROT_SEQ_VCSWAP_10]. 22. Check that VCONN is present at the remote end of the non-CC line [BMC_PROT_SEQ_VCSWAP_11].

23. At the earliest possible stage the Tester requests a further VCONN_Swap. The UUT may initially send a Wait and then perform other operations. The Tester continues, for up to 10 seconds, to request a VCONN_Swap, until either Reject or Accept is received.

24. Check that a Reject message is received from the UUT, if VCONN_Swap_to_Off is not supported [BMC_PROT_SEQ_ VCSWAP _12]. Else check that an Accept message is received from the UUT. [BMC_PROT_SEQ_VCSWAP_13]

25. If the VCONN _Swap was rejected, then skip to step 11.

26. Send a PS_RDY message.

27. Check that VCONN is not present at the remote end of the non-CC line [BMC_PROT_SEQ_VCSWAP_1

28. Emulate a tester-end detach

14.3.4.8 TDA 2.2.5 BMC-PROT-DISCOV ID Checks Test

Status	Primary Test
Purpose	To perform the appropriate protocol checks relating a Cable Discovery sequence.
Critical for Safety	
Applies to	DRP, Consumer, Consumer/Provider
Description	This test performs a Discovery procedure for a UUT, using SOP messages.
Test setup	The UUT is connected to the tester.

Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	6.3.3#3, 6.3.4#3, 6.3.9#6, 6.3.9#7, 6.3.9#8, 6.3.9#9, 6.3.12#3 plus assertions in any appropriate secondary checks. Parameters
Parameters Tested	
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.

2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.

1. The Tester gets the UUT into PD Mode (PROC-PD-MODE) as a Consumer.
2. During the following, respond to any messages received and behave accordingly. Check the appropriateness of such messages.

5. Send a Discover ID Initiator to the UUT, using SOP.

6. Check that the UUT responds with a valid Discover ID ACK message, using SOP [BMC_PROT_DISCOV_1]. If the UUT responds with NAK it is deemed to have failed. If the UUT responds with BUSY, then the Tester will make four further attempts, with a delay in between of tVDMBusy min (100ms) between each attempt. If the UUT does not respond with ACK after one of these attempts, it is deemed to have failed, and is concluded by proceeding to the last step.

7. Check that the first bit of the preamble of this message is sent after tInterFrameGap min (25us) but before tVDMReceiverResponse max (15ms), after the last bit of the EOP of the GoodCRC [BMC_PROT_DISCOV_2]. Check that the values in the Discover ID ACK message meet the requirements of PROT-MSG-DATA-VDM-ID-ACK.

8. Send a Discover SVIDs Initiator to the UUT, using SOP.

9. Check that the UUT responds with a valid Discover SVIDs ACK message or NAK message, using SOP [BMC_PROT_DISCOV_3]. If the response is NAK, the test is concluded by proceeding to the last step. In the case of a NAK, if the UUT has indicated in its response to 'Discover ID' that it supports Modal Operation, and then it is deemed to have failed. If the response is ACK, and the UUT has indicated in its response to 'Discover ID' that it does not support Modal Operation, then it is deemed to have failed. If the UUT responds with BUSY, then the Tester will make four further attempts, with a delay in between of tVDMBusy min (100ms) between each attempt. If the UUT does not respond with ACK after one of these attempts, it is deemed to have failed.

10. Check that the first bit of the preamble of this message is sent after tInterFrameGap min (25us) but before tVDMReceiverResponse max (15ms), after the last bit of the EOP of the GoodCRC [BMC_PROT_DISCOV_4]. Check that the values in the Discover SVID ACK message meet the requirements of PROT-MSG-DATA-VDM-SVID-ACK.

11. If the Discover SVID ACK message indicates that there are further SVIDs to fetch, the sequence is repeated from [7] until there are no further SVIDs.

For each SVID:

11. Send a Discover Modes Initiator to the UUT, using SOP.

13. Check that the UUT responds with a valid Discover Modes ACK message or NAK message, using SOP [BMC_PROT_DISCOV_5]. If the UUT responds with NAK it is deemed to have failed. If the UUT responds with BUSY, then the Tester will make four further attempts, with a delay in between of tVDMBusy min (100ms) between each attempt. If the UUT does not respond with ACK after one of these attempts, it is deemed to have failed.
14. Check that the first bit of the preamble of this message is sent after tInterFrameGap min (25us) but before tVDMReceiverResponse max (15ms), after the last bit of the EOP of the GoodCRC [BMC_PROT_DISCOV_6]. Check that the values in the Discover MODES ACK message meet the requirements of PROT-MSG-DATA-VDM-MODES-ACK.

For each of these Modes: In the following we attempt to enter, then exit each mode advertised. Some modes may not be enterable without first entering some other mode. It must be possible to enter at least one mode.

15. Send an Enter Mode Initiator to the UUT, using SOP.
16. Check that the UUT responds with a valid Enter Mode ACK message or NAK message, using SOP [BMC_PROT_DISCOV_7]. If the UUT responds with BUSY, then the Tester will make four further attempts, with a delay in between of tVDMBusy min (100ms) between each attempt. If the UUT does not respond with ACK or NAK after one of these attempts, it is deemed to have failed.

17. If the Enter Mode response was an ACK, send an Exit Modes Initiator to the UUT, using SOP.
18. Check that the UUT responds with a valid Exit Modes ACK message, using SOP [BMC_PROT_DISCOV_8]. If the response is NAK or BUSY, the test is deemed to have failed.
19. Emulate a tester-end detach.

14.3.4.9 TDA 2.2.6 BMC-PROT-SEQ-PRSWAP PR_Swap Test (Provider/Consumer)

Status	Primary Test
Purpose	To confirm that a UUT always responds appropriately to PR_Swap requests..
Critical for Safety	No
Applies to	Any UUT
Description	The UUT is requested to do a Power Role Swap, under conditions favourable to such a swap. We confirm that the PR_Swap is responded to in the way specified in the Vendor Information File
Test setup	Protocol Tester
Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	6.3.3#4, 6.3.4#4, 6.3.11#3, 6.3.11#5, 6.3.11#7, 6.3.11#8, 6.3.12#4 plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure

For any UUT capable of being a Source (else proceed to the second half of the test description

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'. 2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.

3. Set default tester response to PR_Swap to Reject.

Set default tester response to DR_Swap to Accept.

Set default tester response to VCONN_Swap to Accept.

Set the Tester Unconstrained Power bit to 1.

Set Tester Dual-Role Power to 1.

4. The Tester gets the UUT into PD Mode as a Source (PROC-PD-MODE).

5. The Tester gets the UUT Sink Capabilities, and changes its own Source Capabilities to match the UUT Sink Capabilities, and changes its Unconstrained Power bit to 1, giving the best conditions for the PR_Swap to be accepted.

6. At the earliest possible stage the Tester requests a PR_Swap. The UUT may initially send a Wait and then fetch the Tester Source Capabilities. The Tester continues, for up to 10 seconds, to request a PR_Swap.

7. By the end of this time, check that the response from the UUT matches the VIF declared response (Accepts_PR_Swap_as_Source: YES/NO) [BMC_PROT_SEQ_SWAP_REJ_1]. Accept and Reject are the only options to be considered for a PASS. Continued Wait response after 10 seconds is considered to be a FAIL.

8. If the UUT has sent a Reject message then skip to step 12.

9. (The UUT is now a Sink, the tester is Source; has just completed a PR_Swap and has a contract.) The Tester gets the UUT Source Capabilities, and changes its own Sink Capabilities to match the first PDO of the UUT Source Capabilities, and changes its Unconstrained Power bit to 0, giving the best conditions for the PR_Swap to be accepted. Send these new Capabilities to the UUT, and allow it to request a new contract.

10. Now request a PR_Swap. The UUT may initially send a Wait and then fetch the Tester Sink Capabilities. The Tester continues, for up to 10 seconds, to request a PR_Swap.

11. By the end of this time, check that the response from the UUT matches the VIF declared response (Accepts_PR_Swap_as_Sink: YES/NO) [BMC_PROT_SEQ_SWAP_REJ_2]. Accept and Reject are the only options to be considered for a PASS. Continued Wait response after 10 seconds is considered to be a FAIL.

12. Emulate a tester-end detach.

For any UUT capable of being a Sink (if not, test is complete)

13. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.

14. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive

cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.

15. Set default tester response to PR_Swap to Reject.

Set default tester response to DR_Swap to Accept.

Set default tester response to VCONN_Swap to Accept.

Set the Tester Unconstrained Power bit to 0.

Set Tester Dual-Role Power to 1.

16. The Tester gets the UUT into PD Mode as a Sink (PROC-PD-MODE).

17. The Tester gets the UUT Source Capabilities, and changes its own Sink Capabilities to match the first PDO of the UUT Source Capabilities, and to state that the Tester does not have Unconstrained Power, giving the best conditions for the PR_Swap to be accepted.

18. At the earliest possible stage the Tester requests a PR_Swap. The UUT may initially send a Wait and then fetch the Tester Sink Capabilities. The Tester continues, for up to 10 seconds, to request a PR_Swap.

19. By the end of this time, check that the response from the UUT matches the VIF declared response (Accepts_PR_Swap_as_Sink: YES/NO) [BMC_PROT_SEQ_SWAP_REJ_3]. Accept and Reject are the only options to be considered for a PASS. Continued Wait response after 10 seconds is considered to be a FAIL.

20. If the UUT has sent a Reject message then skip to step 24.

21. (The UUT is now a Source, the tester is Sink; has just completed a PR_Swap and has a contract.) The Tester gets the UUT Sink Capabilities, and changes its own Source Capabilities to match the UUT Sink Capabilities, and changes its Unconstrained Power bit to 1, giving the best conditions for the PR_Swap to be accepted.

22. Now request a PR_Swap. The UUT may initially send a Wait and then fetch the Tester Sink Capabilities. The Tester continues, for up to 10 seconds, to request a PR_Swap.

23. By the end of this time, check that the response from the UUT matches the VIF declared response (Accepts_PR_Swap_as_Source: YES/NO) [BMC_PROT_SEQ_SWAP_REJ_4]. Accept and Reject are the only options to be considered for a PASS. Continued Wait response after 10 seconds is considered to be a FAIL. Sending Reject when parameter Accepts_PR_Swap_as_Source is YES, is deemed to only attract a WARNING.

Note: this WARNING would result from the UUT assuming the state of the Unconstrained Power bit, rather than the logically correct behaviour of sending a Wait, and then fetching the Tester Sink Capabilities to determine the up-to-date state of this bit.

24. Emulate a tester-end detach.

14.3.4.10 TDA 2.2.7 BMC-PROT-BIST-NOT-5V-SRC BIST Functionality at Above 5V Test

Status	Primary Test
Purpose	To confirm that the UUT ignores BIST messages if Vbus is above 5V.
Critical for Safety	Yes
Applies to	DRP, Provider, Provider/Consumer (capable of supplying a voltage above 5V).
Description	The Source is made to supply a voltage above 5V, and then a BIST message is sent to it. It is confirmed that the message is ignored.
Test setup	Protocol Tester.
Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	5.8.1.4#2, 5.8.1.4#3, 6.4.4.3.1#4, 6.4.4.3.2#4, 6.4.4.3.3#2, 6.4.4.3.4#4, 6.4.4.4#1, 6.5.11.1#6, 6.5.11.1#7, plus assertions in any appropriate secondary checks.
Parameters Tested	
Checklist References	

Test Procedure for Provider or Provider/Consumer

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode (PROC-PD-MODE).
4. The Tester makes a Request for a voltage above 5V (PROT-PROC-REQ-TSTR).
5. The Tester sends a BIST request for Mode 2.
6. Check that the UUT does not start sending BIST Mode 2 data. [BMC_PROT_BIST_NOT_5V_SRC_1]

14.3.4.11 TDA 2.2.8 BMC-PROT-REV-NUM Revision Number Test

Status	Primary Test
Purpose	To confirm that on receipt of a message header with a higher revision number than that supported, a port responds using the highest revision number it supports.
Critical for Safety	No
Applies to	DRP, Provider, Consumer, Provider / Consumer, Consumer/Provider
Description	A message containing a revision number higher than the current revision is sent to the UUT. The UUT is checked to see that it responds correctly by returning the correct current revision number in a Request message.
Test setup	Protocol Tester.
Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	6.3.4#2, 6.3.4#7, 8.2.6.2#2 plus assertions in any appropriate secondary checks
Parameters Tested	
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode (PROC-PD-MODE). During this procedure, the Tester sends the Source Capabilities message to the UUT using the value 10b for its Specification Revision field.
4. Check that the UUT responds with a Request, and that this contains the Specification Revision value 01b [BMC_PROT_REV_NUM_1].
   Test is now repeated, using reserved value 11b for the Source Capability message Specification Revision field.

14.3.4.12 TDA.2.2.9: BMC-PROT-GSC-REC Get_Source_Cap Received Test

Status	Primary Test
Purpose	To confirm that on receipt of a Get_Source_Cap message in the PE_SRC_Ready state, the port properly transitions to the PE_SRC_Send_Capabilities state.
Critical for Safety	No
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider
Description	A Get_Source_Cap message is send to a UUT that is in the PE_SRC_Ready state. After sending a Source_Capabilities message, the UUT should then expect a Request message in response. When one is not received, the UUT should timeout to PE_SRC_Hard_Reset.
Test setup	Protocol Tester.
Ping Policy	Send Pings where possible
Preconditions	
Assertions Tested	
Parameters Tested	
Checklist References	

Test Procedure

For UUTs that can be started as Source

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered, except as explicitly described. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode as a Source (PROC-PD-MODE).
4. The Tester sends a Get_Source_Cap message to the UUT.
5. Check that a Source_Capabilities message is received from the UUT. [BMC_PROT_GSC_REC_1]
6. The Tester does not send a Request message.
7. Check that after tSenderResponse timeout (30 ms), the UUT issues a Hard Reset. [BMC_PROT_GSC_REC_2]

For UUTs that are Consumer/Providers

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered, except as explicitly described. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. The Tester gets the UUT into PD Mode as a Sink (PROC-PD-MODE).
4. Request a PR_Swap to make the UUT a Source (offering the most favourable conditions to allow a PR_Swap to take place). Wait till there is an explicit contract in place.
5. The Tester sends a Get_Source_Cap message to the UUT.
6. Check that a Source_Capabilities message is received from the UUT. [BMC_PROT_GSC_REC_1]
7. The Tester does not send a Request message.
8. Check that after tSenderResponse timeout (30 ms), the UUT issues a Hard Reset. [BMC_PROT_GSC_REC_2]

14.3.5 Power Source/Sink

14.3.5.1 TDA 2.3.1.1 BMC-POW-SRC-LOAD-P-PC Source Dynamic Load (P or P/C)

Status	Primary Test
Purpose	To verify that the static and dynamic electrical capabilities of a Source UUT meet the requirements for each PDO offered, and that the procedure for requesting a change in current functions correctly. Also verifies the behavior when a Hard Reset is sent to the UUT.
Critical for Safety	
Applies to	DRP, Provider or Provider/Consumer
Description	The Tester requests power under the terms of each available PDO, and checks the static voltage provided at five equally spaced current loads, and that the voltage remains in specification while the current is increased or decreased at a rate of 100mA per µs, from one specified level to another.
Test setup	Dynamic voltage measurement equipment, protocol Tester, adjustable load.
Ping Policy	n/a

Preconditions	The UUT vendor is assumed to have provided a list of source PDOs, to be the list offered by the UUT.
Assertions Tested	6.4.1#4, 7.1.3#2, 7.1.3#3, 7.1.3#4, plus assertions in any appropriate secondary checks.
Parameters Tested	tPSTransition, tSinkRequest, tSourceActivity
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. During the following, if Ping messages are received from the UUT, check that Ping messages timing meets requirements in PROT-PROC-PING.
4. The Tester gets the UUT into PD Mode (PROC-PD-MODE), initially requesting PDO#1 at 100mA.
5. Wait until a Source Capabilities message is received, note the number of Power Data Objects, and record their contents. Check that they are identical to the list provided by the vendor [BMC_POW_SRC_LOAD_P_PC_1]. If at any time during the following steps a further Capabilities message is received, the PDOs shall be compared to the previous ones. If they differ, report the details, and the test ends as a failure.

Repeat the following steps for each of these Power Data Objects, starting with PDO#1:

6. Repeat the next 4 steps at no load, 25% full load, 50% full load, 75% full load, 100% full load, 75% full load, 50% full load, 25% full load and no load (9 separate Requests per PDO).
7. Monitor the voltage during the next step from just before the Request until a time sufficiently later to capture any significant perturbation in the voltage caused by the applied current change.
8. Send a Request for power under the conditions of the current Power Data Object requesting the appropriate current (or power) (use checks in PROT-PROC-REQ-TSTR).
9. Set the Tester to draw the requested current, changing the current drawn at a rate of 100mA per µs.
10. Check that the extremes of the voltage measured remain within the required limits of vSrcNew (for fixed supplies) or within the limits specified for the battery or variable supply, and confirm that the timing of the VBUS waveform versus the messages meets the

11. Start to monitor the voltage on VBUS; send a Hard Reset and confirm that the timing of the VBUS waveform versus the messages meets the requirements for Hard Reset defined in PROT-PROC-HR-TSTR. [BMC_POW_SRC_LOAD_P_PC_3]
12. Emulate a tester-end detach.
13. The Tester follows the procedure to get the UUT into PD Mode (PROC-PD-MODE), however it makes its first request for the highest voltage advertised, but requests 10ma (or 250mW if it is a battery supply)) more than was offered.
14. Check that the UUT Rejects the Request, [BMC_POW_SRC_LOAD_P_PC_4]

14.3.5.2 TDA 2.3.1.2 BMC-POW-SRC-LOAD-CP-ACC Source Dynamic Load CP Accepting Swap

Status	Primary Test
Purpose	To verify that the static and dynamic electrical capabilities of a Source meet the requirements for each PDO offered, and that the procedure for requesting an increase in current functions correctly.
Critical for Safety	
Applies to	DRP or Consumer/Provider which is able to accept a Swap
Description	The Tester requests power under the terms of each available PDO, initially 25% of the offered power, and then requesting an increase to 100%. It then checks the static voltage provided at five equally spaced current loads, and that the voltage remains in specification while the current is increased or decreased at a rate of 100mA per µs, from one specified level to another.
Test setup	Dynamic voltage measurement equipment, protocol Tester, adjustable load.
Ping Policy	Send Pings where possible
Preconditions	The UUT vendor is assumed to have provided a list of source PDOs, to be the list offered by the UUT; and to have stated that the UUT will accept a Power Role Swap request under the test conditions.
Assertions Tested	6.4.1#4, 7.1.3#2, 7.1.3#3, 7.1.3#4, plus assertions in any appropriate secondary checks.
Parameters Tested	tPSTransition, tSinkRequest, tSourceActivity
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections

of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.

2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.

3. During the following, whenever the UUT is acting as a Source, if Ping messages are received from the UUT, check that Ping messages timing meets requirements in PROT-PROC-PING.

4. The Tester gets the UUT into PD Mode (PROC-PD-MODE).

5. Get the UUT Source Capabilities.

6. Set the Tester Sink Capabilities to match this, and set 'Not Externally Powered'.

Change Tester from being a Source to being a Sink as follows:

7. The Tester requests a power role swap (PROT-PROC-SWAP-TSTR), which may initially be declined with a Wait, while the UUT establishes what the Tester sink requirements are. After having been asked for and then having sent the Sink Capabilities, the Tester once again requests a role swap (PROT-PROC-SWAP-TSTR). As the vendor has stated that the PR_Swap will be accepted, and the correct condition is met, a failure to role swap at this point is deemed a test failure. [BMC_POW_SRC_LOAD_CP_ACC_1]

8. On receiving Source Capabilities from the UUT, after the Swap, the Tester initially requests PDO#1 at 100mA.

9. In this Source Capabilities message, note the number of Power Data Objects, and record their contents. Check that they are identical to the list provided by the vendor [BMC_POW_SRC_LOAD_CP_ACC_2]. If at any time during the following steps a further Capabilities message is received, the PDOs shall be compared to the previous ones. If they differ, report the details, and the test ends as a failure.

Repeat the following steps for each of these Power Data Objects, starting with PDO#1:

10. Repeat the next 4 steps at no load, 25% full load, 50% full load, 75% full load, 100% full load, 75% full load, 50% full load, 25% full load and no load (9 separate Requests per PDO).

11. Monitor the voltage during the next step from just before the Request until a time sufficiently later to capture any significant perturbation in the voltage caused by the applied current change.

12. Send a Request for power under the conditions of the current Power Data Object requesting the appropriate current (or power) (use checks in PROT-PROC-REQ-TSTR).

13. Set the Tester to draw the requested current, changing the current drawn at a rate of 100mA per µs.

14. Check that the extremes of the voltage measured remain within the required limits of vSrcNew (for fixed supplies) or within the limits specified for the battery or variable supply, and confirm that the timing of the VBUS waveform versus the messages meets the requirements defined in PROT-PROC-REQ-TSTR. [BMC_POW_SRC_LOAD_CP_ACC_3]

After doing this for each of these Power Data Objects:

15. Start to monitor the voltage on VBUS; send a Hard Reset and confirm that the timing of the VBUS waveform versus the messages meets the requirements for Hard Reset defined in PROT-PROC-HR-TSTR. [BMC_POW_SRC_LOAD_P_PC_4]

14.3.5.3 TDA 2.3.2.1 BMC-POW-SRC-TRANS-P-PC Source PDO Transition Test (P or P/C)

Status	Primary Test
Purpose	To verify the timing, electrical and protocol compliance of a positive or negative voltage or current transition from a Source.
Critical for Safety	
Applies to	DRP, Provider or Provider/Consumer
Description	The Tester causes the UUT to perform each possible transition between sourcing different voltages, and by monitoring Vbus and the protocol messages, verifies that the appropriate conditions are met.
Test setup	Voltage measurement equipment, protocol Tester, adjustable load.
Preconditions	The UUT vendor is assumed to have provided a list of source PDOs, to be the list offered by the UUT.
Ping Policy	n/a
Assertions Tested	5.2.1#1, 5.2.3#1, 7.1.4#1-8, 7.1.5#1-8, 7.1.7#1, plus assertions in any appropriate secondary checks.
Parameters Tested	tSinkRequest
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.

2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. During the following, if Ping messages are received from the UUT, check that Ping messages timing meets requirements in PROT-PROC-PING.
4. The Tester gets the UUT into PD Mode (PROC-PD-MODE), initially requesting PDO#1 at 100mA.
5. Wait until a Source Capabilities message is received, note the number of Power Data Objects, and record their contents. Check that they are identical to the list provided by the vendor [BMC_POW_SRC_TRANS_P_PC_1]. If at any time during the following steps a further Capabilities message is received, the PDOs shall be compared to the previous ones. If they differ, report the details, and the test ends as a failure.

Choose a sequence of Requests which, starting from PDO #1 will, by their completion, have demonstrated every transition between two different available PDOs, and end back at PDO #1. For each of these transitions, and starting with the Tester applying a nominal capacitance of cSnkBulk min (1uF) across Vbus:

6. Send a Request for power under the conditions of the next PDO in question, with a current of 100mA (or a power of 500mW if Battery) or less if less is offered (use the checks in PROT-PROC-REQ-TSTR). Start monitoring Vbus continuously.
7. Check that the Vbus trace measured and the message timing satisfy the requirements in PROT-PROC-REQ-TSTR. [POW_SRC_TRANS_P_PC_2]
8. If not all PDO voltage transitions have been tested, repeat from step 5.
9. Repeat all transition tests from step 5 while the Tester loads Vbus with a nominal cSnkBulk max (10µF).

14.3.5.4 TDA 2.3.2.2 BMC-POW-SRC-TRANS-CP-ACC Source PDO C/P Accepting Swap

Status	Primary Test
Purpose	To verify the timing, electrical and protocol compliance of a positive or negative voltage or current transition from a Source.
Critical for Safety	No
Applies to	DRP or Consumer/Provider, able to accept a Swap request
Description	The Tester causes the UUT to perform each possible transition between sourcing different voltages for available sets of Source Capabilities, and by monitoring Vbus and the protocol messages, verifies that the appropriate conditions are met.
Test setup	Voltage measurement equipment, protocol Tester, adjustable load.
Ping Policy	Send Pings where possible

Preconditions	The UUT vendor is assumed to have provided a list of source PDOs, to be the list offered by the UUT; and to have stated that the UUT will accept a Power Role Swap request under the test conditions.
Assertions Tested	5.2.1#1, 5.2.3#1, 7.1.4#1, 7.1.4#2, 7.1.4#3, 7.1.4#4, 7.1.4#5, 7.1.4#6, 7.1.4#7, 7.1.4#8, 7.1.5#1, 7.1.5#2, 7.1.5#3, 7.1.5#4, 7.1.5#5, 7.1.5#6, 7.1.5#7, 7.1.5#8, 7.1.7#1, 7.1.12#1, 7.1.12#2, 7.1.12#1, 7.1.12#2, plus assertions in any appropriate secondary checks.
Parameters Tested	tSinkRequest
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. During the following, whenever the UUT is acting as a Source, if Ping messages are received from the UUT, check that Ping messages timing meets requirements in PROT-PROC-PING.
4. The Tester gets the UUT into PD Mode (PROC-PD-MODE).
5. Get the UUT Source Capabilities.
6. Set the Tester Sink Capabilities to match this, and set 'Not Externally Powered'.
7. Change Tester from being a Source to being a Sink as follows:
    a. The Tester requests a power role swap (PROT-PROC-SWAP-TSTR), which may initially be declined with a Wait, while the UUT establishes what the Tester sink requirements are. After having been asked for and then having sent the Sink Capabilities, the Tester once again requests a role swap (PROT-PROC-SWAP-TSTR). As the vendor has stated that the PR_Swap will be accepted, and the correct condition are met, a failure to role swap at this point is deemed a test failure. [BMC_POW_SRC_TRANS_CP_ACC_1]
8. On receiving Source Capabilities from the UUT, after the Swap, the Tester initially requests PDO#1 at 100mA.
9. In this Source Capabilities message, note the number of Power Data Objects, and record their contents. Check that they are identical to the list provided by the vendor [BMC_POW_SRC_ TRANS _CP_ACC_2]. If at any time during the following steps a further Capabilities message is received, the PDOs shall be compared to the previous ones. If they differ, report the details, and the test ends as a failure.

Choose a sequence of Requests which, starting from PDO #1 will, by their completion, have demonstrated every transition between two different available PDOs, and end back at PDO #1. For each of these transitions, and starting with the Tester applying a nominal capacitance of cSnkBulk min (1uF) across Vbus:

10. Send a Request for power under the conditions of the next PDO in question, requesting the largest current offered (use checks in PROT-PROC-REQ-TSTR). Start monitoring Vbus continuously.
11. Check that the Vbus trace measured and the message timing satisfy the requirements in PROT-PROC-REQ-TSTR. [BMC_POW_SRC_ TRANS _CP_ACC_3]
12. If not all PDO voltage transitions have been tested, repeat from step 9.
13. Repeat all transition tests from step #8 while the Tester loads Vbus with a nominal cSnkBulk max (10µF).

14.3.5.5 TDA 2.3.3.1 BMC-POW-SNK-TRANS-C-CP Sink PDO Transition Test (C or C/P)

Status	Primary Test
Purpose	To verify the timing, electrical and protocol compliance of a voltage or current transition for a Sink, and that the Sink does not draw more current than contracted for.
Critical for Safety	No
Applies to	Consumer or Consumer/Provider
Description	The Tester causes the UUT to make a request for power under the terms of a new PDO, selected at the discretion of the test operator. It then checks that the UUT meets the protocol and protocol timing requirements and does not draw more current than permitted at any time during or after the transition. Finally the Sink is suspended and its current draw checked against permitted suspend current.
Test setup	Current measurement equipment, protocol Tester, adjustable supply.
Ping Policy	Send Pings where possible

Preconditions	The Tester attempts to encourage the UUT to make a request for a transition from 5V to the highest voltage it can make use of. If no better alternative is available, a transition from 5V/100mA to 5V at a higher current may be used as the test example. Except for this case we will be testing a voltage and a current increase type transition.
Assertions Tested	5.2.1#1, 5.2.3#1, 7.2.3#1-5, 7.3.1#1-5, 7.3.2#1-6, 7.3.3#1-6, 7.3.4#1-6, 7.3.5#1-6, 7.3.6#1-6, 7.3.7#1-6, 7.3.8#1-6, 7.3.19#1-3, plus assertions in any appropriate secondary checks.
Parameters Tested	tSourceActivity, tNewSnk
Checklist References	

Test Procedure

1. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
2. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
3. During the following, Ping messages are sent by the Tester, as specified in PROT-PROC-PING. (Although optional, it is desirable to check that Ping does not cause any misbehavior.)
4. The Tester gets the UUT into PD Mode (PROC-PD-MODE), initially offering only PDO#1 at 100mA.
5. After a contract has been established, fetch the UUT Sink Capabilities.
6. The Tester sends a Get_Sink_Cap message to the UUT (use checks in PROT-PROC-GETSNKCAPS-TSTR).
7. Check this Sink Capabilities message to ensure that it matches the PDOs specified by the vendor. [POW_SNK_TRANS_C_CP_1] Note the PDO# with the highest voltage for subsequent tests.
8. The Tester changes its capabilities to offer 0mA for PDO#1, and the full requested current (power) at PDO#2 corresponding to the sink PDO# noted above, and sends out a new Source Capabilities message as a result (use checks in PROT-PROC-SRCCAPS-TSTR). (If only 5V is specified in the Sink Capabilities, offer only PDO#1 at the full current required.)
9. Check that we receive a request from the UUT for PDO#2 (or PDO#1 if 5V only), starting to monitor Vbus voltage and current at this point. Check that the transition timing is correct according to Section 7.4.1.
10. Change the Tester Source Capabilities to 0mA at each of the offered PDOs.

11. Check that we receive a valid request for 0mA from the UUT, and Accept that Request. [POW_SNK_TRANS_C_CP_2]
12. Check that the current draw after the transition corresponds to a power draw of 25mW. [POW_SNK_TRANS_C_CP_3]
13. The Tester simulates a cable detach.

14.3.5.6 TDA 2.3.3.2 BMC-POW-SNK-TRANS-PC Sink PDO Transition Test (P/C)

Status	Primary Test
Purpose	To verify the timing, electrical and protocol compliance of a voltage or current transition for a Sink, after a Role Swap, and that the Sink does not draw more current than contracted for.
Critical for Safety	No
Applies to	DRP, Provider/Consumer
Description	The Tester performs a Power Role Swap to make the UUT into a Sink. It then attempts to encourage the UUT to make a request for a transition from 5V to the highest voltage it can make use of. If no better alternative is available, a transition from 5V/100mA to 5V at a higher current may be used as the test example. Except for this case we will be testing a voltage and a current increase type transition. Finally the Sink is suspended and its current draw checked against permitted suspend current.
Test setup	Current measurement equipment, protocol Tester, adjustable supply.
Ping Policy	Send Pings where possible

Preconditions	The UUT vendor is assumed to have provided instructions, and any special equipment required, to force the UUT to accept a role swap, and then request and use a particular Sink PDO, preferably a voltage higher than vSafe5V. If no better alternative is available, a transition from 5V/100mA to 5Vat a higher may be used as the test example. Except for this case we will be testing a voltage and a current increase type transition. For each PDO the vendor is assumed to have specified how long the Tester should wait before the maximum expected load will be drawn. This period has a default minimum of 5 seconds.
Assertions Tested	5.2.1#1, 5.2.3#1, 7.2.3#1-5, 7.3.1#1-5, 7.3.2#1-6, 7.3.3#1-6, 7.3.4#1-6, 7.3.5#1-6, 7.3.6#1-6, 7.3.7#1-6, 7.3.8#1-6, 7.3.19#1-3, plus assertions in any appropriate secondary checks.
Parameters Tested	tSourceActivity, tNewSnk
Checklist References	

Note: A Provider/Consumer is guaranteed to accept a swap request, under defined conditions.

Test Procedure

The following procedure make use of a configuration which will guarantee a Swap will be accepted. Essentially this means that the Provider/Consumer UUT will not be externally powered, and that the Tester will be pre-programmed with the Source Capabilities matching the vendor specified Sink Capabilities are considered to satisfy its condition to accept a Role Swap.

Note: As this is a sink and also as it is role swapped we limit the test to one or two transitions, depending on the circumstances.

1. Follow the appropriate instructions supplied by the vendor to guarantee that the Role Swap will occur.
2. During the following, the Tester is assumed to be running a PD Communications engine, which interacts correctly with all communications encountered. All messages are assumed to be checked in detail against the appropriate sections of this Plan, and the timing between messages and significant power supply events is also checked against the appropriate sections of this Plan. Specific Compliance Plan sections which will be checked in this test are shown above in 'Assertions Tested'.
3. The connection to the UUT is via a short 5A cable with a cable e-marker, or the e-marker may be absent, and the tester may simulate the 5A cable responses. If the UUT has a captive cable then it shall be connected directly to the tester, and the tester shall not simulate a cable marker.
4. The Tester gets the UUT into PD Mode (PROC-PD-MODE). By default, its Source Capabilities will only offer PDO#1 at 100mA, and its Sink Capabilities will only require PDO#1 at 100mA. [BMC_POW_SNK_TRANS_PC_1]

5. Change the Source Capabilities offered to a list which matches the vendor Sink Capabilities.
6. Change Tester from being a Sink to being a Source as follows:
    a. The Tester requests a role swap (use checks in PROT-PROC-SWAP-TSTR-SNK), which may initially be declined with a Wait, while the UUT establishes what the Tester Source Capabilities are. After having been asked for and then having sent the Source Capabilities, the Tester once again requests a role swap (use checks in PROT-PROC-SWAP-TSTR-SNK). As the Tester is meeting the vendor description which guarantees a swap will be accepted, a failure to role swap at this point is deemed a test failure. [BMC_POW_SNK_TRANS_PC_2]
7. The Tester sends the Source Capabilities specified by the vendor (use checks in PROT-PROC-SRCCAPS-TSTR) (not to offer these capabilities would result in the possibility of the UUT requesting a further role swap.)
8. The Sink is obliged to make a request at this point (use checks in PROT-PROC-REQ-UUT). This may be for the target PDO or for an intermediate one. Perform the Transition Checks specified below in PROT-PROC-REQ-UUT.
9. Send a Get_Sink_Cap message (use checks in PROT-PROC-REQ-UUT).
10. Check this Sink Capabilities message to ensure that it matches the PDOs specified by the vendor. [BMC_POW_SNK_TRANS_PC_3] Note the PDO# with the highest voltage for subsequent tests.
11. The Tester changes its capabilities to offer 0mA for PDO#1, and the full requested current (power) at PDO#2 corresponding to the sink PDO# noted above, and sends out a new Source Capabilities message as a result (use checks in PROT-PROC-SRCCAPS-TSTR). (If only 5V is specified in the Sink Capabilities, offer only PDO#1 at the full current required.)
12. Check that we receive a request from the UUT for PDO#2 (or PDO#1 if 5V only), starting to monitor Vbus voltage and current at this point. [BMC_POW_SNK_TRANS_PC_4] Check that the transition timing is correct according to Section 7.4.1.
13. The Tester changes its capabilities to offer 0mA at each of the previously offered voltages, and sends out a new Source Capabilities message as a result (use checks in PROT-PROC-SRCCAPS-TSTR).
14. Check that we receive a valid request for 0mA from the UUT (use checks in PROT-PROC-REQ-UUT), and Accept that Request. [BMC_POW_SNK_TRANS_PC_5]
15. Check that the current draw after the transition corresponds to a power draw of 25mW. [BMC_POW_SNK_TRANS_PC_6]
16. The Tester simulates a cable detach.

14.4 All Devices - Secondary Checks

14.4.1 Message Checks

The following are checks to be performed on messages, **whenever** they are encountered during a Primary Test.

14.4.1.1 TDB 1.1.1 PHY-MSG-GEN PHY Level General Message Test

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To validate the PHY level behavior of message format.
Critical for Safety	
Applies to	Any UUT
Description	This section is a list of specific checks to be made in the course of any other test when a message from the UUT is seen.
Test setup	Depends on test being carried out.
Preconditions	
Assertions Tested	5.6.1.1#3, 5.6.1.1#4
Parameters Tested	
Checklist References	

Test Procedure

1. Check that Preamble is a 64-bit sequence of alternating '0's and '1's. (In practice the last 60 bits are checked as there is some uncertainty about detecting the initial bits.) [PHY_MSG_GEN_1]
2. Check that Preamble ends with '1'. [PHY_MSG_GEN_2]

14.4.1.2 TDB 2.1.2.1 PROT-MSG-HDR Message Header Checks – Except GoodCRC

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any Message Header sent by the UUT (except GoodCRC).
Critical for Safety	
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider, Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1#1, 6.2.1.1#1, 6.2.1.1#2, 6.2.1.2#1, 6.2.1.3#1, 6.2.1.3#2, 6.2.1.4#1, 6.2.1.4#2, 6.2.1.4#3, 6.2.1.4#4, 6.2.1.4#5, 6.2.1.4#7, 6.2.1.5#1, 6.2.1.6#1, 6.2.1.6#2, 6.2.1.8#1, 6.3#1, 6.3#2
Parameters Tested	nMessageIDCount
Checklist References	

Test Procedure - Message Header Checks

During any test which refers to this section, ensure that the following checks are carried out:

1. That bit 15 (reserved) of the Message Header is set to 0. [PROT_MSG_HDR_1]
2. That the size in bytes of the message following the Message Header is 4 times the Number of Data Objects represented by the value in bits 14:12. [PROT_MSG_HDR_2]
3. That the MessageID represented by the value in bits 11:9 of the Message Header is the expected value, i.e.:
    - if this is first message after a Hard Reset was sent or received by the sender of this message, or after attachment, or after a Swap, or (in the case of a cable plug or DFP or UFP talking to a Cable Plug) after a Cable Reset, the value shall be 000b. [PROT_MSG_HDR_3]
    - if the message is a Soft Reset, the value shall be 000b. [PROT_MSG_HDR_4]
    - if the message is the first message after a Soft Reset was received by the sender of the message, the value shall be 000b. [PROT_MSG_HDR_5]
    - that it is incremented by one compared with the previously received message (modulo-[nMessageIDCount+1]), with the following exceptions:
        - during 'Discovery', when the Source Capabilities message shall have the MessageID value 000b until after a GoodCRC is received, and
        - if the message is an exact repeat of the previous message then it is valid for the MessageID to be the same as for that previous message, on the assumption that

the re-sender of this message did not see a GoodCRC.
[PROT_MSG_HDR_6]

- if the message is Returned BIST Counters, then No check is performed on MessageID.

4. That the Port Power Role represented by the value in bit 8 of the Message Header for an SOP Packet Type is the expected value, based on the tester's knowledge of the UUT port role. Additionally, confirm that for a Ping or GotoMin, the Port Power Role is Source (bit 8 = '1'), and for a Request, the Port Power Role is Sink (bit 8 = '0'). The Port Power Role bit in the first PS_RDY during a Swap shall to set to Sink.
[PROT_MSG_HDR_11]
5. That the Cable Plug role represented by the value in bit 8 of the Message Header for any packet type other than an SOP Type is the expected value, based on the tester's knowledge of the UUT. [PROT_MSG_HDR_12]
6. That the Specification Revision represented by the value in bits 7:6 of the Message Header is 01b. [PROT_MSG_HDR_13]
That if BMC is in use, the Specification Revision represented by the value in bits 7:6 of the Message Header is not 00b. [PROT_MSG_HDR_18]
7. That the Port Data Role represented by the value in bit 5 of the Message Header for an SOP Packet Type is the expected value, based on the tester's knowledge of the UUT port role.
[PROT_MSG_HDR_14]
8. That the reserved field represented by the value in bit 5 of the Message Header for any packet type other than an SOP is zero. [PROT_MSG_HDR_15]
9. That the reserved field represented by the value in bit 4 of the Message is zero.
[PROT_MSG_HDR_16]
10. That the MessageType represented by the value in bits 3:0 of the Message Header is not a reserved value. [PROT_MSG_HDR_17]
    a. Reserved values for Control Messages (defined by Number of Data Objects = 0) for an SOP packet type are 0000b, 1110b and 1111b.
    Additional reserved values for BMC are 1001b and 1011b.
    b. Reserved values for Control Messages (defined by Number of Data Objects = 0) for any packet type other than an SOP Type are 0000b, 0010b, 0100b, 0110b, 0111b, 1000b, 1001b, 1010b, 1011b, 1100b, 1110b and 1111b.
    c. Reserved values for Data Messages (defined by Number of Data Objects > 0) for an SOP packet type are 0000b and 0101 to 1110b.
    d. Reserved values for Data Messages (defined by Number of Data Objects > 0) for any packet type other than an SOP Type are 0000b to 0010b, and 0100 to 1110b.

TABLE 4. VALID CONTROL MESSAGETYPES (V1.3)

MessageType	Message Name
0000b	(reserved)
0001b	GoodCRC
0010b	GotoMin
0011b	Accept
0100b	Reject
0101b	Ping
0110b	PS_RDY
0111b	Get_Source_Cap
1000b	Get_Sink_Cap
1001b	Protocol Error (deprecated)
1010b	Swap
1011b	(reserved)
1100b	Wait
1101b	Soft Reset
1110b-1111b	(reserved)

TABLE 5. VALID DATA MESSAGETYPES (V1.3)

MessageType	Number of Data Objects	Message Name
0000b	-	(reserved)
0001b	1 to 7	Source Capabilities
0010b	1	Request
0011b	1	BIST
0100b	1 to 7	Sink Capabilities
0101b-1110b	-	(reserved)
1111b	1 to 7	Vendor Defined

TABLE 6. VALID CONTROL MESSAGETYPES (SOP - V2.0)

MessageType	Message Name
0000b	(reserved)
0001b	GoodCRC
0010b	GotoMin
0011b	Accept
0100b	Reject
0101b	Ping
0110b	PS_RDY
0111b	Get_Source_Cap
1000b	Get_Sink_Cap
1001b	DR_Swap
1010b	Swap
1011b	Vconn_Swap
1100b	Wait
1101b	Soft Reset
1110b-1111b	(reserved)

TABLE 7. VALID CONTROL MESSAGETYPES (NOT SOP V2.0)

MessageType	Message Name
0000b	(reserved)
0001b	GoodCRC
0010b	(reserved)
0011b	Accept
0100b-1100b	(reserved)
1101b	Soft Reset
1110b-1111b	(reserved)

TABLE 8. VALID DATA MESSAGETYPES (SOP - V2.0)

MessageType	Number of Data Objects	Message Name
0000b	-	(reserved)
0001b	1 to 7	Source Capabilities
0010b	1	Request
0011b	1	BIST
0100b	1 to 7	Sink Capabilities
0101b-1110b	-	(reserved)
1111b	1 to 7	Vendor Defined

TABLE 9. VALID DATA MESSAGETYPES (NOT SOP - V2.0)

MessageType	Number of Data Objects	Message Name
0000b-0010b	-	(reserved)
0011b	1	BIST
0100b-1110b	-	(reserved)
1111b	1 to 7	Vendor Defined

14.4.1.3 TDB 2.1.2.2 PROT-MSG-HDR-GCRC Message Header Check – Good CRC

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the GoodCRC message is received by the Tester.
Critical for Safety	
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider, Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section. The correct formatting of the GoodCRC message is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.1#2, 6.2.1.2#1, 6.2.1.3#1, 6.2.1.4#1, 6.2.1.4#7, 6.2.1.5#1, 6.2.1.6#1, 6.2.1.6#3, 6.2.1.7#1, 6.2.1.7#2, 6.3.1#1, 6.3.1#2, 6.3.1#3
Parameters Tested	
Checklist References	

Test Procedure - GoodCRC Checks

This set of checks assumes that the message in which the header appears has already been identified as GoodCRC, because it has the correct value of 000b for the Number of Data Objects in bits 14:12, and the correct MessageType of 0001b in bits 3:0.

During any test which refers to this section, ensure that the following checks are carried out:

1. That bit 15 (reserved) of the Message Header is set to 0. [PROT_MSG_HDR_GCRC_1]
2. That the size in bytes of the message following the Message Header is zero. [PROT_MSG_HDR_GCRC_2]
3. That the MessageID represented by the value in bits 11:9 of the Message Header is the expected value, i.e., the same as the value in the preceding message from the tester. [PROT_MSG_HDR_GCRC_3]
4. That the Port Power Role represented by the value in bit 8 of the Message Header for an SOP Packet Type is the expected value, based on the tester's knowledge of the UUT port role. There is an ambiguous case in the GoodCRC responding to the first PS_RDY during a Swap. The PS_RDY is sent by the new Sink, but the GoodCRC will, in most implementations, be from the old Sink. In practice we will **not** check this during Compliance. [PROT_MSG_HDR_GCRC_7]

5. That the Cable Plug role represented by the value in bit 8 of the Message Header for any packet type other than an SOP Type is the expected value, based on the tester's knowledge of the UUT. [PROT_MSG_HDR_GCRC_8]
6. That the Specification Revision represented by the value in bits 7:6 of the Message Header is 01b. [PROT_MSG_HDR_GCRC_9]
7. That if BMC is in use, the Specification Revision represented by the value in bits 7:6 of the Message Header is not 00b. [PROT_MSG_HDR_GCRC_14]
8. That the Port Data Role represented by the value in bit 5 of the Message Header for an SOP Packet Type is the expected value, based on the tester's knowledge of the UUT port role. [PROT_MSG_HDR_GCRC_10]
9. That the reserved field represented by the value in bit 5 of the Message Header for any packet type other than an SOP is zero. [PROT_MSG_HDR_GCRC_11]
10. That the reserved field represented by the value in bit 4 of the Message is zero. [PROT_MSG_HDR_GCRC_12]
11. That the first bit of the GoodCRC is returned within tTransmit max (195µs) of the last bit of the previous message. [PROT_MSG_HDR_GCRC_13]

14.4.1.4 TDB 2.1.3 PROT-MSG-CTRL Control Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which one of the following Control messages is sent by the UUT: GoodCRC, GoToMin, Accept, Reject, Ping, PS_RDY, Get_Source_Cap, Get_Sink_Cap, Protocol Error, DR_Swap, PR_Swap, Vconn_Swap, Wait, Soft Reset
Critical for Safety	
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider, Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section. The correct formatting of the GoodCRC message is checked.
Test setup	Depends on test referring to this section.

Preconditions	
Assertions Tested	6.2.1.2#1, 6.5.1#6, 6.5.1#7, 6.5.2#6, 6.6.1.1#1, 6.6.1.1#2, 6.6.1.1#3, 6.6.1.2#1, 6.6.1.2#2, 6.6.1.2#3, plus assertions in checks: PROT-HDR PROT-HDR-GCRC
Parameters Tested	
Checklist References	

Test Procedure

This set of checks assumes that the message has already been identified as the one being tested, because it has the correct value of 000b for the Number of Data Objects in bits 14:12, and the correct MessageType in bits 3:0.

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR or PROT-HDR-GCRC.
2. That the number of bytes of the payload, following the header, is zero. [PROT_MSG_CTRL_1]

14.4.1.5 TDB 2.1.3.1 PROT-MDG-CTRL-PING Ping Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Ping message is sent by the UUT.
Critical for Safety	
Applies to	DRP, Provider, Provider/Consumer or Consumer/Provider
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section. The correct formatting of the Ping message is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.5.1#1, 6.5.3.1#2, 6.5.3.1#3, plus assertions in checks: PROT-MSG-CTRL
Parameters Tested	
Checklist References	

Test Procedure

This set of checks assumes that the message has already been identified as the one being tested, because it has the correct value of 000b for the Number of Data Objects in bits 14:12, and the correct Message Type 0101b in bits 3:0.

During any test which refers to this section, ensure that the following checks are carried out:

1. That the Control Message Checks (PROT-MSG-CTRL) are correct.
2. That the partnered devices currently have a contract. [PROT_MSG_CTRL_PING_1]
3. That Pings are sent periodically when a Source is operating at a voltage other than vSafe5V, or if the Source is in a Swapped state. [PROT_MSG_CTRL_PING_2]

14.4.1.6 TDB 2.1.4.1.1 PROT-MSG-DATA-SRC-CAP Source Capability Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the (Source) Capabilities message is sent by the UUT.
Critical for Safety	
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section. The correct formatting of the Source Capabilities message is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.1#1, 6.4.1#3, 6.4.1.2#2, 6.4.1.2.3#1, 6.4.1.2.3#2, 6.4.1.2.3#3, 6.4.1.2.3.1#1, 6.4.1.2.3.1#2, 6.4.1.2.3.2#2, 6.4.1.2.3.3#1, 6.4.1.2.3.4#1, 6.4.1.2.3.5#1, 6.4.1.2.3.5#2, 6.4.1.2.3.6#2, 6.4.1.2.3.6#3, 6.4.1.2.3.6#4, 6.4.1.2.4#1, 6.4.1.2.4#2, 6.4.1.2.5#1, 6.4.1.2.5#2, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.
2. That the Number of Data Objects represented by the value in bits 14:12 is at least 1 [PROT_MSG_DATA_SRC_CAP_1].
3. That the Message Type represented by the value in bits 3:0 of the Message Header is 0001b [PROT_MSG_DATA_SRC_CAP_2].
4. That for the first PDO in a Source Capabilities message, bits B31:B30 are set to 00b (representing a Fixed supply) [PROT_MSG_DATA_SRC_CAP_3].
5. That for the first PDO in a Source Capabilities message, the state of bit B29 matches the vendor supplied information as to whether the UUT is a dual role PD device [PROT_MSG_DATA_SRC_CAP_4].
6. That for the first PDO in a Source Capabilities message, the state of bit B28 matches the vendor supplied information as to whether the UUT supports USB Suspend [PROT_MSG_DATA_SRC_CAP_5].

7. That for the first PDO in a Source Capabilities message, the state of bit B27 matches the current known state of whether the UUT is Externally Powered, in tests where this information is known [PROT_MSG_DATA_SRC_CAP_6].
8. That for the first PDO in a Source Capabilities message, the state of bit B26 matches the vendor supplied information as to whether the UUT is USB Communications capable [PROT_MSG_DATA_SRC_CAP_7].
9. That for the first PDO in a Source Capabilities message, the state of bit B25 matches the vendor supplied information as to whether the UUT is Type-C and performs DR_Swap [PROT_MSG_DATA_SRC_CAP_8].
10. That for the first PDO in a Source Capabilities message, bits B24:B22 are set to 0 [PROT_MSG_DATA_SRC_CAP_9].
11. That for the first PDO in a Source Capabilities message, the value bit B21:B20 contain a value for Peak Power equal to the one declared for this PDO by the vendor [PROT_MSG_DATA_SRC_CAP_10].
12. That for the first PDO in a Source Capabilities message, the voltage represented by bits B19:B10 is 5V [PROT_MSG_DATA_SRC_CAP_11].
13. That for the first PDO in a Source Capabilities message, bits B9:B0 contains a value equal to the one declared for this PDO by the vendor [PROT_MSG_DATA_SRC_CAP_12].
14. That a PDO in a Source Capabilities message has a value in B31:B30 of 00b (referred to as a Fixed PDO), 01b (referred to as a Battery PDO) or 10b (referred to as a Variable PDO), but never 11b [PROT_MSG_DATA_SRC_CAP_13].
15. That any PDOs following the first one, are in the correct order: Fixed PDOs in increasing voltage sequence, Battery PDOs in increasing minimum voltage sequence and finally Variable PDOs in increasing minimum voltage sequence [PROT_MSG_DATA_SRC_CAP_14].
16. That for any Fixed PDO in a Source Capabilities message, other than the first, bits B29:B22 are set to 0 [PROT_MSG_DATA_SRC_CAP_15].
17. That for any Fixed PDO in a Source Capabilities message, bits B21:B20 contain a value for Peak Power equal to the one declared for this PDO by the vendor [PROT_MSG_DATA_SRC_CAP_16].
18. That for any Fixed PDO in a Source Capabilities message, other than the first, the voltage represented by bits B19:B10 equal to that declared by the vendor [PROT_MSG_DATA_SRC_CAP_17].
19. That for any Fixed PDO in a Source Capabilities message, the current represented by bits B9:B0 is equal to that declared by the vendor [PROT_MSG_DATA_SRC_CAP_18].
20. That for any Variable PDO in a Source Capabilities message, the Maximum Voltage represented by bits B29:B20 is equal to that declared by the vendor [PROT_MSG_DATA_SRC_CAP_19].
21. That for any Variable PDO in a Source Capabilities message, the Minimum Voltage represented by bits B19:B10 is equal to that declared by the vendor [PROT_MSG_DATA_SRC_CAP_20].
22. That for any Variable PDO in a Source Capabilities message, the current represented by bits B9:B0 is equal to that declared by the vendor [PROT_MSG_DATA_SRC_CAP_21].

23. That for any Battery PDO in a Source Capabilities message, the Maximum Voltage represented by bits B29:B20 is equal to that declared by the vendor [PROT_MSG_DATA_SRC_CAP_22].
24. That for any Battery PDO in a Source Capabilities message, the Minimum Voltage represented by bits B19:B10 is equal to that declared by the vendor [PROT_MSG_DATA_SRC_CAP_23].
25. That for any Battery PDO in a Source Capabilities message, the current represented by bits B9:B0 is equal to that declared by the vendor [PROT_MSG_DATA_SRC_CAP_24].
26. That no Fixed PDO has the same voltage as any other [PROT_MSG_DATA_SRC_CAP_25].
27. That no Variable PDO has the same voltage range as any other [PROT_MSG_DATA_SRC_CAP_26].
28. That no Battery PDO has the same voltage as any other [PROT_MSG_DATA_SRC_CAP_27].
29. That the Source Capabilities offered are consistent with the PD Power As Source specified by the vendor [PROT_MSG_DATA_SRC_CAP_28]. This means that the Source Capabilities shall meet the Power Rules in the latest specification 2.x version.
30. That the Source Capabilities message differs from the previously sent one, unless it is sent in response to from a Get_Source_Cap message, or during 'Discovery' [PROT_MSG_DATA_SRC_CAP_29].

14.4.1.7 TDB 2.1.4.2.2 PROT-MSG-DATA-SNK-CAP Sink Capability Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the (Sink) Capabilities message is sent by the UUT.
Critical for Safety	
Applies to	DRP, Provider/Consumer, Consumer/Provider or Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section. The correct formatting of the Sink Capabilities message is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.1#1, 6.4.1#3, 6.4.1.2.3#4, 6.4.1.2.3.1#1, 6.4.1.2.3.1#2, 6.4.1.2.3.3#1, 6.4.1.2.3.4#1, 6.4.1.2.3.5#1, 6.4.1.2.3.5#2, 6.4.1.2.4#1, 6.4.1.2.4#2, 6.4.1.2.5#1, 6.4.1.2.5#2, 6.4.1.3#1, 6.4.1.3#2, 6.4.1.3#3, 6.4.1.3#4, 6.4.1.3#6, 6.4.1.3#7, 6.4.1.3.1#1, 6.4.1.3.1#2, 6.4.1.3.1#3, 6.4.1.3.1#4, 6.4.1.3.1.1#1, 6.4.1.3.1.1#2, 6.4.1.3.1.2#1, 6.4.1.3.1.4#1, 6.4.1.3.2#1, 6.4.1.3.2#2, 6.4.1.3.3#1, 6.4.1.3.3#2plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.
2. That the Number of Data Objects represented by the value in bits 14:12 is at least 1 [PROT_MSG_DATA_SNK_CAP_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 0100b [PROT_MSG_DATA_SNK_CAP_2].
4. That for the first PDO in a Sink Capabilities message, bits B31:B30 are set to 00b (representing a Fixed supply) [PROT_MSG_DATA_SNK_CAP_3].
5. That for the first PDO in a Sink Capabilities message, the state of bit B29 matches the vendor supplied information as to whether the UUT is a dual role PD device [PROT_MSG_DATA_SNK_CAP_4].
6. That for the first PDO in a Sink Capabilities message, the state of bit B28 (Higher Capability) matches the vendor supplied information as to whether the UUT needs more than vSafe5V to provide full functionality [PROT_MSG_DATA_SNK_CAP_5].

7. That for the first PDO in a Sink Capabilities message, the state of bit B27 matches the current known state of whether the UUT is Externally Powered, in tests where this information is known [PROT_MSG_DATA_SNK_CAP_6].
8. That for the first PDO in a Sink Capabilities message, the state of bit B26 matches the vendor supplied information as to whether the UUT is USB Communications capable [PROT_MSG_DATA_SNK_CAP_7].
9. That for the first PDO in a Source Capabilities message, the state of bit B25 (Data Role Swap) matches the vendor supplied information as to whether the UUT is Type-C and performs DR_Swap [PROT_MSG_DATA_SNK_CAP_8].
10. That for the first PDO in a Sink Capabilities message, bit B24:B20 (reserved) are set to 0 [PROT_MSG_DATA_SNK_CAP_9].
11. That for the first PDO in a Sink Capabilities message, the voltage represented by bits B19:B10 is 5V [PROT_MSG_DATA_SNK_CAP_10].
12. That for the first PDO in a Sink Capabilities message, bits B9:B0 contains a value no larger than the one declared for this PDO by the vendor [PROT_MSG_DATA_SNK_CAP_11].
13. That a PDO in a Sink Capabilities message has a value in B31:B30 of 00b (referred to as a Fixed PDO), 01b (referred to as a Battery PDO) or 10b (referred to as a Variable PDO), but never 11b [PROT_MSG_DATA_SNK_CAP_12].
14. That any PDOs following the first one, are in the correct order: Fixed PDOs in increasing voltage sequence, Battery PDOs in increasing minimum voltage sequence and finally Variable PDOs in increasing minimum voltage sequence [PROT_MSG_DATA_SNK_CAP_13].
15. That for any Fixed PDO in a Sink Capabilities message, other than the first, bits B29:B20 are set to 0 [PROT_MSG_DATA_SNK_CAP_14].
16. That for any Fixed PDO in a Sink Capabilities message, other than the first, the voltage represented by bits B19:B10 is the value declared by the vendor [PROT_MSG_DATA_SNK_CAP_15].
17. That for any Fixed PDO in a Sink Capabilities message, the current represented by bits B9:B0 does not exceed the value declared by the vendor [PROT_MSG_DATA_SNK_CAP_16].
18. That for any Variable PDO in a Sink Capabilities message, the Maximum Voltage represented by bits B29:B20 is the value declared by the vendor [PROT_MSG_DATA_SNK_CAP_17].
19. That for any Variable PDO in a Sink Capabilities message, the Minimum Voltage represented by bits B19:B10 is the value declared by the vendor [PROT_MSG_DATA_SNK_CAP_18].
20. That for any Variable PDO in a Sink Capabilities message, the current represented by bits B9:B0 does not exceed the value declared by the vendor [PROT_MSG_DATA_SNK_CAP_19].
21. That for any Battery PDO in a Sink Capabilities message, the Maximum Voltage represented by bits B29:B20 is the value declared by the vendor [PROT_MSG_DATA_SNK_CAP_20].
22. That for any Battery PDO in a Sink Capabilities message, the Minimum Voltage represented by bits B19:B10 is the value declared by the vendor [PROT_MSG_DATA_SNK_CAP_21].
23. That for any Battery PDO in a Sink Capabilities message, the current represented by bits B9:B0 does not exceed the value declared by the vendor [PROT_MSG_DATA_SNK_CAP_22].

24. That no Fixed PDO has the same voltage as any other [PROT_MSG_DATA_ SNK _CAP_23].
25. That no Variable PDO has the same voltage range as any other [PROT_MSG_DATA_ SNK _CAP_24].
26. That no Battery PDO has the same voltage as any other [PROT_MSG_DATA_ SNK _CAP_25].
27. That the Sink Capabilities specified are consistent with the PD Power As Sink specified by the vendor [PROT_MSG_DATA_ SNK _CAP_26]. This means that the Sink Capabilities shall meet the Power Rules in the latest specification 2.x version.

14.4.1.8 TDB 2.1.4.2 PROT-MSG-DATA-REQ Request Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Request message is sent by the UUT.
Critical for Safety	
Applies to	DRP, Provider/Consumer, Consumer/Provider or Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section. The correct formatting of the Source Capabilities message is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.2#3, 6.4.2#4, 6.4.2#5, 6.4.2.1#1, 6.4.2.2#1, 6.4.2.3#3, 6.4.2.3#4, 6.4.2.3#5, 6.4.2.4#1, 6.4.2.6#1, 6.4.2.6#3, 6.4.2.7#1, 6.4.2.7#2, 6.4.2.7#3, 6.4.2.8#1, 6.4.2.8#2, 6.4.2.8#3, 6.4.2.9#1, 6.4.2.9#2, 6.4.2.10#1, 6.4.2.10#2, 6.4.2.10#3, 6.4.2.10#4, 6.4.2.11#1, 6.4.2.11#2, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in Section 14.4.1.3.
2. That the Number of Data Objects represented by the value in bits 14:12 is exactly 1 [PROT_MSG_DATA_REQ_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 0010b [PROT_MSG_DATA_REQ_2].
4. That B31 of the Request Data Object (RDO) is set to 0b [PROT_MSG_DATA_REQ_3].

5. That the Object Position represented by B30:28 is not 000b [PROT_MSG_DATA_REQ_4], and is not greater than the number of PDOs offered in the Source Capabilities message most recently received by the UUT [PROT_MSG_DATA_REQ_5].
6. That B25, the USB Communications Capable bit, matches the statement provided by the Vendor as to whether the UUT is USB Communications capable [PROT_MSG_DATA_REQ_6].
7. That B24, the No USB Suspend bit, matches the statement provided by the Vendor as to whether the UUT sets this bit [PROT_MSG_DATA_REQ_7].
8. That B23:20 are set to 0000b [PROT_MSG_DATA_REQ_8].

If the PDO requested is a Fixed or Variable supply and B27 (Giveback flag) is 0:

9. That the Operating Current represented by B19:10 (10mA units) does not exceed the current offered by the referenced PDO [PROT_MSG_DATA_REQ_9].
10. That, if the Maximum Operating Current represented by B9:0 (10mA units) exceeds the current offered by the referenced PDO, then B26 (the Capability Mismatch bit) is also set [PROT_MSG_DATA_REQ_10].
11. That the Operating Current represented by B19:10 (10mA units) does not exceed the Maximum Operating Current represented by B9:0 (10mA units) [PROT_MSG_DATA_REQ_11].

If the PDO requested is a Fixed or Variable supply and B27 (Giveback flag) is 1:

12. That the Operating Current represented by B19:10 (10mA units) does not exceed the current offered by the referenced PDO [PROT_MSG_DATA_REQ_12].
13. That the Minimum Operating Current represented by B9:0 (10mA units) does not exceed the current offered by the referenced PDO [PROT_MSG_DATA_REQ_13].
14. That the Minimum Operating Current represented by B9:0 (10mA units) is less than does not exceed the Operating Current represented by B19:10 (10mA units) [PROT_MSG_DATA_REQ_14].

If the PDO requested is a Battery supply and B27 (Giveback flag) is 0:

15. That the Operating Power represented by B19:10 (250mW units) does not exceed the current offered by the referenced PDO [PROT_MSG_DATA_REQ_15].
16. That, if the Maximum Operating Power represented by B9:0 (250mW units) exceeds the power offered by the referenced PDO, then B26 (the Capability Mismatch bit) is also set [PROT_MSG_DATA_REQ_16].
17. That the Operating Power represented by B19:10 (250mW units) does not exceed the Maximum Operating Power represented by B9:0 (250mW units) [PROT_MSG_DATA_REQ_17].

If the PDO requested is a Battery supply and B27 (Giveback flag) is 1:

18. That the Operating Power represented by B19:10 (250mW units) does not exceed the current offered by the referenced PDO [PROT_MSG_DATA_REQ_18].

19. That the Minimum Operating Power represented by B9:0 (250mW units) does not exceed the power offered by the referenced PDO [PROT_MSG_DATA_REQ_19].
20. That the Minimum Operating Power represented by B9:0 (250mW units) is less than does not exceed the Operating Power represented by B19:10 (250mW units) [PROT_MSG_DATA_REQ_20].

14.4.1.9 TDB 2.1.4.3 PROT-MSG-DATA-VEND Vendor Defined Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which an Unstructured Vendor Defined message is sent by the UUT.
Critical for Safety	No
Applies to	Any UUT
Description	Checks the validity of formatting of a Vendor message to ensure that it will not cause problems to PD devices which do not recognize it.
Test setup	
Preconditions	The checks will be performed on any occasion when a Vendor message is encountered.
Assertions Tested	6.2.1.8#1, 6.4.4#1, 6.4.4#2, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

14.4.1.9.1 Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.
2. That the MessageType represented by the value in bits 3:0 of the Message Header is 1111b [PROT_MSG_DATA_VEND_1]
3. That B31:16 of the Data Object contains the Vendor ID (VID) value, as specified by the Vendor. [PROT_MSG_DATA_VEND_2]

14.4.1.10 TDB 2.1.4.4.1.1 PROT-MSG-DATA-VDM-ID-INIT Discover ID Initiator Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Discover ID Initiator message is sent by the UUT. Also used for the Discover ID NAK, and Discover ID Busy messages.
Critical for Safety	
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider, Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section. The correct formatting of the Discover ID Initiator message is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.4#7, 6.4.4.2#8, 6.4.4.2#10, 6.4.4.2.1#1, 6.4.4.2.3#1, 6.4.4.2.4#5, 6.4.4.2.5#1, 6.4.4.2.5#2, 6.4.4.3.1#5, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.
2. That the Number of Data Objects represented by the value in bits 14:12 is 1 [PROT_MSG_DATA_VDM_ID_INIT_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 1111b [PROT_MSG_DATA_VDM_ID_INIT_2].

VDO #1 (VDM Header)

4. That, for the first VDO in a Discover ID Initiator, NAK or BUSY message, bits B31:B16 are set to 0xFF00 (defining PD SID) [PROT_MSG_DATA_VDM_ID_INIT_3].
5. That, for the first VDO in a Discover ID Initiator, NAK or BUSY message, bit B15 is 1b (defining a structured VDM) [PROT_MSG_DATA_VDM_ID_INIT_4].

6. That, for the first VDO in a Discover ID Initiator, NAK or BUSY message, bits B14:B13 (Structured VDM Version) are 00b (representing Structured VDM V1.0) [PROT_MSG_DATA_VDM_ID_INIT_5].
7. That, for the first VDO in a Discover ID Initiator, NAK or BUSY message, bits B12:B11 (reserved) are set to 00b [PROT_MSG_DATA_VDM_ID_INIT_6].
8. That, for the first VDO in a Discover ID Initiator, NAK or BUSY message, bits B10:B8 (Object Position) are set to 000b [PROT_MSG_DATA_VDM_ID_INIT_7].
9. That, for the first VDO in a Discover ID Initiator, NAK or BUSY message, bits B7:B6 (Command Type) is set to 00b (Initiator), 10b (NAK) or 11b (BUSY) [PROT_MSG_DATA_VDM_ID_INIT_8].
10. That, for the first VDO in a Discover ID Initiator, NAK or BUSY message, bit B5 (reserved) is set to 0b [PROT_MSG_DATA_VDM_ID_INIT_9].
11. That, for the first VDO in a Discover ID Initiator, NAK or BUSY message, bits B4:B0 are set to 00001b (Discover Identity) [PROT_MSG_DATA_VDM_ID_INIT_10].

14.4.1.11 TDB 2.1.4.4.1.2 PROT-MSG-DATA-VDM-ID-ACK Discover ID ACK Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Discover ID ACK message is sent by the UUT.
Critical for Safety	
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section. The correct formatting of the Discover ID ACK message is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.4#7, 6.4.4.2#8, 6.4.4.2#10, 6.4.4.2.1#1, 6.4.4.2.3#1, 6.4.4.2.4#5, 6.4.4.2.5#1, 6.4.4.3.1#5, 6.4.4.3.1#6, 6.4.4.3.1.1#2, 6.4.4.3.1.1#3, 6.4.4.3.1.1#4, 6.4.4.3.1.1#5, 6.4.4.3.1.4#1, 6.4.4.3.1.6#1, 6.4.4.3.1.7#1, 6.4.4.3.1.7#2, 6.4.4.3.1.8#1, 6.4.4.3.1.9#1, 6.4.4.3.1.9#2, 6.4.4.3.1.9#3, 6.4.4.3.1.10#1, 6.4.4.3.1.10#2, 6.4.4.3.1.10#3, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.
2. That the Number of Data Objects represented by the value in bits 14:12 is 4 or 5 [PROT_MSG_DATA_VDM_ID_ACK_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 1111b [PROT_MSG_DATA_VDM_ID_ACK_2].

VDO #1 (VDM Header)

4. That, for the first VDO in a Discover ID ACK message, bits B31:B16 are set to 0xFF00 (defining PD SID) [PROT_MSG_DATA_VDM_ID_ACK_3].
5. That, for the first VDO in a Discover ID ACK message, bit B15 is 1b (defining a structured VDM) [PROT_MSG_DATA_VDM_ID_ACK_4].

6. That, for the first VDO in a Discover ID ACK message, bits B14:B13 (Structured VDM Version) are 00b (representing Structured VDM V1.0) [PROT_MSG_DATA_VDM_ID_ACK_5].
7. That, for the first VDO in a Discover ID ACK message, bits B12:B11 (reserved) are set to 00b [PROT_MSG_DATA_VDM_ID_ACK_6].
8. That, for the first VDO in a Discover ID ACK message, bits B10:B8 (Object Position) are set to 000b [PROT_MSG_DATA_VDM_ID_ACK_7].
9. That, for the first VDO in a Discover ID ACK message, bits B7:B6 (Command Type) is set to 01b (ACK) [PROT_MSG_DATA_VDM_ID_ACK_8].
10. That, for the first VDO in a Discover ID ACK message, bit B5 (reserved) is set to 0b [PROT_MSG_DATA_VDM_ID_ACK_9].
11. That, for the first VDO in a Discover ID ACK message, bits B4:B0 are set to 00001b (Discover Identity) [PROT_MSG_DATA_VDM_ID_ACK_10].

VDO #2 (ID Header)

12. That, for the second VDO in a Discover ID ACK message, bit B31 (Data Capable as USB Host) is set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_11].
13. That, for the second VDO in a Discover ID ACK message, bit B30 (Data Capable as USB Device) is set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_12].
14. That, for the second VDO in a Discover ID ACK message, bits B29:B27 (Product Type) are set to the expected value based on the vendor supplied information, and not to a reserved value (110b or 111b) [PROT_MSG_DATA_VDM_ID_ACK_13].
15. That, for the second VDO in a Discover ID ACK message, bit B26 (Modal Operation supported) is set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_14].
16. That, for the second VDO in a Discover ID ACK message, bits B25:B16 (reserved) are set to 0000000000b [PROT_MSG_DATA_VDM_ID_ACK_15].
17. That, for the second VDO in a Discover ID ACK message, bits B15:B0 (Vendor ID) are set to the expected value based on the vendor supplied information. The value Vendor ID Unassigned (0000h) is permitted if the vendor does not have an assigned Vendor ID [PROT_MSG_DATA_VDM_ID_ACK_16].

VDO #3 (Cert Stat VDO)

18. That, for the third VDO in a Discover ID ACK message, bits B31:B0 (Test ID) are set to the XID allocated (in decimal) by USB-IF before certification [PROT_MSG_DATA_VDM_ID_ACK_18].

VDO #4 (Product VDO)

19. That, for the fourth VDO in a Discover ID ACK message, bits B31:B16 (USB Product ID) are set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_19].
20. That, for the fourth VDO in a Discover ID ACK message, bits B15:B0 (USB bcdDevice) are set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_20].
21. That if the Product Type in the ID Header is 'Undefined', 'Hub' or 'Peripheral', there are exactly 4 VDOs, and this is the end of this check list [PROT_MSG_DATA_VDM_ID_ACK_21].
22. That if the Product Type in the ID Header is 'Active Cable' or 'Passive Cable' the checks in 'VDO #5 (Cable VDO)' are satisfied. [PROT_MSG_DATA_VDM_ID_ACK_49]
23. That if the Product Type in the ID Header is 'Alternate Mode Adapter' the checks in 'VDO #5 (AMA VDO)' are satisfied. [PROT_MSG_DATA_VDM_ID_ACK_50]

VDO #5 (Cable VDO)

24. That, for the fifth VDO in a Discover ID ACK message, bits B31:B28 (HW Version) are set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_22].
25. That, for the fifth VDO in a Discover ID ACK message, bits B27:B24 (Firmware Version) are set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_23].
26. That, for the fifth VDO in a Discover ID ACK message, bits B23:B20 (reserved) are set to 0000b [PROT_MSG_DATA_VDM_ID_ACK_24].
27. That, for the fifth VDO in a Discover ID ACK message, bits B19:B18 (Type-C to Type-A/B/C) are set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_25].
28. That, for the fifth VDO in a Discover ID ACK message, bit B17 (Type-C to Plug/Receptacle) is set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_26].
29. That, for the fifth VDO in a Discover ID ACK message, bits B16:B13 (Cable Latency) are set to the expected value based on the vendor supplied information. Check that the value is not a reserved value (0000b, 1011b, 1100b, 1101b, 1110b or 1111b) [PROT_MSG_DATA_VDM_ID_ACK_27].
30. That, for the fifth VDO in a Discover ID ACK message, bits B12:B11 (Cable Termination type) are set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_28].
31. That, for the fifth VDO in a Discover ID ACK message, bits B10:B7 (Reserved) are set zero [PROT_MSG_DATA_VDM_ID_ACK_51].

32. That, for the fifth VDO in a Discover ID ACK message, bits B6:B5 (Vbus Current Handling Capability) are set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_33].
33. That, for the fifth VDO in a Discover ID ACK message from an Active Cable, bit B4 (Vbus through cable) is set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_34].
34. That, for the fifth VDO in a Discover ID ACK message from a Passive Cable, bit B4 (Reserved) is set to zero [PROT_MSG_DATA_VDM_ID_ACK_52].
35. That, for the fifth VDO in a Discover ID ACK message from an Active Cable, bit B3 (SOP" controller present) is set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_35].
36. That, for the fifth VDO in a Discover ID ACK message from a Passive Cable, bit B3 (Reserved) is set to zero [PROT_MSG_DATA_VDM_ID_ACK_53].
37. That, for the fifth VDO in a Discover ID ACK message, bits B2:B0 (USB Superspeed Signaling Support) are set to the expected value based on the vendor supplied information. Check that the value is not a reserved value (011b, 100b, 101b, 110b or 111b) [PROT_MSG_DATA_VDM_ID_ACK_36].
38. That there are no following VDOs [PROT_MSG_DATA_VDM_ID_ACK_48].

VDO #5 (AMA VDO)

39. That, for the fifth VDO in a Discover ID ACK message, bits B31:B28 (HW Version) are set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_37].
40. That, for the fifth VDO in a Discover ID ACK message, bits B27:B24 (Firmware Version) are set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_38].
41. That, for the fifth VDO in a Discover ID ACK message, bits B23:B12 (reserved) are set to 000000000000b [PROT_MSG_DATA_VDM_ID_ACK_39].
42. That, for the fifth VDO in a Discover ID ACK message, bit B11:B8 (Reserved) is set to zero [PROT_MSG_DATA_VDM_ID_ACK_54].
43. That, for the fifth VDO in a Discover ID ACK message, bits B7:B5 (Vconn power) are set to the expected value based on the vendor supplied information. Check that the value is not a reserved value (111b) [PROT_MSG_DATA_VDM_ID_ACK_44].
44. That, for the fifth VDO in a Discover ID ACK message, bit B4 (Vconn required) is set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_45].
45. That, for the fifth VDO in a Discover ID ACK message, bit B3 (Vbus required) is set to the expected value based on the vendor supplied information [PROT_MSG_DATA_VDM_ID_ACK_46].
46. That, for the fifth VDO in a Discover ID ACK message, bits B2:B0 (USB Superspeed Signaling Support) are set to the expected value based on the vendor supplied information.

Check that the value is not a reserved value (100b, 101b, 110b or 111b) [PROT_MSG_DATA_VDM_ID_ACK_47].

47. That there are no following VDOs [PROT_MSG_DATA_VDM_ID_ACK_48].

14.4.1.12 TDB 2.1.4.4.2.1 PROT-MSG-DATA-VDM-SVID-INIT Discover SVIDs Initiator Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Discover SVIDs Initiator message is sent by the UUT. Also used for the Discover SVIDs NAK, and Discover SVIDs Busy messages.
Critical for Safety	
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider, Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section. The correct formatting of the Discover SVIDs Initiator message is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.4#7, 6.4.4.2#8, 6.4.4.2#10, 6.4.4.2.1#1, 6.4.4.2.3#1, 6.4.4.2.4#5, 6.4.4.2.5#1, 6.4.4.2.5#2, 6.4.4.3.2#4, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.
2. That the Number of Data Objects represented by the value in bits 14:12 is 1 [PROT_MSG_DATA_VDM_SVID_INIT_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 1111b [PROT_MSG_DATA_VDM_SVID_INIT_2].

VDO #1 (VDM Header)

4. That, for the first VDO in a Discover SVIDs Initiator, NAK or BUSY message, bits B31:B16 are set to 0xFF00 (defining PD SID) [PROT_MSG_DATA_VDM_SVID_INIT_3].

5. That, for the first VDO in a Discover SVIDs Initiator, NAK or BUSY message, bit B15 is 1b (defining a structured VDM) [PROT_MSG_DATA_VDM_SVID_INIT_4].
6. That, for the first VDO in a Discover SVIDs Initiator, NAK or BUSY message, bits B14:B13 (Structured VDM Version) are 00b (representing Structured VDM V1.0) [PROT_MSG_DATA_VDM_SVID_INIT_5].
7. That, for the first VDO in a Discover SVIDs Initiator, NAK or BUSY message, bits B12:B11 (reserved) are set to 00b [PROT_MSG_DATA_VDM_SVID_INIT_6].
8. That, for the first VDO in a Discover SVIDs Initiator, NAK or BUSY message, bits B10:B8 (Object Position) are set to 000b [PROT_MSG_DATA_VDM_SVID_INIT_7].
9. That, for the first VDO in a Discover SVIDs Initiator, NAK or BUSY message, bits B7:B6 (Command Type) is set to 00b (Initiator), 10b (NAK) or 11b (BUSY) [PROT_MSG_DATA_VDM_SVID_INIT_8].
10. That, for the first VDO in a Discover SVIDs Initiator, NAK or BUSY message, bit B5 (reserved) is set to 0b [PROT_MSG_DATA_VDM_SVID_INIT_9].
11. That, for the first VDO in a Discover SVIDs Initiator, NAK or BUSY message, bits B4:B0 are set to 00010b (Discover SVIDs) [PROT_MSG_DATA_VDM_SVID_INIT_10].

14.4.1.13 TDB 2.1.4.4.2.2 PROT-MSG-DATA-VDM-SVID-ACK Discover SVIDs ACK Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Discover SVIDs ACK message is sent by the UUT.
Critical for Safety	
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.4#7, 6.4.4.2#8, 6.4.4.2#10, 6.4.4.2.1#1, 6.4.4.2.3#1, 6.4.4.2.4#5, 6.4.4.2.5#1, 6.4.4.3.2#4, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.
2. That the Number of Data Objects represented by the value in bits 14:12 is at least 2 [PROT_MSG_DATA_VDM_SVID_ACK_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 1111b [PROT_MSG_DATA_VDM_SVID_ACK_2].

VDO #1 (VDM Header)

4. That, for the first VDO in a Discover SVIDs ACK message, bits B31:B16 are set to 0xFF00 (defining PD SID) [PROT_MSG_DATA_VDM_SVID_ACK_3].
5. That, for the first VDO in a Discover SVIDs ACK message, bit B15 is 1b (defining a structured VDM) [PROT_MSG_DATA_VDM_SVID_ACK_4].
6. That, for the first VDO in a Discover SVIDs ACK message, bits B14:B13 (Structured VDM Version) are 00b (representing Structured VDM V1.0) [PROT_MSG_DATA_VDM_SVID_ACK_5].
7. That, for the first VDO in a Discover SVIDs ACK message, bits B12:B11 (reserved) are set to 00b [PROT_MSG_DATA_VDM_SVID_ACK_6].
8. That, for the first VDO in a Discover SVIDs ACK message, bits B10:B8 (Object Position) are set to 000b [PROT_MSG_DATA_VDM_SVID_ACK_7].
9. That, for the first VDO in a Discover SVIDs ACK message, bits B7:B6 (Command Type) is set to 01b (ACK) [PROT_MSG_DATA_VDM_SVID_ACK_8].
10. That, for the first VDO in a Discover SVIDs ACK message, bit B5 (reserved) is set to 0b [PROT_MSG_DATA_VDM_SVID_ACK_9].
11. That, for the first VDO in a Discover SVIDs ACK message, bits B4:B0 are set to 00010b (Discover SVIDs) [PROT_MSG_DATA_VDM_SVID_ACK_10].

Each following VDO (Discover SVIDs Responder VDO)

12. That, for this VDO in a Discover SVIDs ACK message, bits B31:B16 (SVID n) are set to the expected value based on the vendor supplied information. This means either a valid SID or VID, or the value zero. If zero, this marks the end of the list; in this case check that the next value is zero [PROT_MSG_DATA_VDM_SVID_ACK_11].
13. Check that the first Discover SVIDs ACK VDO, in the first Discover SVIDs ACK message received, contains at least one (non-zero) SVID [PROT_MSG_DATA_VDM_SVID_ACK_12].
14. That, for this VDO in a Discover SVIDs ACK message, bits B15:B0 (SVID n+1) are set to the expected value based on the vendor supplied information. This means either a valid SID or VID, or the value zero. If zero, this marks the end of the list; in this case check that no further VDOs are present [PROT_MSG_DATA_VDM_SVID_ACK_13].

14.4.1.14 TDB 2.1.4.4.3.1 PROT-MSG-DATA-VDM-MODE-INIT Discover Modes Initiator Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Discover Modes Initiator message is sent by the UUT. Also used for the Discover Modes NAK, and Discover Modes Busy messages.
Critical for Safety	
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider, Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section. The correct formatting of the Discover Modes Initiator, NAK or Busy message is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.4#7, 6.4.4.2#8, 6.4.4.2#10, 6.4.4.2.1#1, 6.4.4.2.3#1, 6.4.4.2.4#5, 6.4.4.2.5#1, 6.4.4.2.5#2, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.
2. That the Number of Data Objects represented by the value in bits 14:12 is 1 [PROT_MSG_DATA_VDM_MODE_INIT_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 1111b [PROT_MSG_DATA_VDM_MODE_INIT_2].

VDO #1 (VDM Header)

4. That, for the first VDO in a Discover Modes Initiator, NAK or BUSY message, bits B31:B16 are set to 0xFF00 (defining PD SID) [PROT_MSG_DATA_VDM_MODE_INIT_3].
5. That, for the first VDO in a Discover Modes Initiator, NAK or BUSY message, bit B15 is 1b (defining a structured VDM) [PROT_MSG_DATA_VDM_MODE_INIT_4].

6. That, for the first VDO in a Discover Modes Initiator, NAK or BUSY message, bits B14:B13 (Structured VDM Version) are 00b (representing Structured VDM V1.0) [PROT_MSG_DATA_VDM_MODE_INIT_5].
7. That, for the first VDO in a Discover Modes Initiator, NAK or BUSY message, bits B12:B11 (reserved) are set to 00b [PROT_MSG_DATA_VDM_MODE_INIT_6].
8. That, for the first VDO in a Discover Modes Initiator, NAK or BUSY message, bits B10:B8 (Object Position) are set to 000b [PROT_MSG_DATA_VDM_MODE_INIT_7].
9. That, for the first VDO in a Discover Modes Initiator, NAK or BUSY message, bits B7:B6 (Command Type) is set to 00b (Initiator), 10b (NAK) or 11b (BUSY) [PROT_MSG_DATA_VDM_MODE_INIT_8].
10. That, for the first VDO in a Discover Modes Initiator, NAK or BUSY message, bit B5 (reserved) is set to 0b [PROT_MSG_DATA_VDM_MODE_INIT_9].
11. That, for the first VDO in a Discover Modes Initiator, NAK or BUSY message, bits B4:B0 are set to 00011b (Discover Modes) [PROT_MSG_DATA_VDM_MODE_INIT_10].

14.4.1.15 TDB 2.1.4.4.3.2 PROT-MSG-DATA-VDM-MODE-ACK Discover Modes ACK Message Check

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Discover Modes ACK message is sent by the UUT.
Critical for Safety	
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.4#7, 6.4.4.2#8, 6.4.4.2#10, 6.4.4.2.1#1, 6.4.4.2.3#1, 6.4.4.2.4#5, 6.4.4.2.5#1, 6.4.4.3.3#1, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.

2. That the Number of Data Objects represented by the value in bits 14:12 is at least 2 [PROT_MSG_DATA_VDM_MODE_ACK_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 1111b [PROT_MSG_DATA_VDM_MODE_ACK_2].

VDO #1 (VDM Header)

4. That, for the first VDO in a Discover Modes ACK message, bits B31:B16 are set to the SVID specified in the preceding Discover Modes initiator message [PROT_MSG_DATA_VDM_MODE_ACK_3].
5. That, for the first VDO in a Discover Modes ACK message, bit B15 is 1b (defining a structured VDM) [PROT_MSG_DATA_VDM_MODE_ACK_4].
6. That, for the first VDO in a Discover Modes ACK message, bits B14:B13 (Structured VDM Version) are 00b (representing Structured VDM V1.0) [PROT_MSG_DATA_VDM_MODE_ACK_5].
7. That, for the first VDO in a Discover Modes ACK message, bits B12:B11 (reserved) are set to 00b [PROT_MSG_DATA_VDM_MODE_ACK_6].
8. That, for the first VDO in a Discover Modes ACK message, bits B10:B8 (Object Position) are set to 000b [PROT_MSG_DATA_VDM_MODE_ACK_7].
9. That, for the first VDO in a Discover Modes ACK message, bits B7:B6 (Command Type) is set to 01b (ACK) [PROT_MSG_DATA_VDM_MODE_ACK_8].
10. That, for the first VDO in a Discover Modes ACK message, bit B5 (reserved) is set to 0b [PROT_MSG_DATA_VDM_MODE_ACK_9].
11. That, for the first VDO in a Discover Modes ACK message, bits B4:B0 are set to 00011b (Discover Modes) [PROT_MSG_DATA_VDM_MODE_ACK_10].

Each following VDO (Discover Modes Responder VDO)

12. The content of the Discover Modes Responder VDO is currently not checked.

14.4.1.16 TDB 2.1.4.4.4 PROT-MSG-DATA-VDM-ENTER-MODE Enter Mode Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Enter Mode message is sent by the UUT.
Critical for Safety	

Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider, Consumer or Cable
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.4#7, 6.4.4.2#8, 6.4.4.2.1#1, 6.4.4.2.3#1, 6.4.4.2.4#5, 6.4.4.2.5#1, 6.4.4.2.5#2, 6.4.4.3.4#1, 6.4.4.3.4#4, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.
2. That the Number of Data Objects represented by the value in bits 14:12 is 1. [PROT_MSG_DATA_VDM_ENTER_MODE_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 1111b [PROT_MSG_DATA_VDM_ENTER_MODE_2].

VDO #1 (VDM Header)

4. That, for the first VDO in an Enter Mode message, bits B31:B16 are set to an SVID specified in a preceding Discover SVIDs ACK message and, if the current message is not an initiator, that the SVID matches the one specified in the corresponding previous initiator [PROT_MSG_DATA_VDM_ENTER_MODE_3].
5. That, for the first VDO in an Enter Mode message, bit B15 is 1b (defining a structured VDM) [PROT_MSG_DATA_VDM_ENTER_MODE_4].
6. That, for the first VDO in an Enter Mode message, bits B14:B13 (Structured VDM Version) are 00b (representing Structured VDM V1.0) [PROT_MSG_DATA_VDM_ENTER_MODE_5].
7. That, for the first VDO in an Enter Mode message, bits B12:B11 (reserved) are set to 00b [PROT_MSG_DATA_VDM_ENTER_MODE_6].
8. That, for the first VDO in an Enter Mode message, bits B10:B8 (Object Position) are set to an Object Position specified in a preceding Discover Modes ACK message and, if the current message is not an initiator, that the Object Position matches the one specified in the corresponding previous initiator [PROT_MSG_DATA_VDM_ENTER_MODE_7].
9. That, for the first VDO in an Enter Mode message, bits B7:B6 (Command Type) is set to 00b (Initiator), 01b (ACK) or 10b (NAK) [PROT_MSG_DATA_VDM_ENTER_MODE_8].
10. That, for the first VDO in an Enter Mode message, bit B5 (reserved) is set to 0b [PROT_MSG_DATA_VDM_ENTER_MODE_9].

11. That, for the first VDO in an Enter Mode message, bits B4:B0 are set to 00100b (Enter Mode) [PROT_MSG_DATA_VDM_ENTER_MODE_10].

Following VDOs

12. Check that there are no further VDOs [PROT_MSG_DATA_VDM_ENTER_MODE_11].

14.4.1.17 TDB 2.1.4.4.5 PROT-MSG-DATA-VDM-EXIT-MODE Exit Mode Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Exit Mode message is sent by the UUT.
Critical for Safety	
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider, Consumer or Cable
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.4#7, 6.4.4.2#8, 6.4.4.2.1#1, 6.4.4.2.3#1, 6.4.4.2.4#5, 6.4.4.2.5#1, 6.4.4.2.5#2, 6.4.4.3.5#1, 6.4.4.3.5#3, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.
2. That the Number of Data Objects represented by the value in bits 14:12 is 1. [PROT_MSG_DATA_VDM_EXIT_MODE_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 1111b [PROT_MSG_DATA_VDM_EXIT_MODE_2].

VDO #1 (VDM Header)

4. That, for the first VDO in an Exit Mode ACK message, bits B31:B16 are set to the SVID specified in the preceding Exit Mode initiator message [PROT_MSG_DATA_VDM_EXIT_MODE_3].
5. That, for the first VDO in an Exit Mode ACK message, bit B15 is 1b (defining a structured VDM) [PROT_MSG_DATA_VDM_EXIT_MODE_4].

6. That, for the first VDO in an Exit Mode ACK message, bits B14:B13 (Structured VDM Version) are 00b (representing Structured VDM V1.0) [PROT_MSG_DATA_VDM_EXIT_MODE_5].
7. That, for the first VDO in an Exit Mode ACK message, bits B12:B11 (reserved) are set to 00b [PROT_MSG_DATA_VDM_EXIT_MODE_6].
8. That, for the first VDO in an Exit Mode ACK message, bits B10:B8 (Object Position) are set to the value specified in the preceding EXIT Mode initiator message [PROT_MSG_DATA_VDM_EXIT_MODE_7].
9. That, for the first VDO in an EXIT Mode ACK message, bits B7:B6 (Command Type) is set to 00b (Initiator) or 01b (ACK) [PROT_MSG_DATA_VDM_EXIT_MODE_8].
10. That, for the first VDO in an EXIT Mode ACK message, bit B5 (reserved) is set to 0b [PROT_MSG_DATA_VDM_EXIT_MODE_9].
11. That, for the first VDO in an EXIT Mode ACK message, bits B4:B0 are set to 00100b (Exit Mode) [PROT_MSG_DATA_VDM_EXIT_MODE_10].

Following VDOs

12. Check that there are no further VDOs [PROT_MSG_DATA_VDM_EXIT_MODE_11].

14.4.1.18 TDB 2.1.4.4.6 PROT-MSG-DATA-VDM-ATT Attention Message Checks

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Attention message is sent by the UUT.
Critical for Safety	
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider, Consumer
Description	This section is a list of specific checks to be made in the course of any other test in this document which refers to this section.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.2.1.2#1, 6.2.1.8#1, 6.4.4#7, 6.4.4.2#2, 6.4.4.2#8, 6.4.4.2.1#1, 6.4.4.2.3#1, 6.4.4.2.5#1, 6.4.4.2.5#2, 6.4.4.3.6#1, 6.4.4.3.6#3, plus assertions in checks: PROT-HDR
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, ensure that the following checks are carried out:

1. All the Message Header Checks detailed in PROT-HDR.

2. That the Number of Data Objects represented by the value in bits 14:12 is 1 [PROT_MSG_DATA_VDM_ATT_1].
3. That the MessageType represented by the value in bits 3:0 of the Message Header is 1111b [PROT_MSG_DATA_VDM_ATT_2].
4. That this message was not sent by a Cable Marker, and was not sent using SOP' or SOP" [PROT_MSG_DATA_VDM_ATT_12].

VDO #1 (VDM Header)

5. That, for the first VDO in an Attention message, bits B31:B16 are set to the SVID specified in the preceding Enter Mode initiator message [PROT_MSG_DATA_VDM_ATT_3].
6. That, for the first VDO in an Attention message, bit B15 is 1b (defining a structured VDM) [PROT_MSG_DATA_VDM_ATT_4].
7. That, for the first VDO in an Attention message, bits B14:B13 (Structured VDM Version) are 00b (representing Structured VDM V1.0) [PROT_MSG_DATA_VDM_ATT_5].
8. That, for the first VDO in an Attention message, bits B12:B11 (reserved) are set to 00b [PROT_MSG_DATA_VDM_ATT_6].
9. That, for the first VDO in an Attention message, bits B10:B8 (Object Position) are set to the value specified in the preceding Enter Mode initiator message [PROT_MSG_DATA_VDM_ATT_7].
10. That, for the first VDO in an Attention message, bits B7:B6 (Command Type) is set to 00b (Initiator - no other value is allowed) [PROT_MSG_DATA_VDM_ATT_8].
11. That, for the first VDO in an Attention message, bit B5 (reserved) is set to 0b [PROT_MSG_DATA_VDM_ATT_9].
12. That, for the first VDO in an Attention message, bits B4:B0 are set to 00100b (Exit Mode) [PROT_MSG_DATA_VDM_ATT_10].

Following VDOs

13. Check that there are no further VDOs [PROT_MSG_DATA_VDM_ATT_11].

14.4.2 Procedures and Procedure Checks

The following are checks to be performed on procedures, **whenever** they are encountered during a Primary Test.

14.4.2.1 TDB 2.2.1.1 PROT-PROC-AMS for Atomic Message Sequence

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which a message is sent in response to another message as part of an Atomic Message Sequence.
Critical for Safety	No
Applies to	Any
Description	The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.5.2#5, plus assertions in checks: PROT-MSG-CTRL
Parameters Tested	
Checklist References	

Test Procedure

During any test in which a message from the UUT is in response to a message from the Tester as part of an Atomic Message Sequence:

1. Check that the time from the last bit of the message sent by the Tester until the start of the response does not exceed 15ms (except in cases where another criterion is specified e.g. power transition timings). [PROT_PROC_AMS_1]

14.4.2.2 TDB 2.2.2.1 PROT-PROC-GOODCRC-TSTR for GoodCRC from Tester

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which a GoodCRC is sent by the Tester in response to any other message.
Critical for Safety	No
Applies to	Cable, DRP, Provider, Consumer , Provider/Consumer, Consumer/Provider
Description	This section describes the procedure which starts with a Tester originated GoodCRC message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	assertions in checks: PROT-MSG-CTRL
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. Send a GoodCRC message, alternately starting the preamble after tInterframeGap min (25µs) and tTransmit max (195 µs) of the last bit of the previously received message.

14.4.2.3 TDB 2.2.2.2 PROT-PROC-GOODCRC-UUT for GoodCRC from UUT

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which a GoodCRC is sent by the UUT in response to any other message.
Critical for Safety	No
Applies to	Cable, DRP, Provider, Consumer , Provider/Consumer, Consumer/Provider
Description	This section describes the procedure which starts with a UUT originated GoodCRC message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.1#3, 6.5.1#6, 6.5.1#7, plus assertions in checks: PROT-MSG-CTRL
Parameters Tested	tBusIdle, tTransmit
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. Check that the first bit of the preamble of a GoodCRC is received after tInterframeGap min (25μs) to tTransmit max (195 μs) of the last bit of the previously sent message. [PROT_PROC_GOODCRC_UUT_1]
2. Check that this GoodCRC message meets the requirements of PROT-MSG-CTRL. [PROT_PROC_GOODCRC_UUT_2]

14.4.2.4 TDB 2.2.3.1.1 PROT-PROC-SWAP-TSTR-SNK Tester (Sink) Originated Swap

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Swap message is sent by the Tester acting as a Sink.
Critical for Safety	No
Applies to	DRP, Provider/Consumer, Consumer/Provider
14.4.2.4.1 Description	This section describes the procedure which starts with a Tester originated Swap message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.3#2, 6.3.3#6, 6.3.6#1, 6.3.10#1, 6.3.10#2, 6.5.2#5, 6.5.3.1#1, 6.5.3.1#2, 6.5.3.1#3, 6.5.6.2#2, 7.1.11#1, 7.1.11#2, 7.1.11#3, 7.2.4#2, 7.2.4#4, 7.3.9#1, 7.3.9#2, 7.3.9#3, 7.3.9#4, 7.3.9#6, plus assertions in checks: PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	tReceiverResponse, tTypeCSinkWaitCap, tSourceActivity,
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. Send a Swap message to the UUT (Source).
2. Check that an Accept message is received from UUT within tReceiverResponse max (15ms) of the last bit of the Request message. [PROT_PROC_SWAP_TSTR_SNK_1]
3. Check that this Accept message meets the requirements of PROT-MSG-CTRL.
4. Ensure that we are drawing no more than iSwapStandby within tSrcTransition min (25ms) after we sent the last GoodCRC.
5. Check that the UUT reduces its Vbus voltage to vSafe0V max (0.8V) within tSrcTransition max (35ms) plus tSrcSwapStdby max (650ms) after the last bit of GoodCRC was sent in response to the received Accept. [PROT_PROC_SWAP_TSTR_SNK_3] We do not check that the UUT stops driving Vbus.

6. The UUT may sends Ping(s) if it is attempting to meet the timing tSourceActivity (40ms to 50ms). However, this is optional, so not checked.
7. Check that we receive a PS_RDY message after Vbus reaches vSafe0V, and by no later than tSrcTransition max (35ms) plus tSrcSwapStdby max (650ms) after after the last bit of GoodCRC was sent in response to the received Accept. [PROT_PROC_SWAP_TSTR_SNK_5]
8. Check that this PS_RDY message meets the requirements of PROT-MSG-CTRL.
9. If the Tester Ping Policy is currently to send Pings, from now on send Ping messages if required to meet the timing tSourceActivity (40ms to 50ms). If the Ping Policy for the test is not to send Pings, then do not send Pings.
10. Turn on Vbus drive and take it to vSafe5V completing the transition before sending PS_RDY, both within tNewSRC max (275ms) of the GoodCRC we sent in response to the PS_RDY from the UUT.
11. If we are in a 'PSSourceOnTimer Test', then go to PROT-PROC-PSSOURCEONTIMER or PROT-PROC-PSSOURCEONTIMER-SWPD as appropriate, and complete test there.
12. Send this PS_RDY.
13. Wait 300ms from the time when Vbus rose above vSafe0V (so just under tTypeCSinkWaitCap min) and then send Source Capabilities. This is deliberate 'out of spec' behavior to test the tTypeCSinkWaitCap parameter.
14. Check that we receive a Request and that the UUT draws no more than pSnkSusp max/5 (25/5 = 5mA) until we Accept the Request. [PROT_PROC_SWAP_TSTR_SNK_6]
15. Continue using procedure PROT-PROC-REQ-UUT.

14.4.2.5 TDB 2.2.3.1.2 PROT-PROC-SWAP-TSTR-SRC Tester (Source) Originated Swap

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Swap message is sent by the Tester acting as a Source.
Critical for Safety	No
Applies to	DRP, Provider/Consumer, Consumer/Provider
Description	This section describes the procedure which starts with a Tester originated Swap message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.3#2, 6.3.3#6, 6.3.6#1, 6.3.10#1, 6.3.10#2, 6.5.3.1#1, 6.5.3.1#2, 6.5.3.1#3, 6.5.6.3#1, 6.5.9.2#1, 7.1.2#4, 7.1.11#1, 7.1.11#2, 7.1.11#3, 7.1.11#4, 7.2.2#5, 7.2.7#1, 7.2.7#2, 7.2.7#3, 7.2.7#4, plus assertions in checks: PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	tTypeCSinkWaitCap, tSourceActivity
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. Send a Swap message to the UUT (Sink).
2. Check that an Accept message is received from UUT within tReceiverResponse max (15ms) of the last bit of the Request message. [PROT_PROC_SWAP_TSTR_SRC_1]
3. Check this message (PROT-MSG-CTRL).
4. If the Tester Ping Policy is currently to send Pings, from now on send Ping messages if required to meet the timing tSourceActivity (40ms to 50ms). If the Ping Policy for the test is not to send Pings, then do not send Pings.
5. Check that UUT is not drawing more than iSwapStandby after a time tSourceTransition min (25ms) after the last bit of GoodCRC is sent in response to the Accept we received. [PROT_PROC_SWAP_TSTR_SRC_2]

6. Starting at tSinkTransition max (35ms) after the last bit of GoodCRC was sent in response to the Accept we received, reduce the Vbus voltage to less than vSafe0V max (0.8V) within tSrcSwapStdby max (650ms) and stop driving Vbus.
7. If we are in a 'PSSourceOffTimer Test', then go to PROT-PROC-PSSOURCEOFFTIMER or PROT-PROC-PSSOURCEOFFTIMER-SWPD as appropriate, and complete test there.
8. Send PS_RDY immediately following this tSrcSwapStdby period.
9. Check that the UUT takes Vbus to vSafe5V (4.75V to 5.5V) and only once it is in this range that it sends PS_RDY [PROT_PROC_SWAP_TSTR_SRC_4]
10. Check this message (PROT-MSG-CTRL).
11. Check that this PS_RDY was started within tNewSrc max (275ms) of the GoodCRC we sent in response to the PS_RDY from the UUT [PROT_PROC_SWAP_TSTR_SRC_6]
12. Check that the UUT sends a Source Capabilities message within tFirstSourceCap max (250ms). [PROT_PROC_SWAP_TSTR_SRC_7]

14.4.2.6 TDB 2.2.3.2.1 PROT-PROC-SWAP-UUT-SNK UUT (Sink) Originated Swap

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Swap message is sent by the UUT acting as a Sink.
Critical for Safety	No
Applies to	DRP, Provider/Consumer, Consumer/Provider
Description	This section describes the procedure which starts with a Tester originated Swap message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.6#1, 6.5.3.1#1, 6.5.3.1#2, 6.5.3.1#3, 7.1.2#4, 7.1.11#1, 7.1.11#2, 7.1.11#3, 7.1.11#4, 7.1.11#5, 7.2.2#5, 7.2.7#1, 7.2.7#2, 7.2.7#3, 7.2.7#4, 7.2.7#5, 7.3.9#1, 7.3.9#2, 7.3.9#3, 7.3.9#4, 7.3.9#6, plus assertions in checks: PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	tSinkWaitCap, tSourceActivity
Checklist References	

14.4.2.6.1 Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester receives a PR_Swap message from the UUT. Check that the details of this message are valid, and as expected (PROT-MSG-CTRL).
2. Send an Accept message after slightly less than tSenderResponse min (24-1=23ms) from the last bit of the GoodCRC message sent (this is out of spec, in order to test the parameter tSenderResponse, but should not cause misoperation). [PROT_PROC_SWAP_UUT_SNK_1]
3. If the Tester Ping Policy is currently to send Pings, from now on send Ping messages if required to meet the timing tSourceActivity (40ms to 50ms). If the Ping Policy for the test is not to send Pings, then do not send Pings.

4. Check that UUT is not drawing more than iSnkSwapStandby after a time tSrcTransition max (35ms) after the last bit of GoodCRC is received in response to the Accept we sent. [PROT_PROC_SWAP_UUT_SNK_3]
5. Starting at tSrcTransition max (35ms) after the last bit of GoodCRC is received in response to the Accept we sent, reduce the Vbus voltage to less than vSafe0V max (0.8V) within tSrcSwapStdby max (650ms) and stop driving Vbus [PROT_PROC_SWAP_UUT_SNK_4]
6. If we are in a 'PSSourceOffTimer Test', then go to PROT-PROC-PSSOURCEOFFTIMER or PROT-PROC-PSSOURCEOFFTIMER-SWPD as appropriate, and complete test there.
7. Send PS_RDY immediately following this tSrcSwapStdby period. [PROT_PROC_SWAP_UUT_SNK_5]
8. Check that the UUT takes Vbus to vSafe5V (4.75V to 5.50V) and only once it is in this range that it sends PS_RDY [PROT_PROC_SWAP_UUT_SNK_6]
9. Check that this PS_RDY was finished within tPSSourceOn max (480ms) of the GoodCRC we sent in response to the PS_RDY from the UUT [PROT_PROC_SWAP_UUT_SNK_8]
10. Check this PS_RDY message (PROT-MSG-CTRL)
11. Check that the UUT sends a Source Capabilities message within tFirstSourceCap max(250ms). [PROT_PROC_SWAP_UUT_SNK_9]

14.4.2.7 TDB 2.2.3.2.2 PROT-PROC-SWAP-UUT-SRC UUT (Source) Originated Swap

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Swap message is sent by the UUT acting as a Source.
Critical for Safety	No

Applies to	DRP, Provider/Consumer, Consumer/Provider
Description	This section describes the procedure which starts with a Tester originated Swap message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.6#1, 6.5.3.1#1, 6.5.3.1#2, 6.5.3.1#3, 7.1.11#1, 7.3.10#4, 7.3.10#6, 7.3.10#7, plus assertions in checks: PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	tTypeCSinkWaitCap, tSourceActivity
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester receives a Swap message from the UUT. Check that the details of this message are valid, and as expected (PROT-MSG-CTRL).
2. Send an Accept message after slightly less than tSenderResponse min (24-1=23ms) from the last bit of the GoodCRC message sent (this is out of spec, in order to test the parameter tSenderResponse, but should not cause misoperation).
3. Ensure that we are drawing no more than iSwapStandby within tSrcTransition max (35ms) after we sent the last GoodCRC.
4. Check that the UUT reduces its Vbus voltage to vSafe0V max (0.8V) within tSrcTransition max (35ms) plus tSrcSwapStdby max (650ms) after the last bit of GoodCRC was sent in response to the received Accept. We do not check that the UUT stops driving Vbus. [PROT_PROC_SWAP_UUT_SRC_1]
5. Check that we receive a PS_RDY message after Vbus reaches vSafe0V and by no later than tPSSourceOff max (920ms) after the last bit of GoodCRC was sent in response to the received Accept. [PROT_PROC_SWAP_UUT_SRC_2]
6. Check this message (PROT-MSG-CTRL).
7. If the Tester Ping Policy is currently to send Pings, from now on send Ping messages if required to meet the timing tSourceActivity (40ms to 50ms). If the Ping Policy for the test is not to send Pings, then do not send Pings.
8. Turn on Vbus drive and take it to vSafe5V, with a rise time within tNewSRC max (275ms), and completing the transition in time to send PS_RDY timed to arrive at just under

tPSSourceOn max (480ms) of the GoodCRC we sent in response to the PS_RDY from the UUT. [PROT_PROC_SWAP_UUT_SRC_3]

9. If we are in a 'PSSourceOnTimer Test', then go to PROT-PROC-PSSOURCEONTIMER or PROT-PROC-PSSOURCEONTIMER-SWPD as appropriate, and complete test there.
10. Send this PS_RDY
11. Wait just under tTypeCSinkWaitCap min (310ms - 10ms = 300ms) and then send Source Capabilities. This is deliberate 'out of spec' behavior to test the tTypeCSinkWaitCap parameter.
12. Check that we receive a Request and that the UUT draws no more than pSnkSusp max/5 (25/5 = 5mA) until we Accept the Request. [PROT_PROC_SWAP_UUT_SRC_4]

14.4.2.8 TDB 2.2.4 PROT-PROC-PSSOURCEOFFTIMER PSSourceOffTimer

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the PSSourceOffTimer test, as an alternative to completing the a appropriate Swap test.
Critical for Safety	No
Applies to	DRP, Provider /Consumer, Consumer/Provider
Description	This section describes the procedure to test PSSourceOffTimer. The main element is the failure to send the first PS_RDY when expected by the UUT. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.5.6.2#1, 6.5.6.2#2, 6.5.6.2#3, 6.5.6.2#4, 7.1.1#4, plus assertions in checks: PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	vSafe0V, tPSSourceOff, tSwapRecover
Checklist References	

Test Procedure for Not Sending First PS_RDY

During any test which refers to this section, follow this procedure:

Note: We are testing PSSourceOffTimer by failing to send PS_RDY, so we were the Source and have just turned off Vbus.

1. Do not send this (1st) PS_RDY (also stop sending Pings if we were sending them). Maintain Rp at 4k7 to 3.3V.
2. Check that within tPSSourceOff max (920ms) of the last bit of the EOP that we sent in response to receiving the Accept from the UUT, the UUT transitions to Error Recovery. [PROT_PROC_PSSOURCEOFFTIMER_1]
3. The test which contains this sequence ends at this point, by simulating a tester end cable detach.

14.4.2.9 TDB 2.2.5 PROT-PROC-PSSOURCEONTIMER PSSourceOnTimer

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the PSSourceOnTimer test, as an alternative to completing the a appropriate Swap test.
Critical for Safety	No
Applies to	DRP, Provider /Consumer, Consumer/Provider
Description	This section describes the procedure to test PSSourceOnTimer. The main element is the failure to send the second PS_RDY when expected by the UUT. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.5.6.3#1, 6.5.6.3#2, 6.5.9.1#1, 7.1.1#4, plus assertions in checks: PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	vSafe0V, vSafe5V, tPSSourceOn, tSwapRecover
Checklist References	

Test Procedure for Not Sending Second PS_RDY

During any test which refers to this section, follow this procedure:

Note: We are testing PSSourceOnTimer by failing to send PS_RDY, so we have become Source, connected Rp and just turned on vSafe5V; UUT has connected Rd.

1. Do not send this (2nd) PS_RDY (also do not send any Pings).
2. Check that within tPSSourceOn max (480ms) of receiving the PS_RDY from the UUT, the UUT transitions to Error Recovery. [PROT_PROC_PSSOURCEONTIMER_1]
3. The test which contains this sequence ends at this point, by simulating a tester end cable detach.

14.4.2.10 TDB 2.2.6 PROT-PROC-PING Ping from Tester

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To check that the timing of any Ping sent by the UUT is appropriate.
Critical for Safety	No

Applies to	DRP, Consumer/Provider, Provider/Consumer, Provider, Consumer
Description	This section describes the procedure to test Pings sent by a UUT The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.5.3.1#2, 6.3.5.1#1, 6.2.1.4#2, plus assertions in checks: PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	
Checklist References	

Test Procedure

Assuming that a Ping has been received from the UUT:

1. Check that the UUT is acting as a Source at the time. [PROT_PROC_PING_1]
2. Check that at least tSourceActivity min (40ms) has elapsed since the previous message on the bus, and that no more than tSourceActivity min (50ms) has elapsed since the previous message on the bus. [PROT_PROC_PING_2]

14.4.2.11 TDB 2.2.7.1 PROT-PROC-REQ-TSTR Tester Originated Request

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Request message is sent by the Tester.
Critical for Safety	No
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider
Description	This section describes the procedure which starts with a Tester originated Request message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.3#1, 6.3.3#6, 6.3.4#1, 6.3.6#1, 6.5.2#5, 6.5.3.1#1, 6.5.3.1#2, 6.5.3.1#3, 6.5.6.1#2, 7.1.4#4, 7.1.4#5, 7.1.5#2, 7.1.5#4, 7.3.2#2, 7.3.2#3, 7.3.6#3, plus assertions in checks: PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	tReceiverResponse , tSourceActivity, tPSTransition
Checklist References	

14.4.2.11.1 Test Procedure

During any test which refers to this section, follow this procedure. If this is a test requiring Vbus voltage transition measurement, perform the appropriate measurements specified below at the same time:

1. Send a Request for the Power Data Object in question at a specified power not exceeding that offered.
2. Check that an Accept message is received from UUT within tReceiverResponse max (15ms) of the last bit of the Request message. [PROT_PROC_REQ_TSTR_1].
3. If Reject or Wait is received from the UUT instead of the Accept, check that it is received within tReceiverResponse max (15ms) of the last bit of the Request message. Retry the Request from step 1, three times and then abandon the test as a failure. [PROT_PROC_REQ_TSTR_2]

    a. If the transition involves a current decrease, decrease it to the new value within tSinkTransition min (20ms) of the last bit of the GoodCRC we sent in response to the Accept message we received.
    b. If the transition involves a voltage change, decrease the current drawn by the Tester to less than pSnkStdby/ Vbus mA within tSinkTransition min (20ms) of the last bit of the GoodCRC we sent in response to the Accept message we received.
4. Check that the last bit of a PS_RDY message is received from UUT by tPSTransition min (450ms) from the receipt of the last bit of the Accept message. [PROT_PROC_REQ_TSTR_3]
5. Voltage Measurement Checks for a Rise in Voltage:
    a. Check that from the end of the GoodCRC we sent in response to the Accept till the voltage leaves its initially valid range was not less than tSrcTransition min (25ms). [PROT_PROC_REQ_TSTR_4]
    b. Check that the voltage was within its target range of nominal voltage ±5%, by tSrcSettlePos from time voltage started to rise, and remained in range for the next 80ms from that time. [PROT_PROC_REQ_TSTR_5]
    c. Check that the slew rate was not greater than 30mV/µs. [PROT_PROC_REQ_TSTR_6]
    d. Check that Vbus does not exceed nominal + 10% of the target voltage during the tSrcSettlePos period from time voltage started to rise. [PROT_PROC_REQ_TSTR_7]
    e. Check that once Vbus has crossed nominal – 20% of the target voltage, it does not fall below this value again during the tSrcSettlePos period from time voltage started to rise. [PROT_PROC_REQ_TSTR_8]
    f. Check that PS_RDY was not received from the UUT before the voltage was within its target range. [PROT_PROC_REQ_TSTR_9]
    g. Check that the last bit of a PS_RDY message is received from UUT by tPSTransition min (450ms) from the end of the Accept message. [PROT_PROC_REQ_TSTR_10]
6. Voltage Measurement Checks for a Fall in Voltage:
    a. Check that from the end of the GoodCRC we sent in response to the Accept till the voltage leaves its initially valid range was not less than tSrcTransition min (25ms). [PROT_PROC_REQ_TSTR_11]
    b. Check that the voltage was within its target range of nominal voltage ±5%, by tSrcSettleNeg from time voltage started to fall, and remained in range for the next 80ms from that time. [PROT_PROC_REQ_TSTR_12]
    c. Check that the slew rate was not greater than 30mV/µs. [PROT_PROC_REQ_TSTR_13]
    d. Check that Vbus does not go lower than nominal - 10% of the target voltage during the tSrcSettlePos period from time voltage started to fall. [PROT_PROC_REQ_TSTR_14]
    e. Check that once Vbus has crossed nominal +20% of the target voltage, it does not rise above this value again during the tSrcSettlePos period from time voltage started to fall. [PROT_PROC_REQ_TSTR_15]

f. Check that PS_RDY was not received from the UUT before the voltage was within its target range. [PROT_PROC_REQ_TSTR_16]
g. Check that the last bit of a PS_RDY message is received from UUT by tPSTransition min (450ms) from the end of the Accept message. [PROT_PROC_REQ_TSTR_17]

14.4.2.12 TDB 2.2.7.2 PROT-PROC-REQ-UUT UUT Originated Request

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Request message is sent by the UUT.
Critical for Safety	No
Applies to	DRP, Consumer, Provider/Consumer, Consumer/Provider
Description	This section describes the procedure which starts with a UUT originated Request message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.4.1#5, 6.4.1.2#7, 6.4.2#1, 6.5.3.1#2, 6.5.3.1#3, 7.2.3#2, 7.3.2#4, 7.3.3#4, 7.3.4#4, 7.3.5#4, 7.3.6#5, 7.3.7#4, plus assertions in checks: PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	tSourceActivity,
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. Check that a Request message is sent by the UUT. Check that the details of this Request are valid, and as expected. [PROT_PROC_REQ_UUT_1]
2. Send an Accept message after slightly less than tReceiverResponse min (15-1=14ms) from the last bit of the GoodCRC message sent.
3. For voltage change (with or without current change):
    a. After a total of tSrcTransition min (25 ms), check that current drawn by the UUT does not exceed pSnkStdby max / Vbus (150 mW / Vbus) mA. [PROT_PROC_REQ_UUT_2]

b. Wait a nominal tSrcTransition (30 ms) from the GoodCRC message, and then change Vbus voltage requested to the new value and/or be prepared to supply more or less current within tSrcTransition max (35ms) plus tSrcReady max (285ms) as appropriate (total 315ms).

c. As soon as the voltage on Vbus has stopped changing, check that current drawn by the UUT does not exceed pSnkStdby max / Vbus (150 mW / Vbus) mA. [PROT_PROC_REQ_UUT_3]

d. The Protocol Tester sends a PS_RDY message to the UUT, and checks for receipt of a GoodCRC message. [PROT_PROC_REQ_UUT_4]

e. The Protocol Tester checks that the current drawn by the UUT is not in excess of the level specified in the current PDO over the next 5 seconds. [PROT_PROC_REQ_UUT_5]

f. Over the same 5 seconds, if the test in question requires it, the Tester sends a Ping message every tSourceActivity max (50ms) and checks for receipt of a GoodCRC message. [PROT_PROC_REQ_UUT_6]

4. For current change only:

    a. Wait a nominal tSrcTransition (30 ms) from the GoodCRC message, and then be prepared to supply more or less current as appropriate, within tSrcTransition max (35ms) plus tSrcReady max (285ms) (total 315ms).

    b. After this 315ms, check that the current drawn from Vbus does not exceed the previously contracted current [PROT_PROC_REQ_UUT_7]

    c. The Protocol Tester sends a PS_RDY message to the UUT, and checks for receipt of a GoodCRC message. [PROT_PROC_REQ_UUT_8]

    d. The Protocol Tester checks that the current drawn by the UUT is not in excess of the level specified in the current PDO over the next 5 seconds. [PROT_PROC_REQ_UUT_9]

    e. Over the same 5 seconds, if the test in question requires it, the Tester sends a Ping message every tSourceActivity max (50ms) and checks for receipt of a GoodCRC message. [PROT_PROC_REQ_UUT_10]

14.4.2.13 TDB 2.2.8.1 PROT-PROC-SRCCAPS-TSTR Tester Originated Source Capabilities

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Source Capabilities message is sent by the Tester. The assumption is that this has occurred while the Tester is acting as a Source.
Critical for Safety	No
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a Tester originated Source Capabilities message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester sends a Source Capabilities message containing the pre-determined information required.
2. If the UUT is acting as a Sink, now continue to the procedure PROT-PROC-REQ-UUT, ensuring that the Request message is received by the Tester within tReceiverResponse max (15ms), from the last bit of the GoodCRC message.

14.4.2.14 TDB 2.2.8.2 PROT-PROC-SRCCAPS-UUT UUT Originated Source Capabilities

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Source Capabilities message is sent by the UUT. The assumption is that this has occurred while the Tester is acting as a Sink.
Critical for Safety	No
Applies to	DRP, Provider, Provider/Consumer or Consumer/Provider
Description	This section describes the procedure which starts with a Tester originated Source Capabilities message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.4.1#1, 6.4.1#2, 6.4.1#3, 6.4.1.2#1, 6.4.1.2#2, 6.4.1.2#3, plus assertions in checks: PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-CTRL
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester receives a Source Capabilities message.
2. If the UUT is acting as a Source, now continue to the procedure PROT-PROC-REQ-TSTR, sending the Request message tReceiverResponse max (15ms) from the last bit of the GoodCRC message received.

14.4.2.15 TDB 2.2.9.1 PROT-PROC-GETSRCCAPS-TSTR Tester Originated Get_Source_Cap

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Get_Source_Cap message is sent by the Tester.
Critical for Safety	No
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a Tester originated Get_Source_Cap message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.7#1, 6.3.7#2, plus assertions in checks: PROT-MSG-CTRL PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-DATA-SRC-CAP
Parameters Tested	tBusIdle, tTransmit, tSenderResponse tReceiverResponse
Checklist References	

14.4.2.15.1 Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester sends a Get_Source_Cap message to the UUT.
2. Check that for a Provider, Provider/Consumer, or Consumer/Provider UUT, a Source Capabilities message is received by the Tester within tReceiverResponse max (15ms), from the last bit of the GoodCRC message. [PROT_PROC_GETSRCCAPS_TSTR_1]
3. Check that this message meets all the requirements detailed in PROT-MSG-DATA-SRC-CAP. [PROT_PROC_GETSRCCAPS_TSTR_2]
4. Check that for a Consumer UUT, a Reject message is received by the Tester within tReceiverResponse max (15ms) from the last bit of the GoodCRC message. [PROT_PROC_GETSRCCAPS_TSTR_3]
5. Check that this message meets all the requirements detailed in PROT-MSG-CTRL. [PROT_PROC_GETSRCCAPS_TSTR_4]

6. If the Tester is acting as a Sink, now continue to the procedure PROT-PROC-REQ-TSTR, ensuring that the Request is sent within tReceiverResponse max (15ms), from the last bit of the GoodCRC message.

14.4.2.16 TDB 2.2.9.2 PROT-PROC-GETSRCCAPS-UUT UUT Originated Get_Source_Cap

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Get_Source_Cap message is sent by the UUT.
Critical for Safety	No
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a UUT originated Get_Source_Cap message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.8#1, 6.3.8#2, plus assertions in checks: PROT-MSG-CTRL PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-DATA-SRC-CAP
Parameters Tested	tBusIdle, tTransmit, tSenderResponse
Checklist References	

14.4.2.16.1 Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester receives a Get_Source_Cap message from the UUT.
2. If the tester is emulating a Provider, Provider/Consumer, or Consumer/Provider, send a valid Source Capabilities message to the UUT after tReceiverResponse max (15ms), from the last bit of the GoodCRC message.
3. If the tester is emulating a Consumer, send a valid Reject message to the UUT after tSenderResponse max (30ms), from the last bit of the GoodCRC message.

4. If the UUT is acting as a Sink, now continue to the procedure PROT-PROC-REQ-UUT, ensuring that the Request message is received by the Tester within tReceiverResponse max (15ms) of the last bit of the GoodCRC message.

14.4.2.17 TDB 2.2.10.1 PROT-PROC-GETSNKCAPS-TSTR Tester Originated Get_Sink_Cap

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Get_Sink_Cap message is sent by the Tester.
Critical for Safety	No
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a Tester originated Get_Sink_Cap message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.8#1, 6.3.8#2, plus assertions in checks: PROT-MSG-CTRL PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-DATA-SNK-CAP
Parameters Tested	tBusIdle, tTransmit, tSenderResponse
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester sends a Get_Sink_Cap message to the UUT.
2. Check that for a Consumer, Consumer/Provider, or Provider/Consumer UUT, a Sink Capabilities message is received by the Tester within tReceiverResponse max (15ms) of the last bit of the GoodCRC message. [PROT_PROC_GETSNKCAPS_TSTR_1]
3. Check that this message meets all the requirements detailed in PROT-MSG-DATA-SNK-CAP. [PROT_PROC_GETSNKCAPS_TSTR_2]

4. Check that for a Provider UUT, a Reject message is received by the Tester within tReceiverResponse max (15ms) of the last bit of the GoodCRC message. [PROT_PROC_GETSNKCAPS_TSTR_3]
5. Check that this message meets all the requirements detailed in PROT-MSG-CTRL. [PROT_PROC_GETSNKCAPS_TSTR_4]

14.4.2.18 TDB 2.2.10.2 PROT-PROC-GETSNKCAPS-UUT UUT Originated Get_Sink_Cap

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Get_Sink_Cap message is sent by the UUT.
Critical for Safety	No
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a UUT originated Get_Sink_Cap message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.8#1, 6.3.8#2, plus assertions in checks: PROT-MSG-CTRL PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-DATA-SRC-CAP
Parameters Tested	tBusIdle, tTransmit, tSenderResponse tReceiverResponse
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester receives a Get_Sink_Cap message from the UUT.
2. Check that this message meets all the Control Message Checks detailed in PROT-MSG-CTRL. [PROT_PROC_GETSNKCAPS_UUT_1]

3. If the tester is emulating a Consumer, Consumer/Provider, or Provider/Consumer, send a valid Sink Capabilities message to the UUT after ~~tSenderResponse max (30ms)~~ tReceiverResponse max (15ms), from the last bit of the GoodCRC message.
4. If the tester is emulating a Provider, send a valid Reject message to the UUT after tReceiverResponse max (15ms), from the last bit of the GoodCRC message.

14.4.2.19 TDB 2.2.11.1 PROT-PROC-GOTOMIN-TSTR Tester Originated GotoMin

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the GotoMin message is sent by the Tester.
Critical for Safety	No
Applies to	DRP, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a Tester originated GotoMin message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	7.3.11#1, 7.3.11#2, 7.3.11#3, 7.3.11#4, plus assertions in checks: PROT-MSG-CTRL PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-DATA-SNK-CAP
Parameters Tested	tSnkTransition
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester sends a GotoMin message to the UUT.
2. Check that the Sink current is reduced to the Minimum Operating Current specified by the previous UUT Request, within tSrcTransition max (35ms) from the last bit of the GoodCRC message received in response to the GoToMin message. [PROT_PROC_GOTOMIN_TSTR_1]
3. From the last bit of the GoToMin message wait for tSrcTransition min plus tSnkNewPower max (25+15 = 40ms), then send PS_RDY.

14.4.2.20 TDB 2.2.11.2 PROT-PROC-GOTOMIN_UUT UUT Originated GotoMin

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the GotoMin message is sent by the UUT.
Critical for Safety	No
Applies to	DRP, Provider, Provider/Consumer, Consumer/Provider
Description	This section describes the procedure which starts with a UUT originated GotoMin message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	7.3.11#1, 7.3.11#2, 7.3.11#3, 7.3.11#4, plus assertions in checks: PROT-MSG-CTRL PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-DATA-SNK-CAP
Parameters Tested	tSnkTransition, tSrcNewPower,
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester receives a GotoMin message from the UUT.
2. Check that the UUT is not behaving as a Sink. [PROT_PROC_GOTOMIN_UUT_2]
3. The Tester ensures that Sink current it is drawing is reduced to the Minimum Operating Current specified by the previous Request within tSrcTransition max (35ms) from the last bit of the GoToMin message.
4. Check that a PS_RDY message is received by the Tester within tSrcTransition min plus tSnkNewPower max (25+15 = 40ms) from the last bit of the GoodCRC message received in response to the GotoMin message. [PROT_PROC_GOTOMIN_UUT_1]

14.4.2.21 TDB 2.2.12.1 PROT-PROC-SR-TSTR Tester Originated Soft Reset

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Soft Reset message is sent by the Tester.
Critical for Safety	No
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a Tester originated Soft Reset message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.3.3#5, 6.3.3#6, plus assertions in checks: PROT-MSG-CTRL PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT
Parameters Tested	
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester sends a Soft Reset message to the UUT.
2. Check that an Accept message is received by the Tester within tReceiverResponse max (15ms), from the last bit of the GoodCRC message. [PROT_PROC_SR_TSTR_1]
3. Check that this message meets all the requirements detailed in PROT-MSG-CTRL. [PROT_PROC_SR_TSTR_2]
4. If UUT is currently acting as a Source:
    a. Continue to the procedure PROT-PROC-SRCCAPS-UUT ensuring that the Source Capabilities message is received within tReceiverResponse max (15ms), from the last bit of the GoodCRC message. [PROT_PROC_SR_TSTR_3]
5. If UUT is currently acting as a Sink:
    a. Continue to the procedure PROT-PROC-SRCCAPS-TSTR ensuring that the Source Capabilities message is sent at a time slightly less than tReceiverResponse max (15ms), from the last bit of the GoodCRC message. [PROT_PROC_SR_TSTR_4]

14.4.2.22 TDB 2.2.12.2 PROT-PROC-SR-UUT UUT Originated Soft Reset

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Soft Reset message is sent by the UUT.
Critical for Safety	No
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a UUT originated Soft Reset message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	PROT-MSG-CTRL PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT
Parameters Tested	
Checklist References	

14.4.2.22.1 Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester receives a Soft Reset message from the UUT.
2. Check that the UUT is not a Cable. [PROT_PROC_SR_UUT_4]
3. Check that this message meets all the Control Message Checks detailed in PROT-MSG-CTRL. [PROT_PROC_SR_UUT_1]
4. The Tester sends an Accept message to the UUT after tReceiverResponse max (15ms) from the last bit of the GoodCRC message received.
5. If UUT is currently acting as a Source:
    a. Continue to the procedure PROT-PROC-SRCCAPS-UUT ensuring that the Source Capabilities message is received within tReceiverResponse max (15ms), from the last bit of the GoodCRC message. [PROT_PROC_SR_TSTR_2]
6. If UUT is currently acting as a Sink:
    a. Continue to the procedure PROT-PROC-SRCCAPS-TSTR ensuring that the Source Capabilities message is sent at a time slightly less than tReceiverResponse max (15ms), from the last bit of the GoodCRC message. [PROT_PROC_SR_TSTR_3]

14.4.2.23 TDB 2.2.13.1 PROT-PROC-HR-TSTR Tester Originated Hard Reset

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Hard Reset signal is sent by the Tester.
Critical for Safety	No
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a Tester originated Hard Reset message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages and Vbus voltage involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.5.4.3#1, 6.5.10.2#1, 7.1.6#1, 7.1.6#2, 7.1.6#4, 7.1.6#5, 7.3.12#5, 7.3.12#6, plus assertions in checks.
Parameters Tested	
Checklist References	

Test Procedure

1. If UUT is behaving as Source:
   a. The Tester sends a Hard Reset signal.
   b. Check Vbus stays within present valid voltage range for tPSHardReset min (25ms) after last bit of Hard Reset signal. [PROT_PROC_HR_TSTR_1]
   c. Check that Vbus starts to fall below present valid voltage range by tPSHardReset max(35ms). [PROT_PROC_HR_TSTR_2]
   d. Check that Vbus reaches vSafe0V within tSafe0v max (650 ms). [PROT_PROC_HR_TSTR_3]
   e. Check that Vbus starts rising to vSafe5V after a delay of tSrcRecover (0.66s - 1s) from reaching vSafe0V. [PROT_PROC_HR_TSTR_4]
   f. Check that Vbus reaches vSafe5V within tSrcTurnOn max (275ms) of rising above vSafe0v max (0.8V). [PROT_PROC_HR_TSTR_5]
   g. Check that Source Capabilities are finished sending within tFirstSourceCap max (250ms) of Vbus reaching vSafe5v min. [PROT_PROC_HR_TSTR_6]
2. If UUT is behaving as Sink:

a. The Tester sends a Hard Reset signal.
b. Keep Vbus within present valid voltage range for tPSHardReset nom (30ms) after last bit of Hard Reset signal.
c. Take Vbus to vSafe0V within tSafe0v max (650 ms).
d. Keep Vbus at vSafe0V for tSrcRecover (0.66s - 1s).
e. Take Vbus to vSafe5V within tSrcTurnOn max (275ms) of rising above vSafe0v max (0.8V).
f. Send Source Capabilities within tFirstSourceCap max (250ms) of Vbus reaching vSafe5v min.

14.4.2.24 TDB 2.2.13.2 PROT-PROC-HR-UUT UUT Originated Hard Reset

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the Hard Reset signal is sent by the UUT.
Critical for Safety	No
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a UUT originated Hard Reset message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages and Vbus voltage involved is checked.
Test setup	Depends on test referring to this section.
Preconditions	
Assertions Tested	6.5.4.3#1, 6.5.10.2#1, 7.1.6#1, 7.1.6#2, 7.1.6#4, 7.1.6#5, 7.3.12#5, 7.3.12#6, plus assertions in checks.
Parameters Tested	
Checklist References	

Test Procedure

1. If UUT is behaving as source
    a. The UUT receives a Hard Reset signal from the UUT.
    b. Check that the UUT is not a Cable. [PROT_PROC_HR_UUT_1]
    c. Check Vbus stays within present valid voltage range for tPSHardReset min (25ms) after last bit of Hard Reset signal. [PROT_PROC_HR_UUT_2]

d. Check that Vbus starts to fall below present valid voltage range by tPSHardReset max(35ms). [PROT_PROC_HR_UUT_3]

e. Check that Vbus reaches vSafe0V within tSafe0v max (650 ms). [PROT_PROC_HR_UUT_4]

f. Check that Vbus starts rising to vSafe5V after a delay of tSrcRecover (0.66s - 1s) from reaching vSafe0V. [PROT_PROC_HR_UUT_5]

g. Check that Vbus reaches vSafe5V within tSrcTurnOn max (275ms) of rising above vSafe0v max (0.8V). [PROT_PROC_HR_UUT_6]

h. Check that Source Capabilities are finished sending within tFirstSourceCap max (250ms) of Vbus reaching vSafe5v min. [PROT_PROC_HR_UUT_7]

2. If UUT is behaving as Sink:

   a. The UUT receives a Hard Reset signal from the UUT.

   b. Keep Vbus within present valid voltage range for tPSHardReset nom (30ms) after last bit of Hard Reset signal.

   c. Take Vbus to vSafe0V within tSafe0v max (650 ms).

   d. Keep Vbus at vSafe0V for tSrcRecover (0.66s - 1s).

   e. Take Vbus to vSafe5V within tSrcTurnOn max (275ms) of rising above vSafe0v max (0.8V).

   f. Send Source Capabilities within tFirstSourceCap max (250ms) of Vbus reaching vSafe5v min.

14.4.2.25 TDB 2.2.14 PROT-PROC-BIST-TSTR Tester Originated BIST

Status	Secondary Checks performed during any Primary Test where the specified situation is encountered
Purpose	To perform the appropriate protocol checks relating to any circumstance in which the BIST message is sent by the Tester.
Critical for Safety	No
Applies to	Cable, DRP, Provider, Provider/Consumer, Consumer/Provider or Consumer
Description	This section describes the procedure which starts with a UUT originated BIST message. The checks described are made any time the sequence is encountered during testing. The correct formatting, sequence and timing of the messages involved is checked.
Test setup	Depends on test referring to this section.

Preconditions	
Assertions Tested	6.4.3#7, 6.4.3#10, 6.4.3.6#1, 6.4.3.6#2, 6.4.3.9#1, 6.4.3.9#2, plus assertions in checks: PROT-MSG-CTRL PROT-PROC-GOODCRC-TSTR PROT-PROC-GOODCRC-UUT PROT-MSG-DATA-SNK-CAP
Parameters Tested	tBusIdle, tTransmit, tSenderResponse tReceiverResponse
Checklist References	

Test Procedure

During any test which refers to this section, follow this procedure:

1. The Tester sends a BIST message to the UUT.
2. Check that the requesting operation is performed. [PROT_PROC_BIST_TSTR_1]
   Two commands are relevant:
   - BIST Carrier Mode 2: Check that the pattern starts within tBISTMode max (300ms) and continues for tBISTContMode (40-60ms).
   - BIST Test Data: Check that the UUT does not originate any traffic, before a Hard Reset or detachment.

15 Appendix G:VISA Configuration

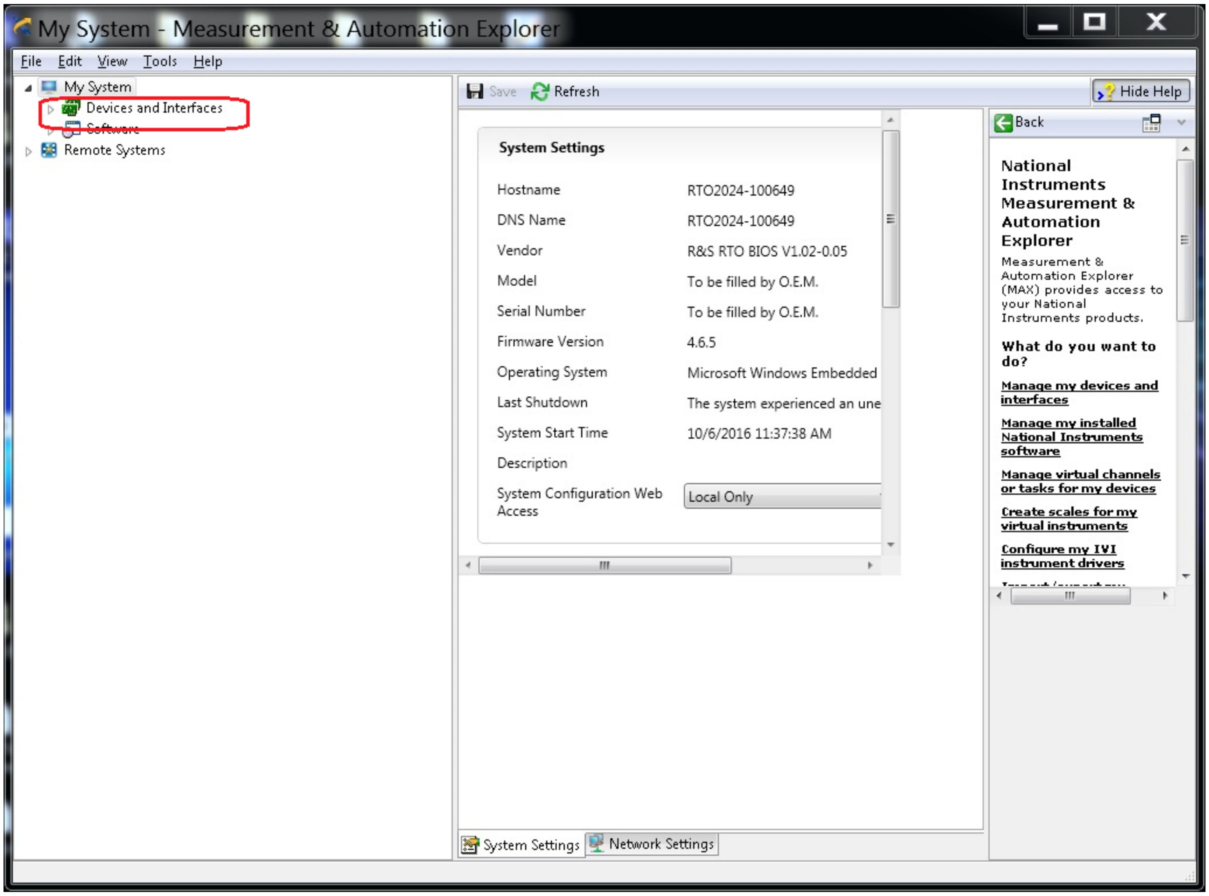
15.1 NI VISA Configuration for Scope and eLoad Detection

NI VISA software is installed on the oscilloscope models that do not have a proprietary VISA software. The NI VISA software can be downloaded from the following link.

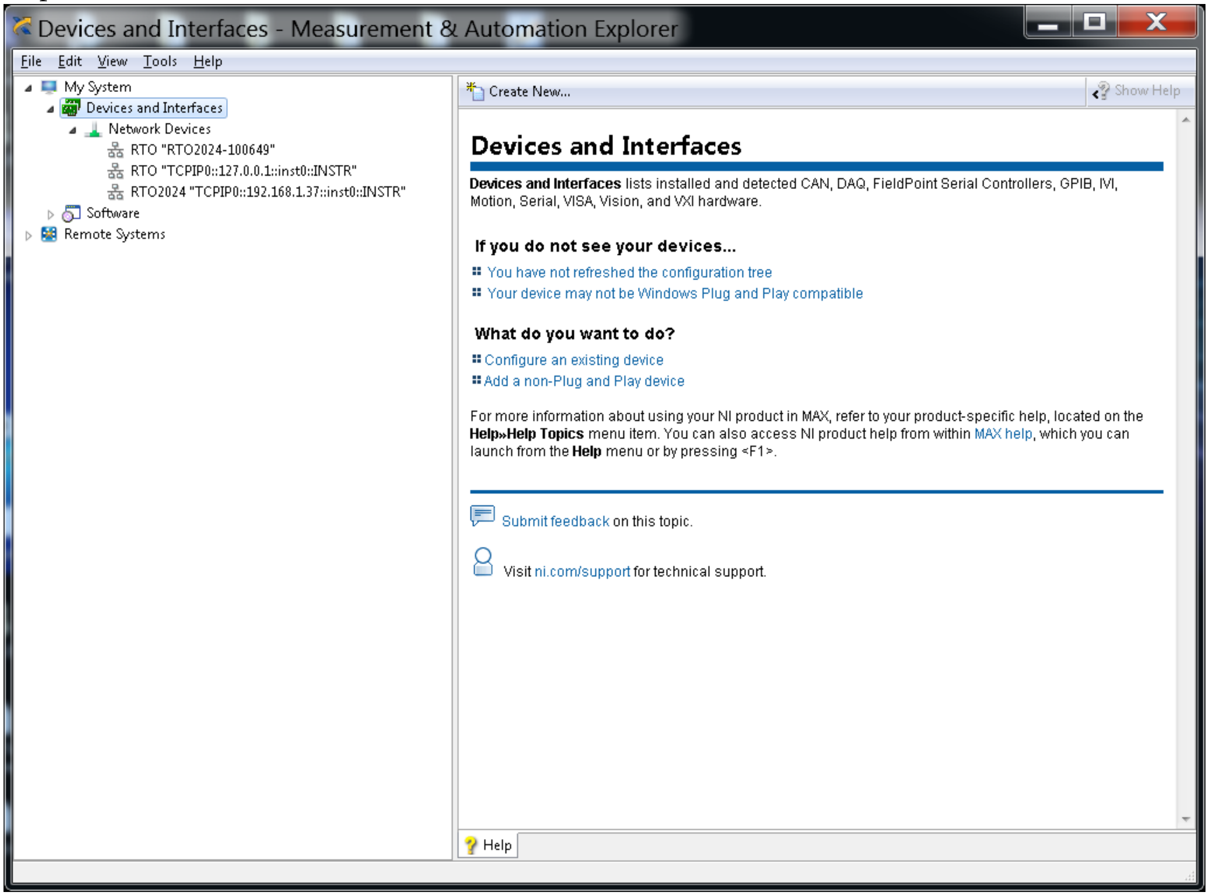
http://ftp.ni.com/support/softlib/visa/NI-VISA/14.0.1/NIVISA1401full.exe.

The following steps are done to enable the GRL application to connect to oscilloscope via NI Max Software.

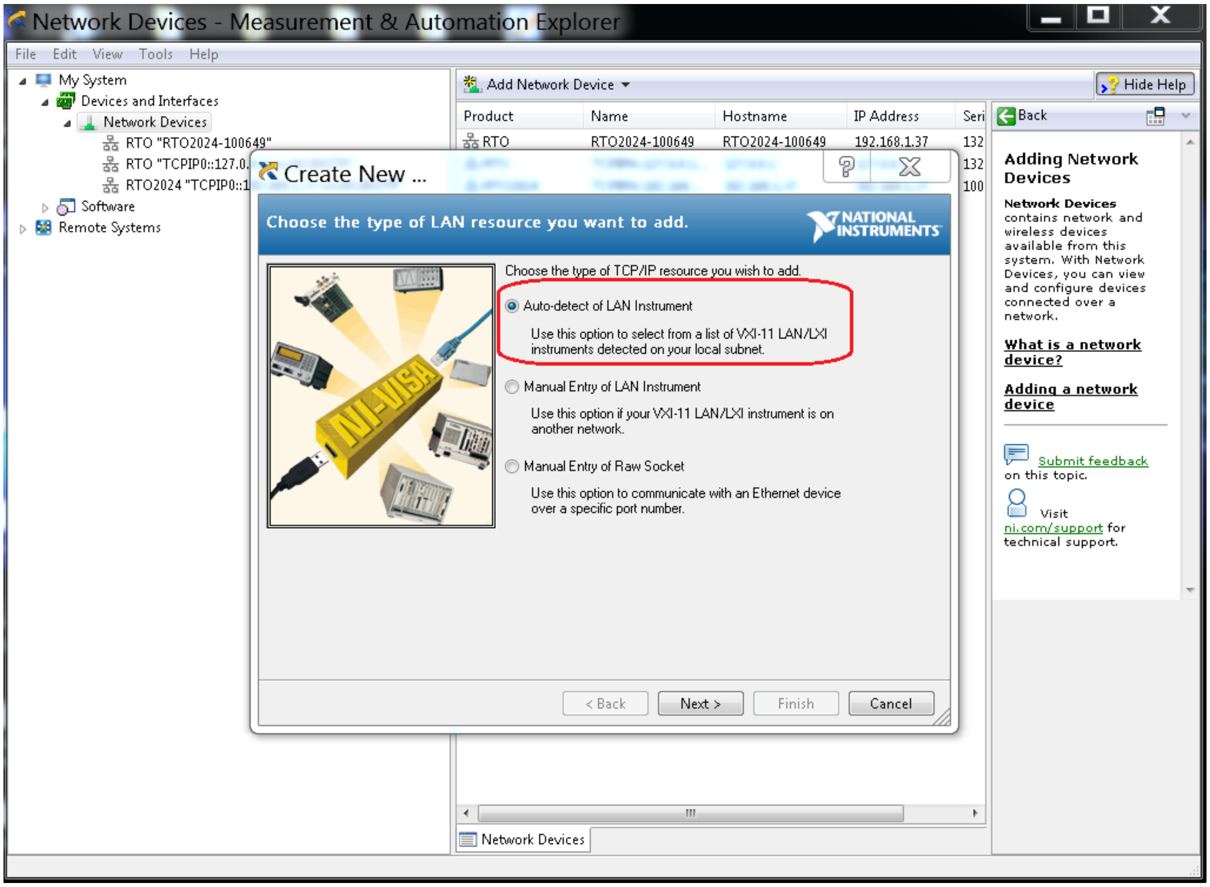
1. Open NI Max Software. The following screen would appear.


My System - Measurement & Automation Explorer
File Edit View Tools Help
My System
Devices and Interfaces
Software
Remote Systems
Save
Refresh
Hide Help
System Settings
Hostname
RTO2024-100649
DNS Name
RTO2024-100649
Vendor
R&S RTO BIOS V1.02-0.05
Model
To be filled by O.E.M.
Serial Number
To be filled by O.E.M.
Firmware Version
4.6.5
Operating System
Microsoft Windows Embedded
Last Shutdown
The system experienced an une
System Start Time
10/6/2016 11:37:38 AM
Description
System Configuration Web Access
Local Only
Back
National Instruments Measurement & Automation Explorer
Measurement & Automation Explorer (MAX) provides access to your National Instruments products.
What do you want to do?
Manage my devices and interfaces
Manage my installed National Instruments software
Manage virtual channels or tasks for my devices
Create scales for my virtual instruments
Configure my IVI instrument drivers
System Settings
Network Settings

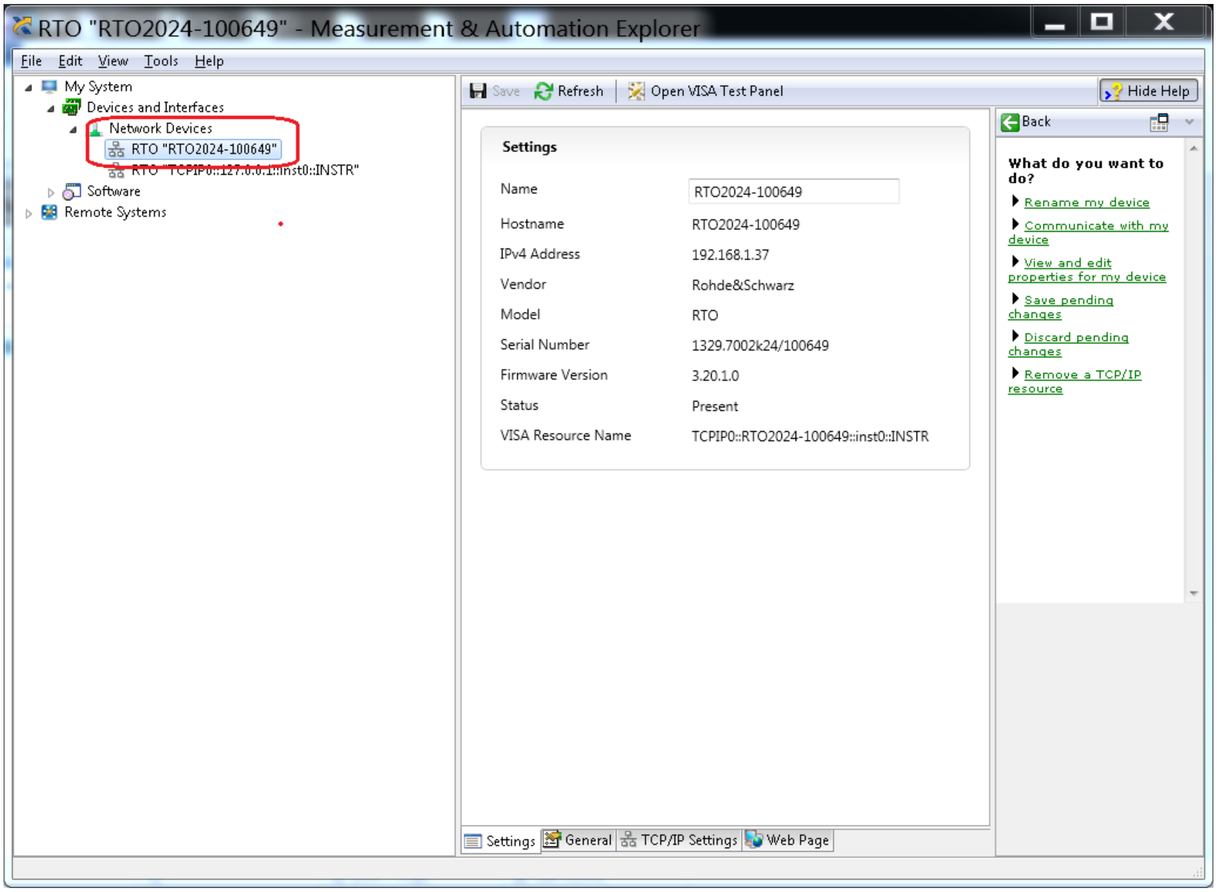
2. Expand Devices and Interfaces.



3. Right click on the Network Devices .Create a new VISA TCPIP resource. As shown in below figure. Check the Auto Detect LAN instrument option and then Select the Next and Finish Button.



4. The Scope Instrument has to be listed in Network and Devices list as shown below.



5. Close and Open the GRL Software and try to connect to oscilloscope as explained in section 4.3

15.2 Tektronix VISA Configuration and eLoad Detection

Steps 1: Download the UsbInstr.dll from below link

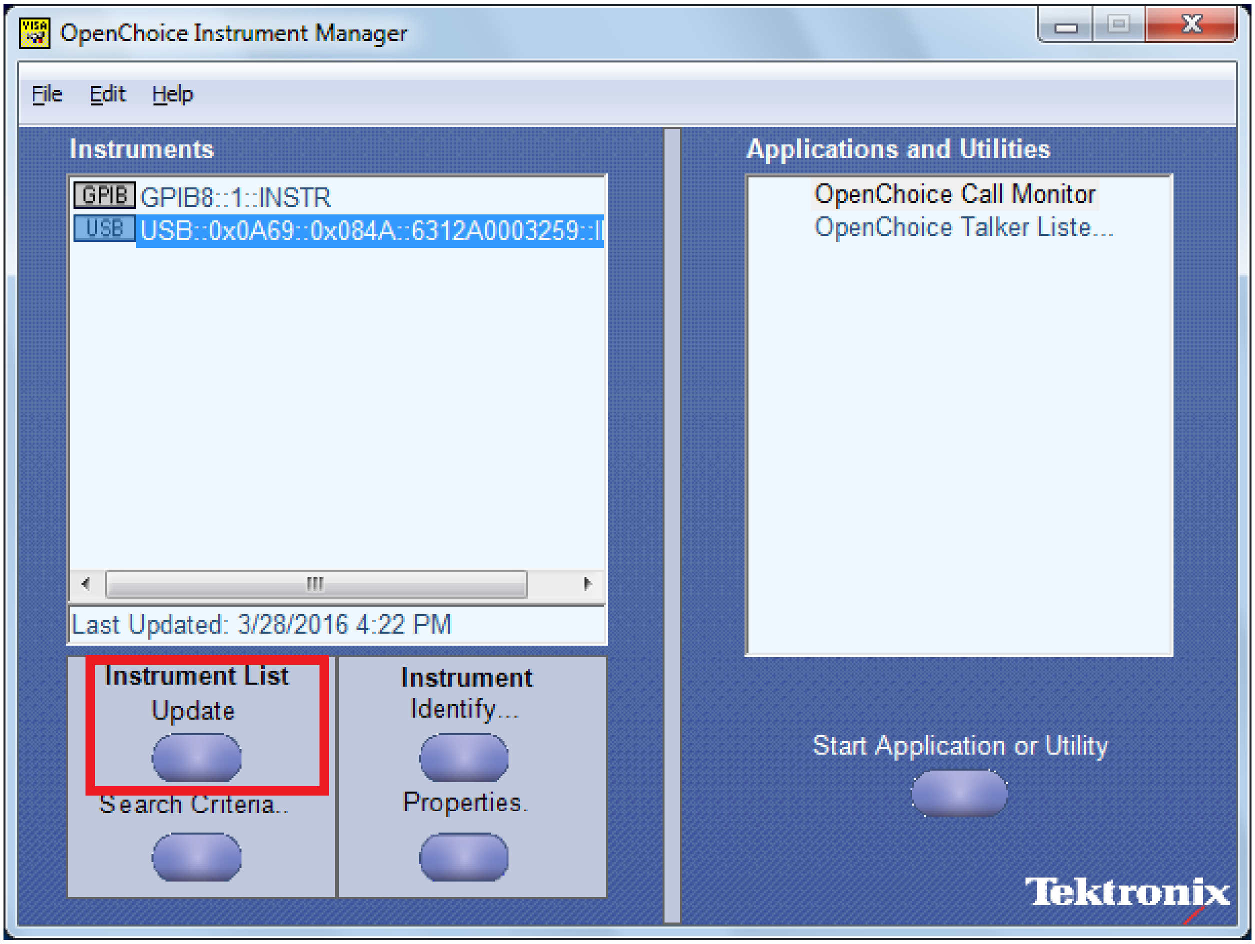
https://app.box.com/s/7a502u1jm2s9mik9ag79wk11duj9eh66

Step2: Replace UsbInstr.dll in TekVISA installation path i.e. (C:\Program Files (x86)\IVI Foundation\VISA\WinNT\TekVISA\Bin\).

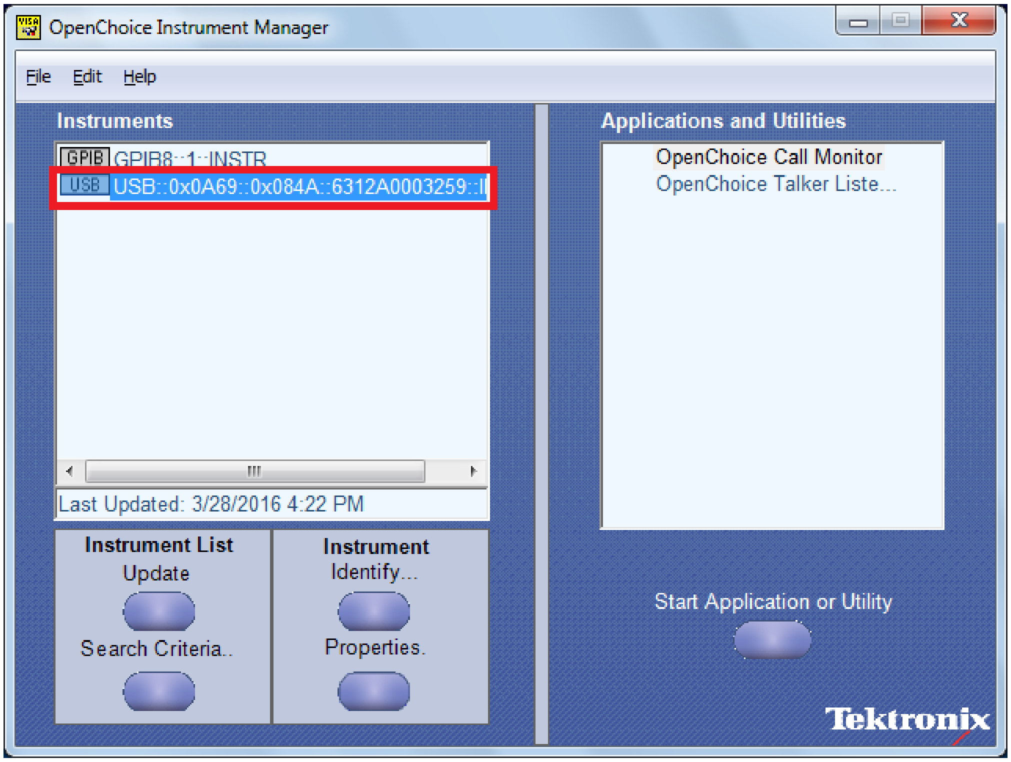
Note:In the case Tektronix VISA location path does not exist, UsbInstr.dll has to be searched and replaced.

Step 3: Open Tektronix VISA Application "Open Choice Instrument Manager"

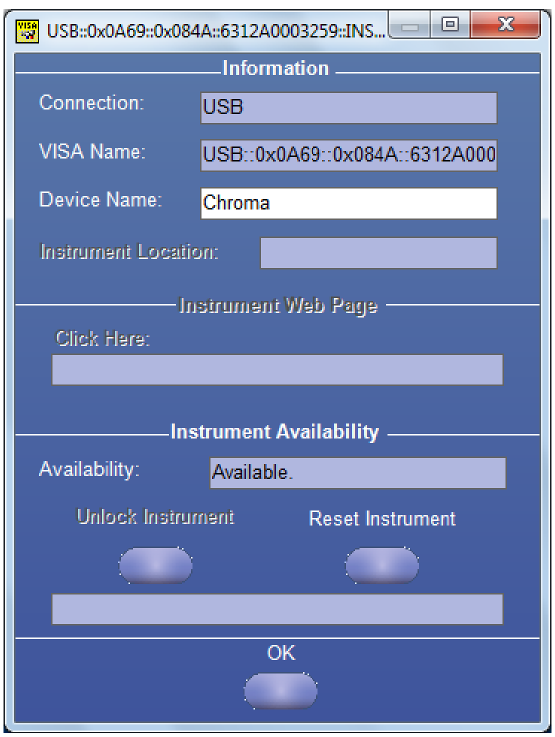
Step 4: Click on Update Instruments list button as shown below



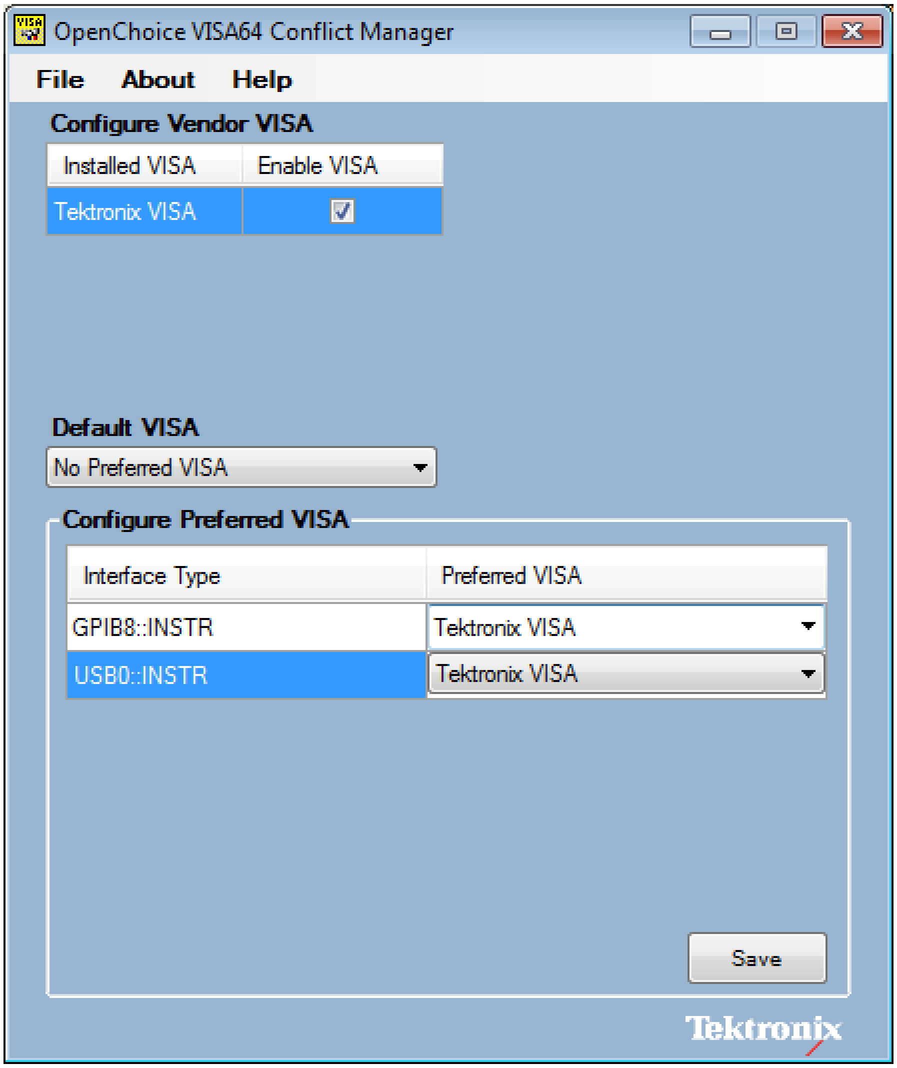
Step 4: Select load VISA Address as shown below



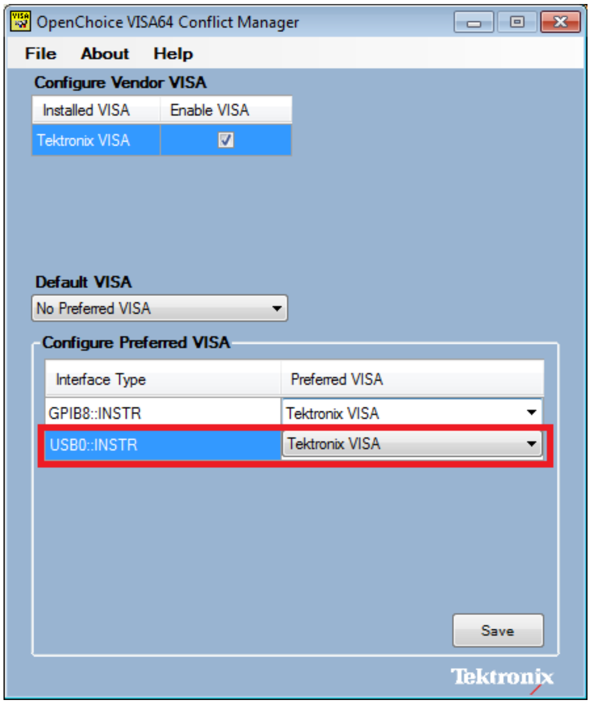
Step 5: Click on Properties button, in the Properties Window change the Device name with respect to eLoad as shown below.



Step 6: Open Tektronix VISA application “Open Choice VISA64 Conflict Manager” as shown below.



Step 7: Make sure that Tektronix VISA option is selected as Preferred VISA option as shown below.



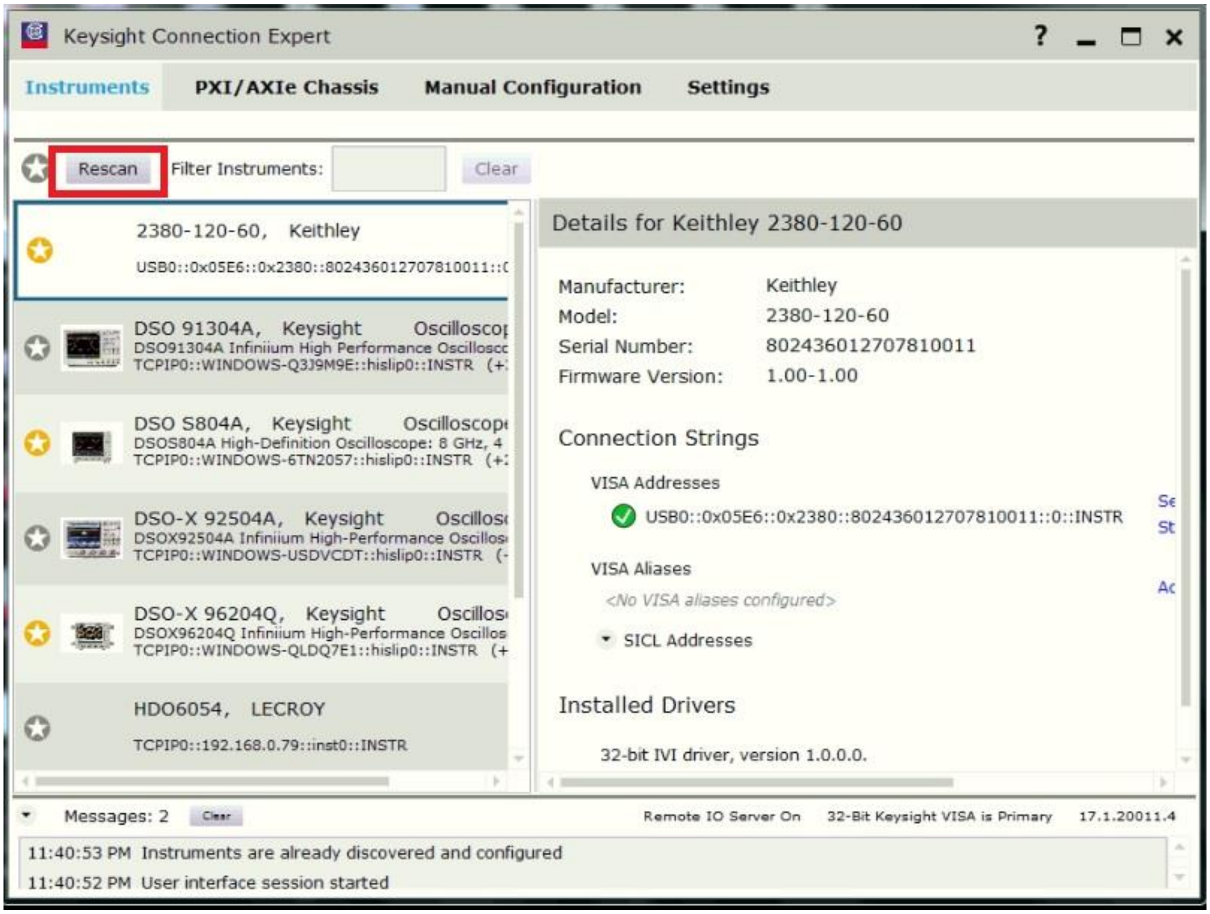
Step 9: Close Tekronix VISA Application and GRL Application.

Step10: Restart GRL Application.

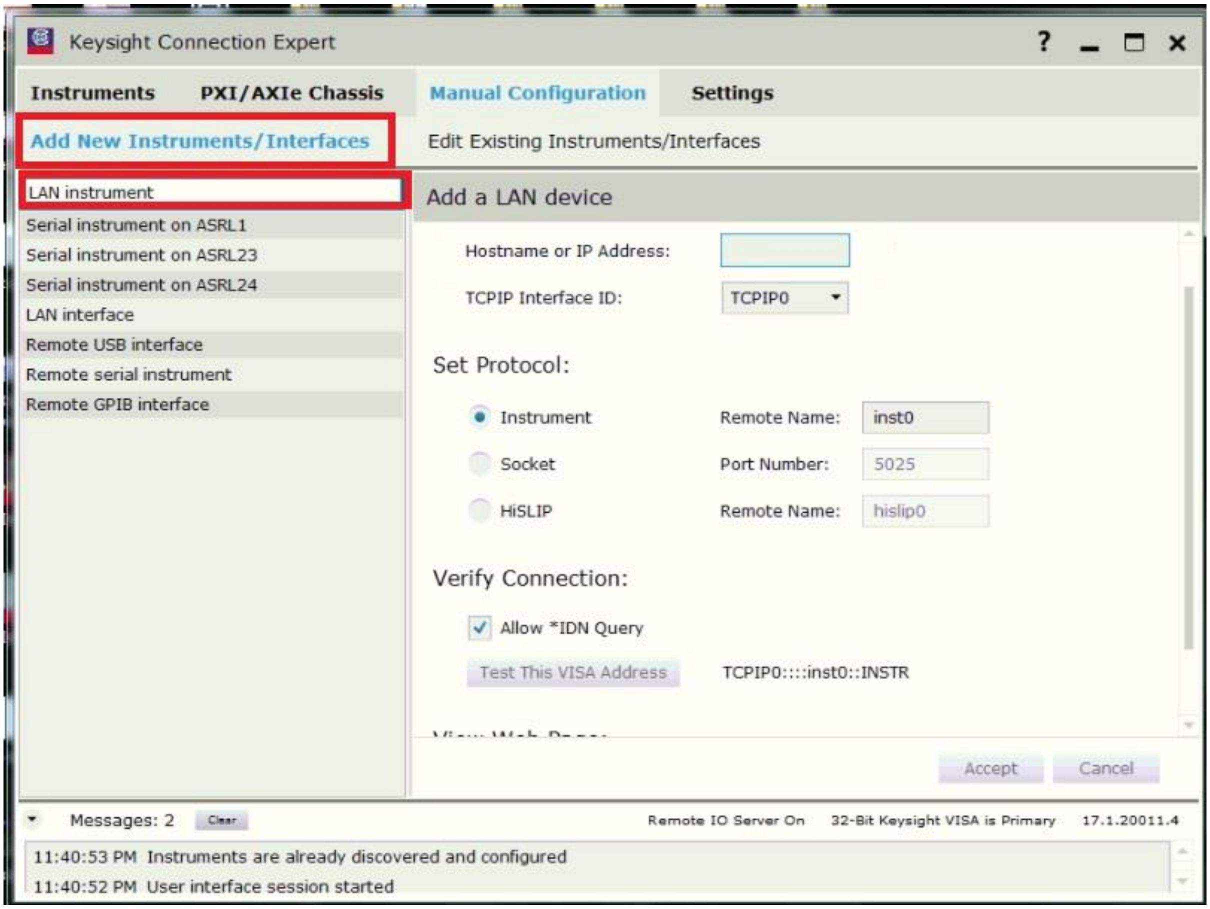
15.3 Agilent IO Setup and eLoad Detection

The following steps are done to complete the Agilent Instrument IO setup.

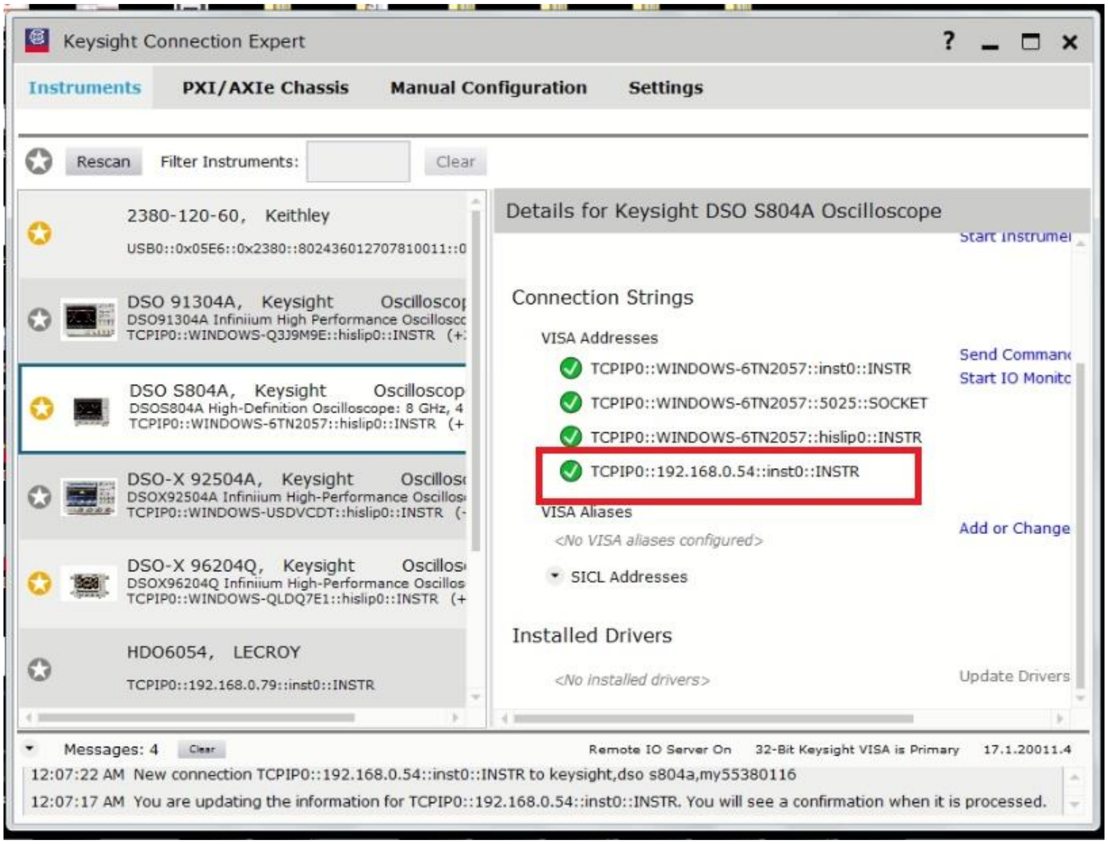
1. Open Key Sight Connection Expert Software(Agilent IO Software)
2. Click on Instruments Tab
3. Click on Rescan Button as shown in following image.



4. VISA layer Instruments are listed as shown in above figure. If they are not getting listed then manual configuration has to be done as mentioned in step 5,6 and 7
5. Click on Manual Configuration Tab
6. Click on Add New Instrument and Select LAN Instrument
7. Update Host IP Address with Scope IP Address.
8. Click on Accept Button. Please refer to the below Image.



9. Select Instruments Tab and make sure the Connect Settings lists the VISA Address as Green Icon as shown below.



END_OF_DOCUMENT