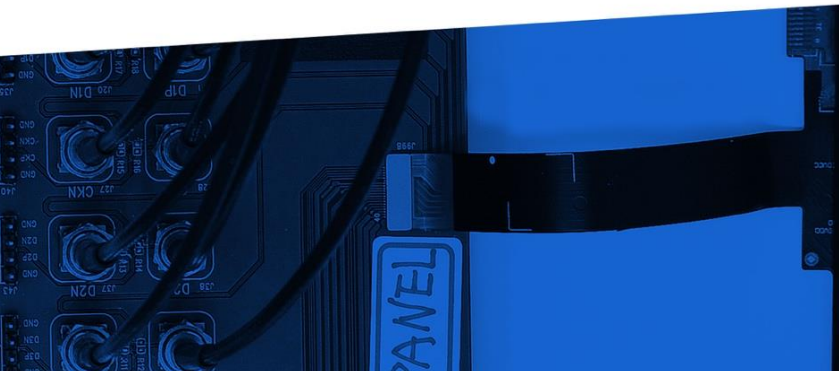
DATA SHEET

SV4E-I3C

I3C Test and Debug Module

E SERIES



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Introduction

OVERVIEW

The SV4E-I3C is an all-inclusive solution for I3C-based device interface development, test, and programming. Containing three instruments in one, this tool can act as a protocol exerciser, a protocol analyzer, and a general purpose I3C device programmer. As an exerciser, it may be used to implement, test and debug both I3C controller and I3C target devices. As a protocol analyzer, it provides timing analysis with 10 ns capture resolution. The optional PurVue Analyzer™ provides a fully-embedded real-time oscilloscope (500 MHz, 12 bit) to the suite of Introspect I3C analysis tools and eliminates the need for external oscilloscope probes. As an I3C device programmer, the deep memory of the SV4E-I3C can support a wide range of device programming requirements. All three categories of instrumentation features are accessible simultaneously and in real-time using award-winning Introspect ESP Software.

KEY FEATURES

- **Device instances:** integrates 4 parallel devices, each with its own independent protocol stack
- **Device roles:** able to configure multiple devices with different roles (main controller, secondary controller, target) with concurrent operation.
- **Analog waveform analysis:** fully integrated real time (500 MHz / 12 bit) oscilloscope on two simultaneous channels (SCL and SDA).
- **Protocol analysis:** easily trigger all analysis functions on CCC's and patterns for private and broadcast communications including IBI and hot-join functions.

KEY BENEFITS

- **Self-Contained:** simultaneous protocol exercising and protocol analysis enables complete characterization, debug, and test environment for individual sensor/controller devices and for entire multi-device systems
- **Flexible:** solution features I3C and I3C Basic protocol support with real-time voltage and timing controls
- **Automated:** scripting capability ideal for debug tasks, verification and full-fledged production screening of devices and system boards

BLOCK DIAGRAM

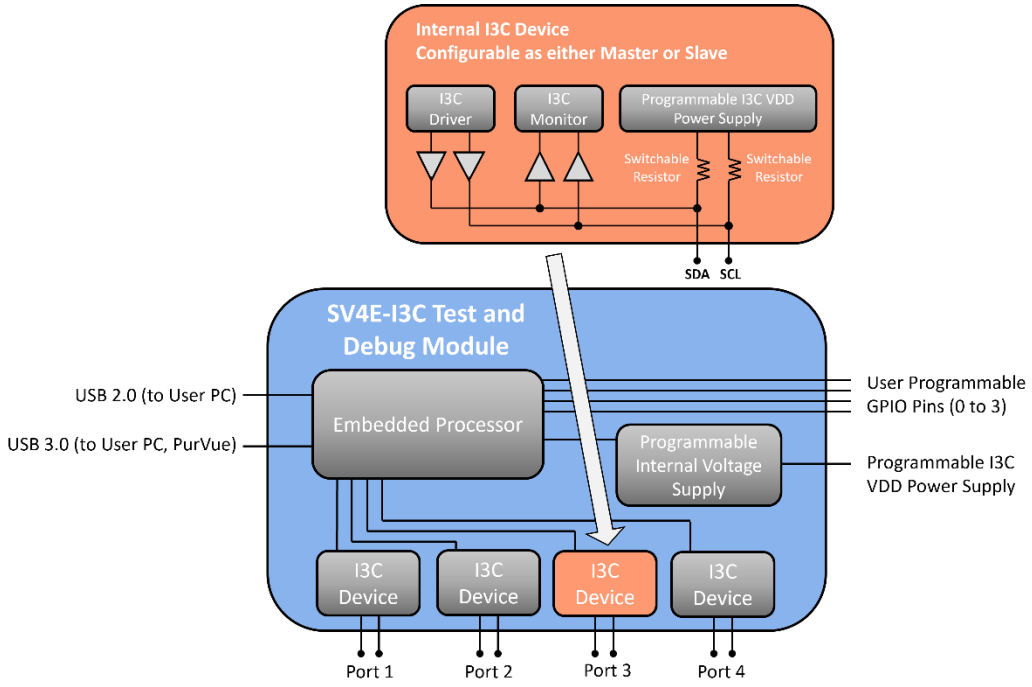


Figure 1: Block diagram of the SV4E-I3C module (blue) and detail of one of four internal I3C devices (orange).

TYPICAL APPLICATION

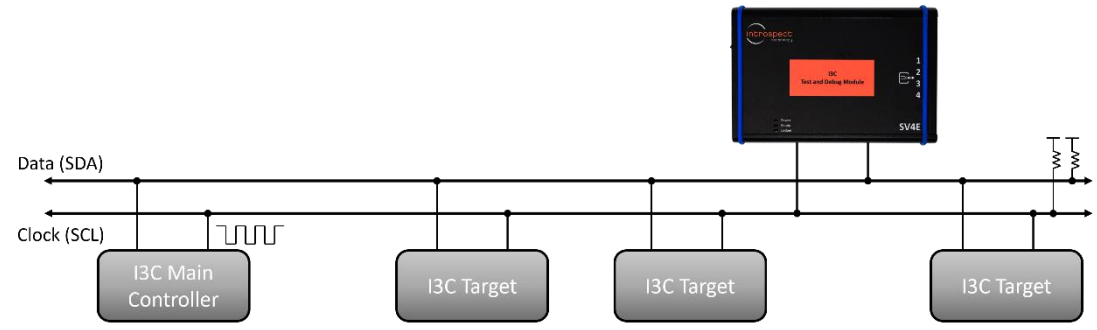


Figure 2: Typical application for an SV4E-I3C Test and Debug Module on an I3C bus.

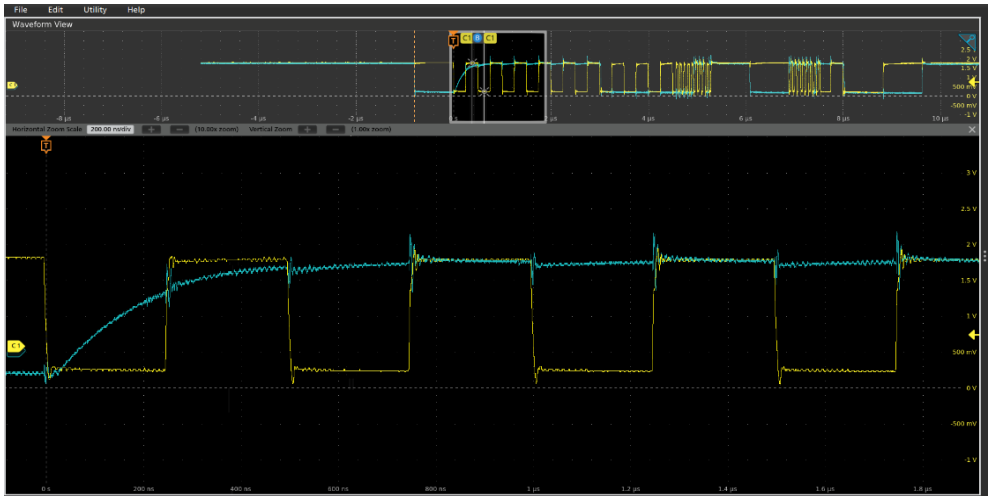
ORDERING INFORMATION

TABLE 1: ITEM NUMBERS FOR THE SV4E-I3C

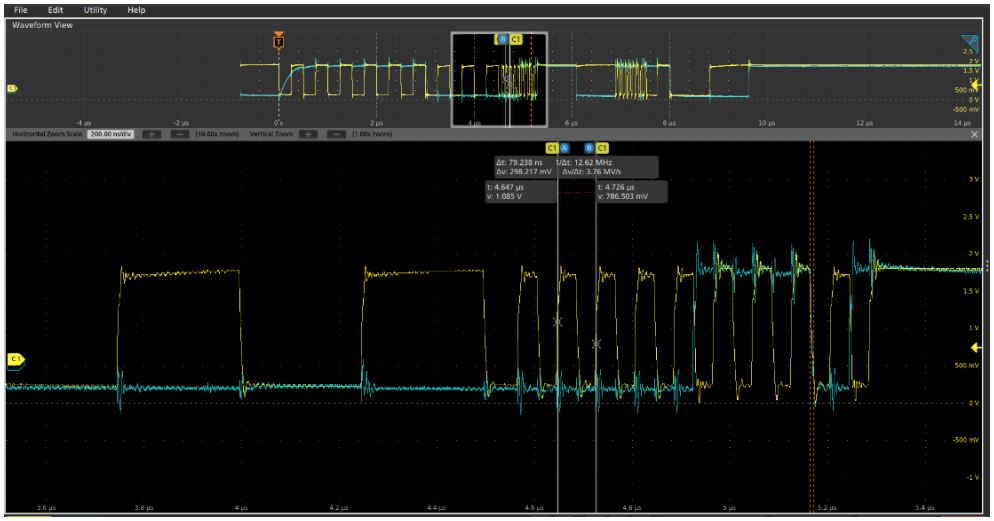
PART NUMBER	NAME	KEY DIFFERENTIATORS
6604	SV4E-I3C Test and Debug Module Standard 2.0 V Interface	Characterization, debug and test of I3C devices for I3C VDD = 0.8 to 2.0 V. Includes PC software license (perpetual) and the standard 2.0 V interface adapter board
6606	PurVue Analyzer™ Integrated Oscilloscope Option	Option to provide PurVue Analyzer™ Protocol-Triggered Real-Time Oscilloscope to SV4E-I3C Test and Debug Module waveform capture capabilities
6608	SV4E-I3C with PurVue Analyzer™	
4845	Low Voltage Adapter for SV4E-I3C	Standard adapter board to support 2.0 V operation
4865	High Voltage Adapter for SV4E-I3C	Adapter board to support 3.6 V operation
5410	I3C Target Device CTS Application	Based on the following CTS specifications: mipi_I3C-v1-1-1_CTS_v1-0 and I3C-Basic-v1-1-1_CTS_v1-0 Contact Introspect for Method of Implementation (MOI) documentation
5418	I3C Controller Device CTS Application	Based on the following CTS specifications: mipi_I3C-v1-1-1_CTS_v1-0 and I3C-Basic-v1-1-1_CTS_v1-0 Contact Introspect for Method of Implementation (MOI) documentation

Feature Overview

TYPICAL I3C OUTPUT WAVEFORMS



(a)



(b)

Figure 3: Typical waveform of SV4E-I3C controller driving a DUT (a) Open Drain Frequency=2 MHz (b) Push-Pull Frequency=12.5 MHz

DETAILED ANALYSIS CAPABILITY

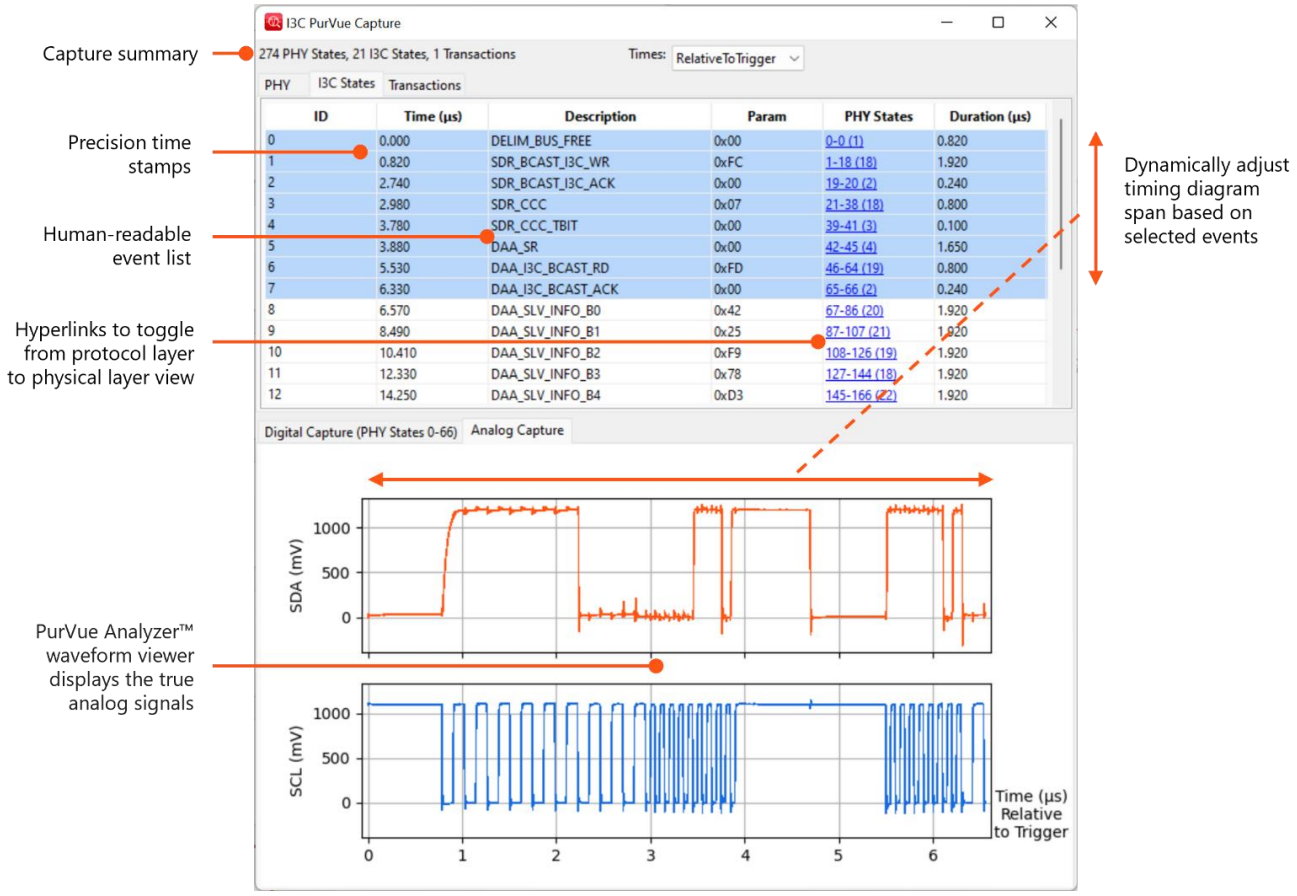


Figure 4: Introspect ESP Software interface for data capture and protocol analysis

Physical Connections

Figure 5 shows the physical connections on the SV4E-I3C module. The four I3C Ports (SCL and SDA) are available via 0.1″ female header connections. A programmable power supply for VDD of the I3C bus and four programmable general purpose I/Os are each available via separate 0.1″ male header connectors. Please see the following section for a detailed description of each of the header pinouts.

The SV4E-I3C has a USB port that allows the SV4E to communicate directly with a PC through USB cable connections on the left side of the module. Power is provided to the SV4E-I3C module with a 12 V DC supply through a barrel connector. The recommended DC power supply, included with the SV4E-I3C module, is produced by CUI Incorporated, Part # CUI SDI65-12-U-P5.

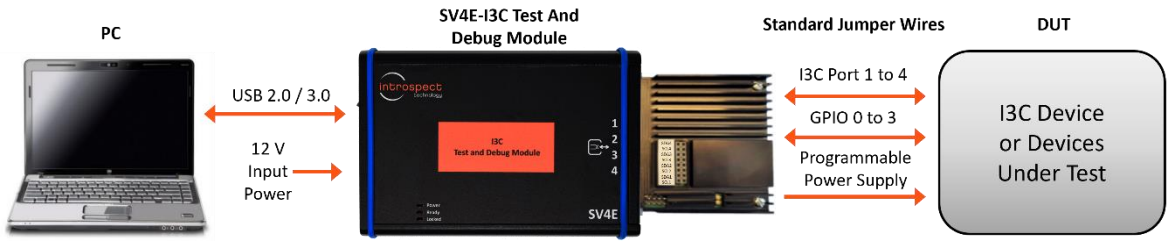


Figure 5: (a) Physical connections to the SV4E-I3C module (b) close-up view of the SV4E-I3C interface board

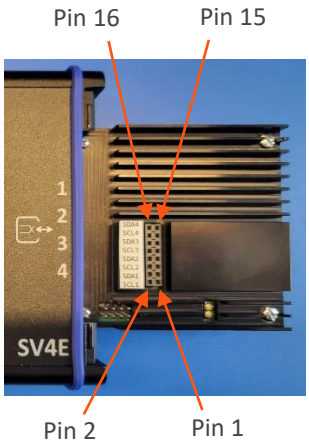
NOTE

The SV4E-I3C is available with two interface options: the standard 2.0 V interface and an extended 3.6 V interface (refer to the ordering information in Table 1). The hardware differences between the two options are contained within the interface board connected to the right side of the SV4E-I3C module, as shown above. The two options require separate firmware versions.

I3C PORT SIGNAL CONNECTIONS

The SV4E-I3C module has a 16 pin female header providing connections to all four I3C ports. The connector is from Samtec (part number BCS-108-L-D-TE) and the pinout for the connector is provided in Table 2 below.

TABLE 2: SV4E I3C SIGNAL PINS

I3C PORT CONNECTOR DIAGRAM	PIN NUMBER	SIGNAL NAME	SIGNAL DESCRIPTION
	2	SCL1	Port 1 I3C Clock
	4	SDA1	Port 1 I3C Data
	6	SCL2	Port 2 I3C Clock
	8	SDA2	Port 2 I3C Data
	10	SCL3	Port 3 I3C Clock
	12	SDA3	Port 3 I3C Data
	14	SCL4	Port 4 I3C Clock
	16	SDA4	Port 4 I3C Data
	1, 3, 5, 7, 9, 11, 13, 15	Ground	Ground

Introspect also provides eight standard 6" jumper cables for rapid connection between the connector and the device under test. Jumper cables are compatible with the female header part number provided above.

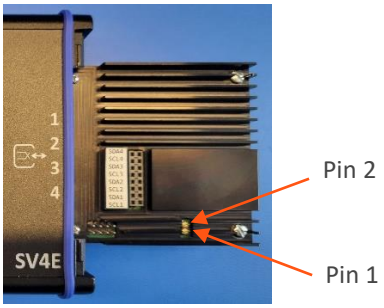
I3C PROGRAMMABLE POWER SUPPLY

The SV4E-I3C module has a 2 pin header providing a direct connection to the VDD supply for the I3C bus. The bus voltage is set directly in Introspect ESP software.

The connector is a standard 0.100" male header (Mill Max Manufacturing, part number 350-10-102-00-006000) and the pinout for the connector is provided in Table 3. If this power supply is brought directly to a DUT board, please ensure that appropriate power supply decoupling is applied where connections are made.

The programmable range of this supply varies according to the interface option used (refer to Table 1). For the standard 2.0 V product, the VDD supply voltage range is 1.0 V to 2.02 V. For the extended range 3.6 V product, the VDD supply voltage range is 2.0 V to 3.6 V. The VDD supply supports up to 1.0 A of output currents across the full output voltage range. Also refer to Table 6 in the specifications section of the document.

TABLE 3: SV4E PROGRAMMABLE POWER SUPPLIES

PROGRAMMABLE POWER SUPPLY, J3 CONNECTOR DIAGRAM	PIN NUMBER	SIGNAL NAME	SIGNAL DESCRIPTION
	1	Ground	Ground
	2	I3C VDD (I3C Bus)	User programmable power supply for VDD for I3C bus. This supply is also used for the logic "1" voltage level for GPIO_2 and GPIO_3 for the standard 2.0 V interface (refer to the next section and to Table 4).

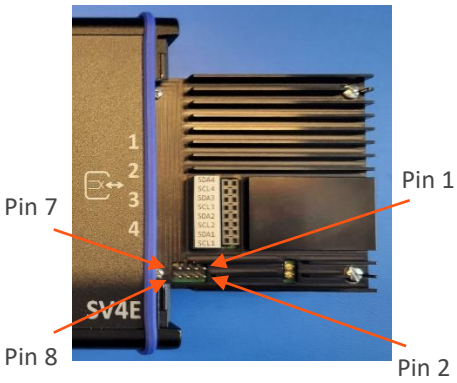
I3C GPIO CONNECTIONS

The SV4E-I3C module has an 8-pin header providing connections to four GPIO pins. The connector is a standard 0.100" male header (Sullins, part number PREC004DAAN-RC) and the pinout for the connector is provided in Table 4.

GPIO_0 and GPIO_1 operate with 1.8 V LVCMOS logic and voltage characteristics which are provided in Table 10 in the "Specifications" section of the document.

GPIO_2 and GPIO_3 voltage characteristics vary according to the interface option used (refer to Table 1). For the standard 2.0 V product, the GPIO_2 and GPIO_3 logic "1" voltage levels track the programmable VDD for I3C bus (refer to Table 3). For the extended range 3.6 V product, the GPIO_2 and GPIO_3 pins operate with 1.8 V LVCMOS logic described in Table 10 in the "Specifications" section of this document.

TABLE 4: SV4E GPIO PINS

GPIO, J2 CONNECTOR DIAGRAM	PIN NUMBER	SIGNAL NAME	SIGNAL DESCRIPTION
	1, 2	Reserved	Reserved
	3	RESET_N (GPIO_0)	SV4E reset pin, active low ("0" = reset, "1" = not in reset) Logic "1" voltage = 1.8 V Logic "0" voltage = 0 V
	4	GPIO_1	User configurable, input or output Logic "1" voltage = 1.8 V Logic "0" voltage = 0 V
	5	GPIO_2	User configurable, input or output Logic "1" voltage = I3C VDD or 1.8 V (see the description above this table) Logic "0" voltage = 0 V
	6	GPIO_3	User configurable, input or output Logic "1" voltage = I3C VDD or 1.8 V (see the description above this table) Logic "0" voltage = 0 V
	7, 8	Ground	Ground

Additional Documentation

SV4E-I3C Quick Start Manual

- EN-G035E-E-20100 - SV4E-I3C Quick Start Manual

SV4E-I3C PurVue Analyzer™ Product Brief

- EN-D034E-E-22154 - I3C PurVue Analyzer™ Product Brief

Specifications

TABLE 5: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Protocol			
Physical Layer Interface	MIPI I3C		MIPI I3C version 1.0 and 1.1 MIPI I3C Basic
	JEDEC I3C		JESD82-511 DDR5 RCD JESD403B Sideband Bus JESD300-5 SPD JESD301-1A PMIC JESD301-2 PMIC JESD302-1 TS5110 Thermal Sensor JESD302-1 TS5111 Thermal Sensor
I3C Controller Device Support	Yes		Includes I2C support
I3C Target Device Support	Yes		Includes I2C support
Ports			
Number of I3C device instances	4		Each fully configurable as controller, secondary controller, or target.
Number of GPIO pins	4		
Programmable On-Board Power Supplies	1		
Connections to PC for Introspect ESP Software Control	2		USB 2.0 USB 3.0 (for I3C PurVue Analyzer™)
Memory			
On-board memory	1	GByte	
Power Consumption			
DC Input Voltage	12	V	DC Input Voltage
Maximum Current Draw	1.6	A	Typical operating current draw

TABLE 6: I3C BUS SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Physical Line Characteristics			
Internal SCL and SDA pull-up: Push-Pull Open Drain Mode High Keeper	 N/A 500 10	 Ohm kOhm	In open drain mode, a 500 Ohm pull-up resistance to I3C VDD is automatically switched onto the line when required
Pin Capacitance	2.5	pF	Typical
Programmed operating voltage			
Standard 2.0 V Interface: Minimum Programmed VDD voltage Maximum Programmed VDD voltage	 800 2020	 mV mV	VDD sets SCL and SDA high voltage
Extended 3.6 V Interface: Minimum Programmed VDD voltage Maximum Programmed VDD voltage	 2000 3600	 mV mV	VDD sets SCL and SDA high voltage
VDD resolution	1	mV	
Operating Frequencies			
Minimum Open Drain Frequency	0.25	MHz	
Maximum Open Drain Frequency	5.0	MHz	
Minimum Push-Pull Frequency	0.25	MHz	
Maximum Push-Pull Frequency	12.5	MHz	
Minimum Legacy I2C Frequency	0.002	MHz	Interoperates with legacy I2C devices
Maximum Legacy I2C Frequency	1	MHz	Interoperates with legacy I2C devices

TABLE 7: I3C BUS TIMING SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
SCL / SDA Timing			
SDA Setup Time Range	1.0	UI	Specification for the timing from SCL falling edge to the following SDA edge, expressed as a fraction of the UI. See Figure 6 on following page.
Independent SDA Setup Timing	Yes		SDA setup time is set independently for I3C Open Drain, I3C Push Pull, and I2C operation
SCL to SDA Skew Injection Resolution	2.5 *	ns	Timing resolution, SCL to SDA for 12.5 MHz Push-Pull Operation. Please see footnote below. A diagram of SDA setup time is shown in Figure 6 on the following page.
Duty Cycle Timing Resolution	10	ns	
Protocol Analyzer Timing Resolution	10	ns	Timing resolution for the digital protocol analyzer. The PurVue Analyzer has greater timing resolution, refer to Table 8.

* This 2.5 ns timing resolution may be selectively applied to any one of the parameters listed below. All other timing parameters may be set with 10 ns resolution.

Push-Pull SDA setup time
HDR / DDR Positive SDA setup time
HDR / DDR Negative SDA setup time
Start or Repeated Start hold time (t_{CAS} or t_{CASr})
Repeated Start setup time (t_{CBSr})
Stop setup time (t_{CBP})

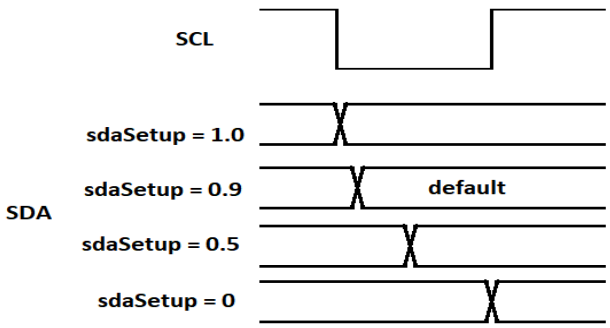


Figure 6: Timing diagram for SDA setup time.

TABLE 8: PURVUE ANALYZER™ SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
General Performance			
Number of Channels	2		Analysis for SCL and SDA of one port
Minimum Input Voltage	-500	mV	
Maximum Input Voltage	3600	mV	
Oscilloscope Resolution	12	bit	1 mV resolution at full input range
Oscilloscope Triggering			Oscilloscope captures are triggered by I3C protocol events
Sampling Rate	1.0	GHz	Maximum sampling rate
Data Transfer (via USB 3.0)	5.0	Gbps	Provides rapid waveform uploads

TABLE 9: I3C MODES AND OPERATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Additional supported features			
Operations	CCC Direct RW Private RW Hot-Join IBI		
Signaling Modes	SDR HDR-DDR		
Mixed Bus Mode Support	Yes		
50 ns Spike Filter	Yes		Automatic for mixed bus mode
Error Injection	Yes		ACK/NACK behavior Flipped parity bit Setup time and hold time violations
Protocol Analysis	Yes		
Offline Capability / Tri-State Mode	Yes		Tri-state mode for SCL/SDA pins

TABLE 10: 1.8 V LVCMOS GPIO CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Voltage			
Voltage Level	1.8	V	All values on the left are listed for 1.8 V LVCMOS logic only. See page 11 and Table 4 for a list of all possible voltage levels supported by the GPIO pins.
V_{IL} minimum	-0.3	V	
V_{IL} maximum	0.7	V	
V_{IH} minimum	1.5	V	
V_{IH} maximum	2.25	V	
V_{OL} maximum	0.4	V	
V_{OH} minimum	1.7	V	

REVISION NUMBER	HISTORY	DATE
1.0	Document Release	June 8, 2020
1.1	Updated specifications	April 24, 2021
1.2	Updated specifications, description of new features	June 3, 2022
1.3	Updated specifications, improved pinout clarity in Figures 2 to 4	September 20, 2022

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