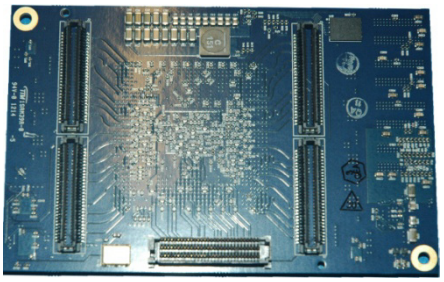
SV3D SerDes Transceiver Endpoint

Product Brief

32 Lane, 14 Gbps Plugin-Module Enables Test on Any Load Board



Highly-integrated tester that mounts directly on an application or test board without requiring cables. Featuring **32 independent** receivers and transmitters, SV3D satisfies a growing need for parallel, multi-site Gbps testing methodology at the lowest possible total cost.

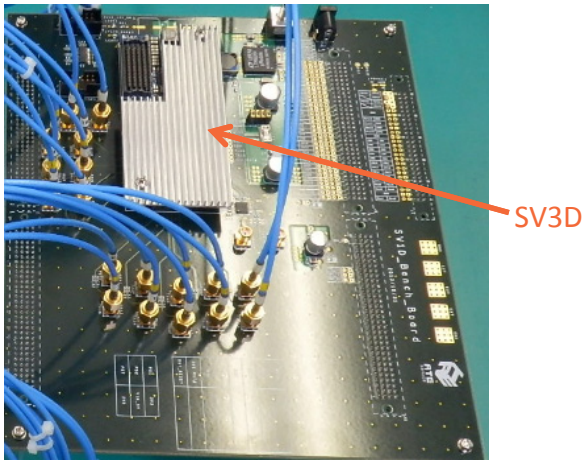
Key Features:

- **Data rates and lanes:** 250 Mbps to 14 Gbps fully-continuous operating range on up to 32 independent Tx and Rx differential lanes.
- **Signal impairments:** sinusoidal and random jitter, de-emphasis, skew, and bit slip.
- **DUT Tx measurements:** eye diagram, EQ, analog waveform and jitter separation.
- **Easy of integration:** direct attachment with standard, low-cost connectors. Single 12-V DC power supply with internal regulation. Internal clock synthesis and jitter cleaning.

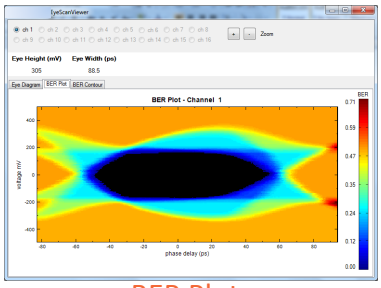
Key Benefits:

- **Multi-Site:** with its small size and high lane count, the SV3D can test many parallel devices simultaneously.
- **Self Contained:** an all-in-one system reduces board space and helps create a compact tester-on-board for characterization tasks or production test.
- **Automation:** Scripting capability is ideal for debug tasks, verification and full-fledged production screening of devices and system boards.

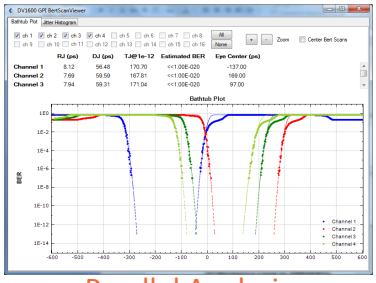
Typical Application:



Typical Application (Tester on Board)



BER Plot



Parallel Analysis

For Developing • For Verifying • For Shipping

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Pattern Generator Functions

Feature	Description	Benefit
Pattern Generators	Pre-built patterns, PRBS (5, 7, 9, 11, 15, 23, 31), custom user-defined pattern, nested pattern sequencers	Allows for flexible stimulus generation (e.g. training sequences or compliance patterns)
Analog Controls	Polarity inversion, voltage swing, transmit pre-emphasis, duty cycle, bit-slip	Provides deep receiver stress characterization with truly independent multi-variable analysis
Synthesis Capability	Sinusoidal jitter injection, random jitter injection, de-emphasis generation	Allows for compliance-based receiver testing with internally synthesized noise sources

BERT and Scope Functions

Feature	Description	Benefit
Error Detectors	BERT engines work with all types of patterns listed under Pattern Generator section; single-shot (up to 2^{32} cycles) or continuous error counting modes; 32-bit error counters; automatic pattern alignment	Optimized architecture for production testing and data collection, ensuring rapid pattern alignment and error checking
Equalizer Control	Continuous-time linear equalizers, DFE; ability to measure closed eyes	Allows for design exploration, de-embedding, and correlation with simulation
Clock Recovery	Per-pin analog, hardware clock recovery unit with optimized connection to sampling circuitry	Offers a realistic test environment on any production ATE load board
Analysis Capability	Identify pattern; BERT measurement; BERT scan; eye diagram; analog waveform capture; jitter separation; transition & non-transition eyes	Rapid signal integrity analysis functions behind each transceiver channel

Environment and Control

Feature	Description	Benefit
Parallel Tester Bus	Dedicated low-frequency control I/O pins for extended test program flexibility	Access and set the DUT SerDes control registers or expand the SPI bus for multi-site testing
User Interface	SPI command register space with full suite of capability. Compatible with Introspect ESP software for automatic SPI vector generation	Enables full lab automation; provides a scalable, future-proof solution
Scripting	Data logging; automatic report generation	Suited for performing optimization sweeps

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