Next Generation Digital Tester Design

White Paper

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Introduction

Increasingly, semiconductor component manufacturers and electronic module manufacturers embark on creating custom test systems based on commercial off the shelf (COTS) components. Instead of purchasing third-party Automatic Test Equipment (ATE), these organizations are tempted to rely on building their own in-house systems out of microcontrollers and FPGAs for performing the required highly specialized test, measurement, and processing functions. The motivations for this approach are well understood: ATE has become expensive and technologically lagging.

At face value, the above methodology has the perceived benefit of dramatically reducing bill-of-material and operational costs once a tester design is released to manufacturing. This being said, design iterations as well as firmware and embedded software development efforts become dominant cost factors. If not carefully scheduled and managed, this part of development can represent a major hurdle to profitability and flexibility; a hurdle that has been faced by the ATE manufacturers themselves over recent years. To address this hurdle, plug-in digital test modules called **Direct Attach SerDes Transceiver End-Points** have been created specifically for in-house instrument makers who desire the *fastest time to market for introducing FPGA-based high-speed digital testers*. These modules are the result of multiple generations of research and development on high-speed test and measurement instruments for the electronic component, board, and system industries.

In the following section, we describe how design iterations can impact profitability. Then, we introduce the advanced FPGA-based architecture of Introspect's **Direct Attach SerDes Transceiver End-Points**. We then describe the included parametric measurement features as well as functional and protocol-aware features that result in a truly capable digital tester.

Problem: Never-Ending Design and its Impact on Profitability

The impact of slower development times on the long term profit of a given project is well documented and understood as attested by the summary data below, which was taken from a study by the Pivot International consulting group [1]:

- A 12 month reduction in time to market increases Internal Rate of Return (IRR) by ~92%.
- A 9 month reduction in time to market increases IRR by ~63%.
- A 6 month reduction in time to market increases IRR by ~39%.

These relationships are, for the most part, unaffected by changes in other variables including product life or product profitability, and this is illustrated in Figure 1. This figure, which is adapted directly from [1], plots a product's Internal Rate of Return as a function of development time for varying ratios of annual gross profit to investment.

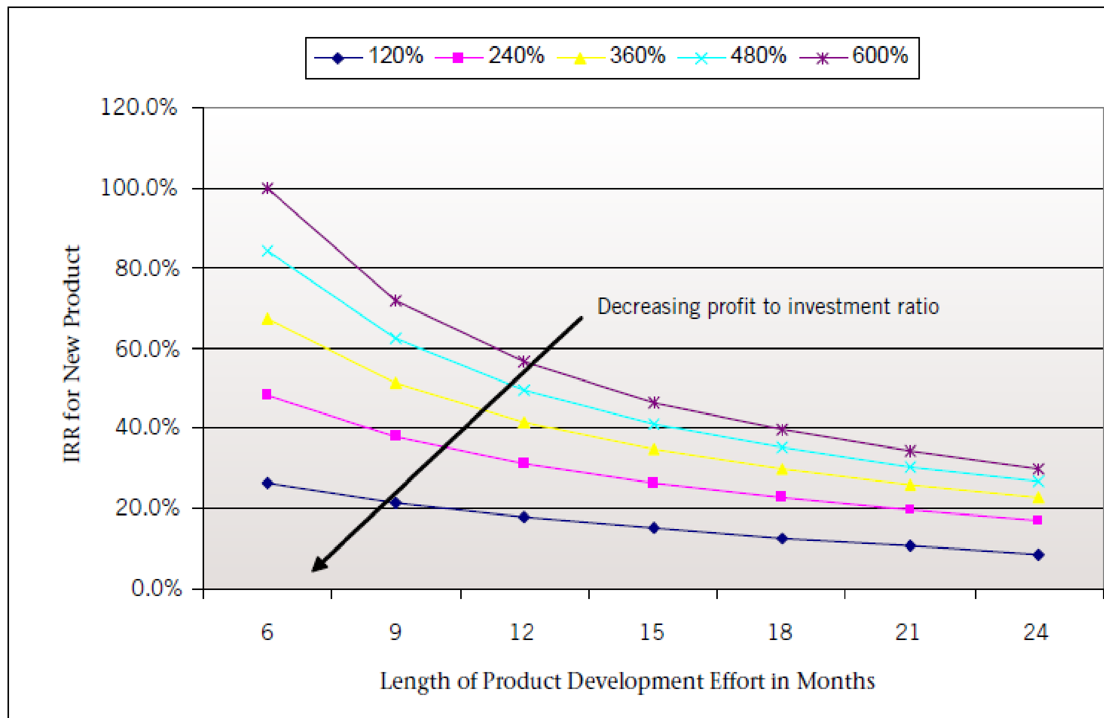


Figure 1 Internal Rate of Return as a function of development time.

As can be seen in Figure 1, regardless of the profit level, reducing time to market is the single most important factor contributing to return on investment. Yet, tester development programs often run well beyond budgeted schedule and cost, and this has grave effects on the commercial benefits of introducing a new tester product [2]. Various factors impede the ability of ATE or internal test instrument developers to deliver products on time, and these include:

- Extremely complex system designs with a tendency to follow an "all-in" approach to feature selection
- Constantly shifting user requirements
- Little attention to hidden costs associated with difficult-to-track soft deliverables such as firmware or embedded software

Because of these factors, it is not uncommon in the industry to have 12-24 month delays in full-feature tester product releases [2]. What is worse is that incremental “urgent” releases are often made in order to meet immediate customer demands, thus forcing development teams to enter into a nearly perpetual cycle of bug fixes and corrections. *Recognizing the hidden costs of never-ending tweaks to firmware and embedded software features is key to the profitability of any tester development program whether internal or commercial*, and this is addressed in the next section.

Solution: An Introspect Module is the Tester and it is Ready-Made

In this section, we describe how to best leverage an FPGA-based architecture for constructing a high-speed digital tester. Specifically, we describe Introspect’s plug-in test cards, which have been created specifically for high-speed digital test instrument deployment on large scale and in the timeliest manner. Figure 2 shows the architecture of the test cards. Deceptively simple, these cards have been engineered for high-performance test applications, optimizing all aspects of test instrument development from high-speed interfaces to calibration and data logging. At the center of the instrument is a high-performance tester engine called **Introspect ESP**. This engine performs most of the “test” functionality that is advertised for the instrument (including determining the maximum data rate) and the interface to the device-under-test (DUT) pins. Additionally, minimal support circuitry is included on the test card. Namely, the following components are added

- High-performance fractional clock synthesis supporting continuous data rate control from DC up to 28 Gbps
- Non-volatile memory for storing multiple configuration files
- Program memory for storing embedded test procedures and embedded CPU code
- Non-volatile memory for storing test data and/or calibration data
- Volatile user memory (for test patterns, etc.)
- A backplane controller to communicate with the host system’s native language

As can be seen, very simple hardware elements are deployed, and this allows for extreme selectivity of designed-part grades and component value derating. The bulk of the high-speed digital testing functionality is embedded in the form of a ready-designed, ready-verified, ready-synthesized **Introspect ESP** engine.

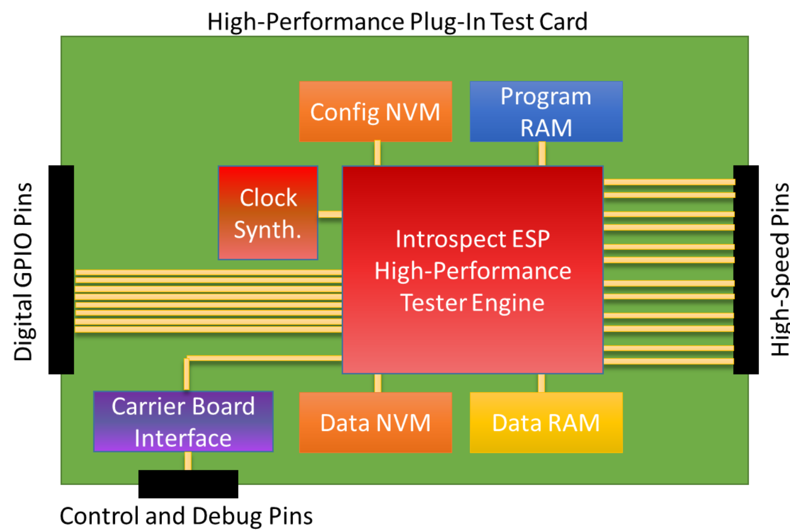
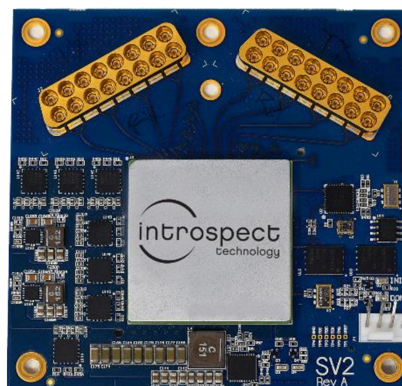


Figure 2 Introspect plug-in test card architecture: simple at a high level, extremely attentive to tester-centric detail.

The **Introspect ESP** architecture has been refined over multiple generations of high-speed digital instruments. Figure 3 shows three existing test cards that are based on this architecture. In Figure 3(a), an extremely high-performance module is illustrated that includes high-speed SerDes capability, digital vector capability, 2 GBytes of DDR3 DRAM, and on-board calibration circuitry. The card is capable of testing SerDes links up to 14 Gbps while at the same time acting as a digital debug vector sequencer for test interfaces on devices under test. Similarly, Figure 3(b) shows a massively parallel system with 32 bidirectional SerDes links and hundreds of digital general-purpose I/O (GPIO) pins. Such scale of capability in a small form factor enables surprisingly flexible protocol test applications. Finally, Figure 3(c) illustrates a test card capable of operating at 28 Gbps across 8 lanes. In all of these cases, the hardware architecture is very similar to that of Figure 2.

(a)

(b)



(c)

Figure 3 Three examples of Introspect plug-in test cards: (a) 14 Gbps SerDes tester with digital vector generation, (b) 32-lane SerDes end-point with ~150 digital pin electronics, and (c) 8-lane 28 Gbps parallel link tester.

In the following sections, we describe the various features that enable the Introspect test cards to be the solution of choice for high-speed digital tester designs worldwide. We start with parametric features, and then we describe functional and protocol-aware test features and the unified software architecture that is compatible with industry-standard tools.

Wide Ranging Tester Capability

AC Parametric Features

This section describes the various AC parametric features that are included in **Introspect ESP**. To be fully utilized, any high-speed digital test instrument is generally expected to perform a set of analog functions such as

- Programmable transmitter voltage swing control
- Programmable transmitter waveform shape control
- Programmable transmitter skew control (delay lines) and jitter injection
- Receiver comparator threshold control
- Receiver strobe timing control (delay lines) and jitter measurement

These, and others, are all supported in a test card like those shown in Figure 3. Specifically, Figure 4 shows how the tester's driver waveform shape is controlled in order to emulate different system-level bandwidth effects or to introduce data-dependent jitter.

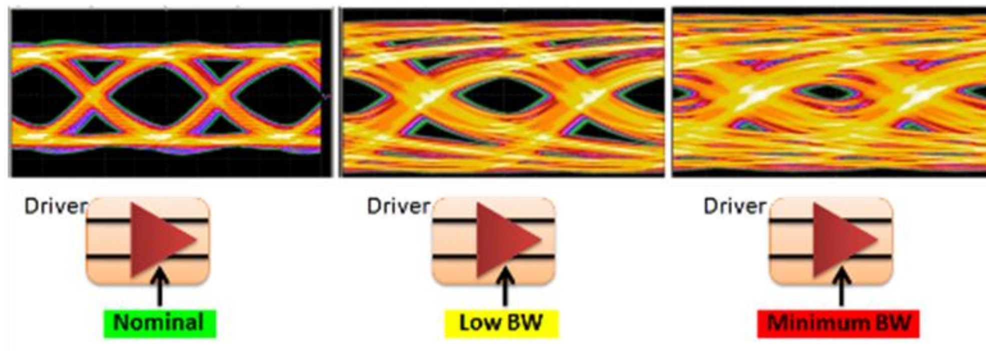


Figure 4 Waveform shape control and jitter injection.

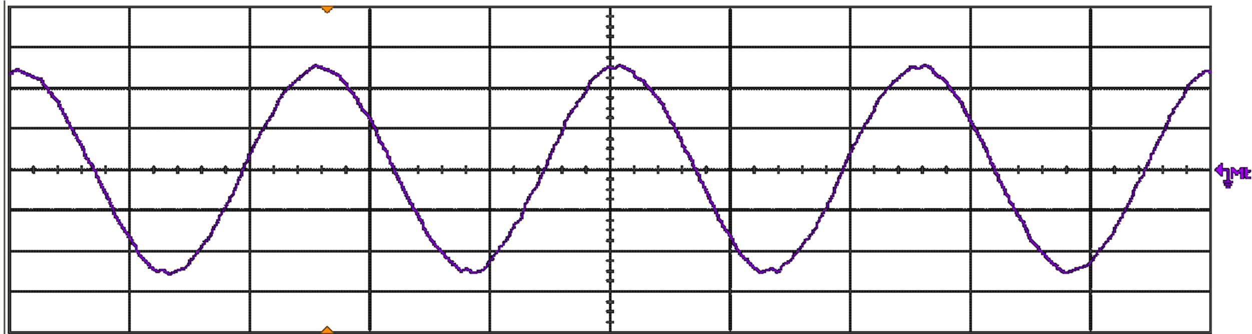


Figure 5 Time-domain view of high-purity injected jitter at 28 Gbps.

Similarly, Figure 5 shows an example of sinusoidal jitter injection at 28 Gbps, which is enabled in **Introspect ESP**. The figure illustrates superior signal fidelity in the injected jitter. It is important to note that Figure 5 has the dimensions of time versus time. That is, the y-axis is the time deviation of digital edges (in femtoseconds) from their ideal locations. **Introspect ESP** allows the digital synthesis of high spectral-purity jitter waveforms.

Finally, Figure 6, Figure 7, and Figure 8 show the various measurement features of **Introspect ESP**. All of these features rely on unique time-base technology and mixed-signal digital signal processing (DSP) algorithms.

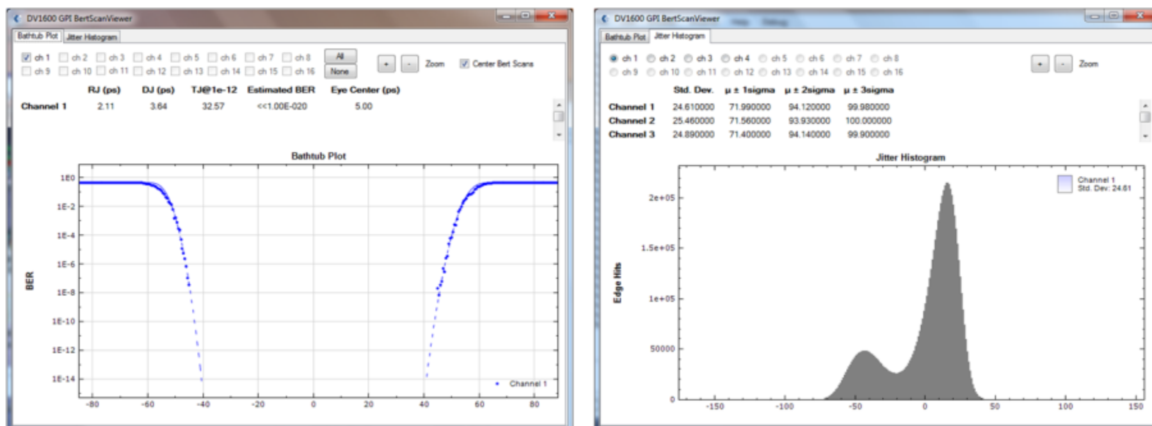


Figure 6 Per-pin jitter measurement through bathtub plots and histograms.

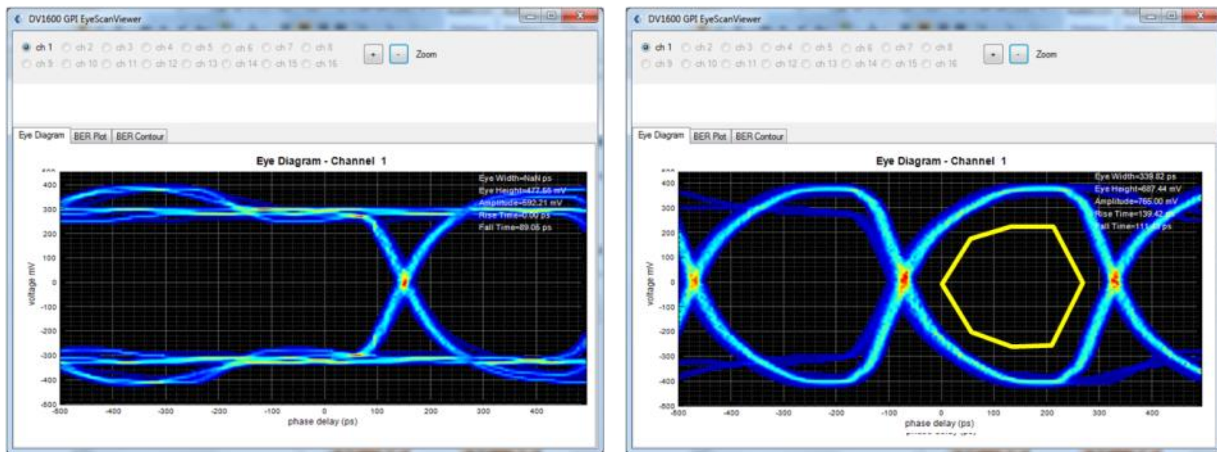


Figure 7 Complex eye diagram captures and mask testing: (a) non-transition eye, and (b) worst-case transition eye.

Figure 8 Per-pin oscilloscope captures with automated parameter extraction.

Functional and Protocol-Aware Features

Introspect ESP is based on an award-winning test instrument architecture. It offers a highly intuitive GUI, and it enables true protocol awareness for popular standards. Figure 9 shows a screen capture of the **Introspect ESP** Software GUI that illustrates protocol-based video frame generation. In this setup, the plug-in test card is configured to be a MIPI D-PHY generator, enabling the transmission of completely compliant protocol packets, whether they are CSI-2, DSI, or proprietary. Similarly, Figure 10 and Figure 11 show a receiver application in which the plug-in test card acts as a protocol receiver, decoding received packets in real-time and constructing message data (an image frame in this case) and analyzing the contents of the packets for verification of packet construction and packet error rate. Finally, other protocol capability exists such as PCI Express.

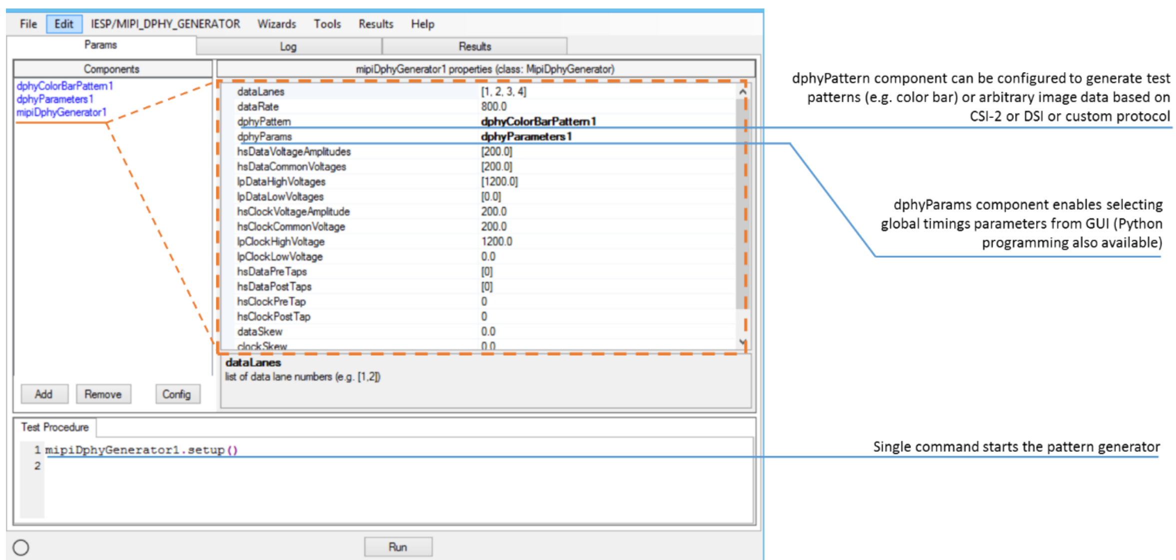


Figure 9 Illustration of unified, high-level software environment and protocol based video frame generation.

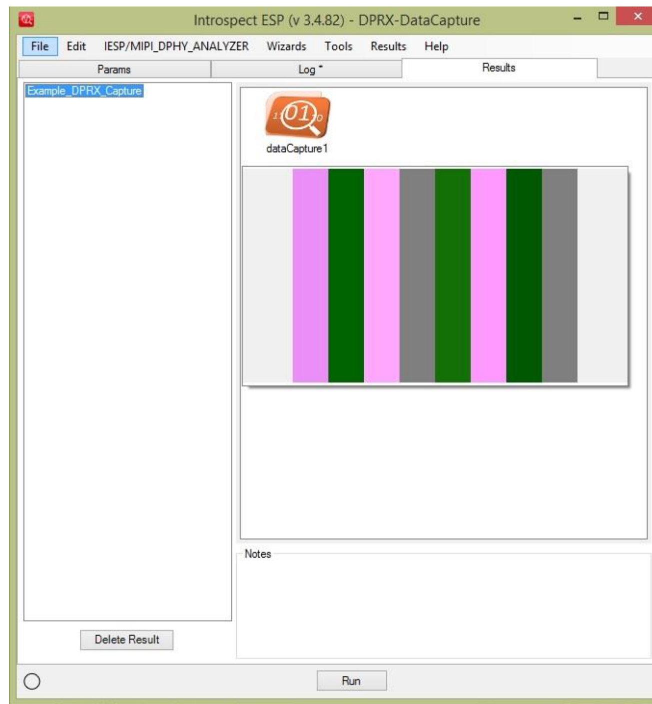


Figure 10 Introspect software illustrating reception of protocol data (imaging application) and reconstruction of it for visualization (plotting real images).

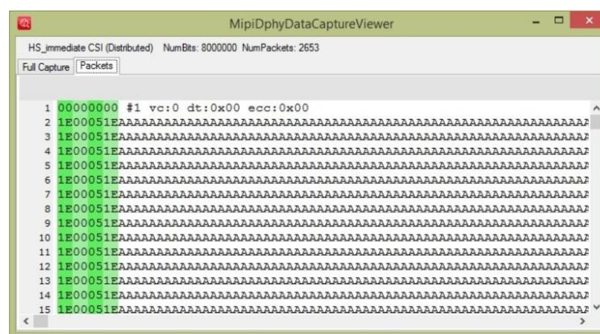


Figure 11 Packet analysis view of Introspect ESP Software.

Digital Test Vector Sequencing

In addition to high-speed transceiver testing, real-life device screening requires some amount of vector sequencing for failure analysis, device register programming, or even scan chain testing. **Introspect ESP** enables vector sequencing in a manner very similar to commercial ATE. In Figure 12, an ASCII vector file is shown illustrating multiple pin format options such as drive high, drive low, compare high, and compare low.

```
 1 FORMAT gpio_01 gpio_02 gpio_03 gpio_04 gpio_05 gpio_
 2 R3  tset1 1X1111111100010000000001000100000100;
 3 R1  tset1 1X0100000000000000010000001001101001;
 4 R40 tset1 1X11XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX;
 5 R1 tset1 1X11HLHLLLLLLLHLLLHLLLHLLLLLLLLLLLLL;
 6 R1  tset1 1X00XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX;
 7 R1  tset1 1X11XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX;
 8 R3  tset1 1X1111111100010000000001000100000100;
 9 R1  tset1 1X1000000000000000010000001001101001;
10 R1 tset1 1X1110100000001000100010000000000000;
11 R1 tset1 1X1110100000001000100010000000000000;
12 R1 tset1 1X0010100000001000100010000000000000;
13 R15 tset1 1X0010100000001000100010000000000000;
14 R1 tset1 1X1010100000001000100010000000000000;
```

Figure 12 Sample ATE vector file that can be executed within Introspect ESP's optional vector sequencing capability.

Plug-In Test Cards Represent the Best of Make vs. Buy

As previously stated, time to market is perhaps the most critical parameter in determining the viability of tester development (whether internal or external). Choosing COTS firmware and software as well as hardware components is now an option for high speed digital test. The design team can now focus resources on product specific engineering tasks, such as socket design and system integration software, while choosing the **Introspect Direct Attach Transceiver Endpoint** to eliminate the need to re-invent timing and formatting firmware and embedded software. Such division of labor approach results in tremendous productivity enhancement, and this is perhaps best illustrated by the test system

in Figure 13. In the figure, a complete MIPI D-PHY receiver test system with CSI-2 protocol capability was constructed in record time (~8 weeks). This was enabled by allowing the application engineer to focus on the illuminator/socket setup while relying on the Introspect SV1D for all MIPI CSI-2 capture and debug capability.

Figure 13   Illustration of a complete protocol-based image sensor test system based on Introspect's SV1D plug-in test card.

Conclusion

In this paper, we described a plug-in test card solution that dramatically alters the economics of development for next-generation high-speed digital tester instruments. The solution eliminates a large portion of the uncertainty that is associated with new product development, and it provides innovative solutions for the most advanced digital test applications. Consisting of a robust **Introspect ESP** engine, embedded software, and sophisticated programming environment and GUI, it allows for rapid introduction of digital test capability while co-existing with tried and true internal product development processes. It also allows for the creation of scalable test solutions (in terms of number of channels and speed) since these fundamental specifications are now determined by the underlying FPGA and not any given ASIC technology.

References

[1] Kirk Douglass, "What Does Product Development Really Cost?", Pivot International, http://www.pivotint.com/images/pdfs/Pivot_what-does-product-development-really-cost.pdf

[2] F. Gino; G. P. Pisano. Teradyne Corporation: The Jaguar Project. Harvard Case 9-606-042.

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