introspect technology

Empowering Solutions for High-Speed Communications

MIPI Brochure

2015 BEST in Design & Test WINNER
DesignCon
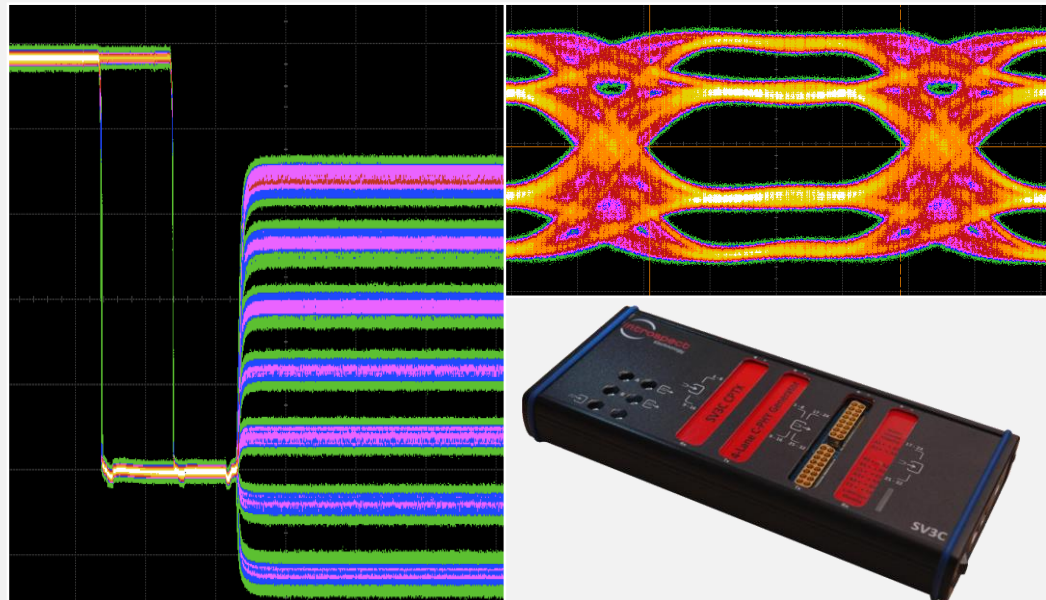
Industry leading solutions for laboratory, validation, and production testing in the rapidly changing landscape of high–speed I/O.

Ultra Portable

With Introspect, more engineers have access to high–performance testing, increasing throughput at every stage of a product's life cycle from the bench to customer service. What previously took racks of equipment fits in the palm of your hand.

*SV1C Personal SerDes Tester*

High Performance

All Introspect tools offer user–defined control over transmitter and receiver attributes including signal amplitudes, jitter injection, and phase delay. Capture eye diagrams and bathtub plots according to any data rate or pattern, in burst or high–speed–only modes. Full support for physical– and transport–layer testing of PCIe Gen1–Gen3, MIPI C–PHY, D–PHY, and more!
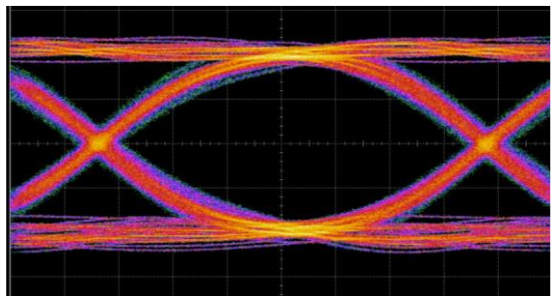
SV2C Eye Diagram at 28 Gbps

Powerful Software

Python–based software enables real–time control over your tests with the flexibility to build and automate to your needs. With a single line, execute a BERT or change data rates, or command loops synchronized with your device to find its exact, optimized operating conditions. Automation made easy!
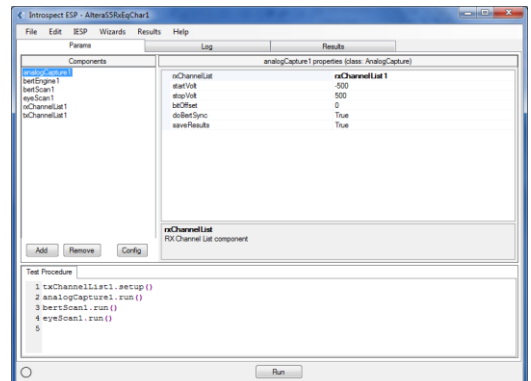
IntrospectESP GUI

Generators and Analyzers for D-PHY, C-PHY, and M-PHY

Introspect provides the capability to understand the limits of your devices and measure real-world performance. SV3C Generators are dual-capable C-PHY and D-PHY to transmit MIPI-compliant data, inject physical and protocol impairments and interoperate with your devices. The CPRX 4-Lane C-PHY Analyzer is the winner of the 2015 DesignCon Best in Design & Test and is the only system capable of eye capture, complete BER detection and protocol analysis.

Physical Layer Performance

- **C-PHY 1.0/1.1:** 4 Lanes (12 wires)

- **D-PHY 1.2/2.0:** 4 Lanes + CLK (10 wires)

- **M-PHY G1-G3/G4:** 8 Lanes (16 wires)

- Per-wire skew control with 1-ps resolution

- Per-lane HS and LP amplitude controls

- Inject impairments such as DCD, jitter and skew

- Capture eye diagrams, count errors and analyze packets for timing and payload analysis
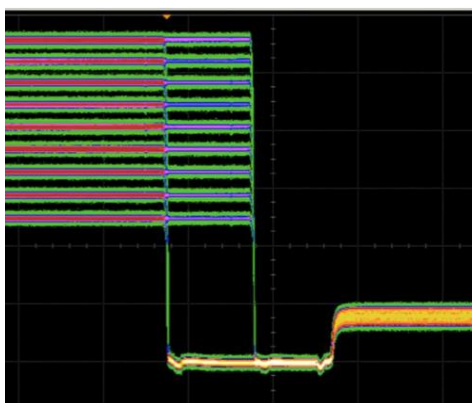
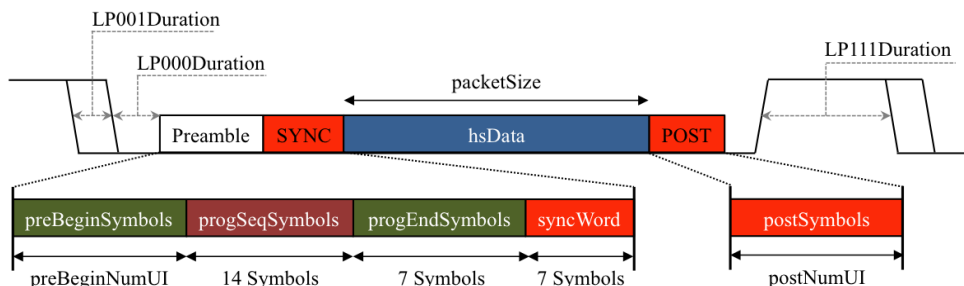*SV3C-CPTX sweeping LP Voltage for C-PHY LP Voltage Tolerance Test*

Interoperability

- DSI/CSI compilers for both D-PHY and C-PHY

- Packet payloads of real images, PRBS patterns, counter patterns and user-defined creations

- Burst and High-Speed Only modes of operation

- Full user-control over LP and HS global timing parameters and payload characteristics
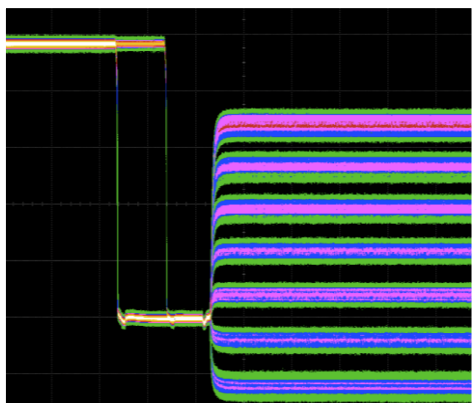
SV3C-DPTX sweeping HS common-mode level for D-PHY HS CM Voltage Test

SV3C-CPTX Packet Construction: Using the IntrospectESP Software, packet building blocks are user-defined and can be varied on-the-fly

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SV3C–DPTX sweeping differential HS voltage swing with high precision

SV3C–DPTX provides individual HS voltage swing control for each lane

SV3C–DPTX sweeping clock and data skew individually

SV3C–DPTX provides individual jitter injection control for each lane

SV3C–DPTX programming a positive CM voltage for Lane 0 and a negative CM voltage for Lane 3

SV3C–DPRX screen capture illustrating Python reporting and analysis of received packet data

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SV3C-CPTX global packet construction is similar to DPTX

SV3C-CPTX automatically maps and encodes C-PHY symbols

Screen shot of SV3C-CPTX output illustrating high-fidelity three-level signaling

SV3C-CPTX includes a full suite of signal impairments per wire such as jitter, skew, and voltage mismatch

Award-winning SV3C-CPRX offers unprecedented analysis capability and ease of use. It is the only electrical/protocol C-PHY analyzer in the industry

SV1C-MPHY Gear3 output eye diagram after long channel
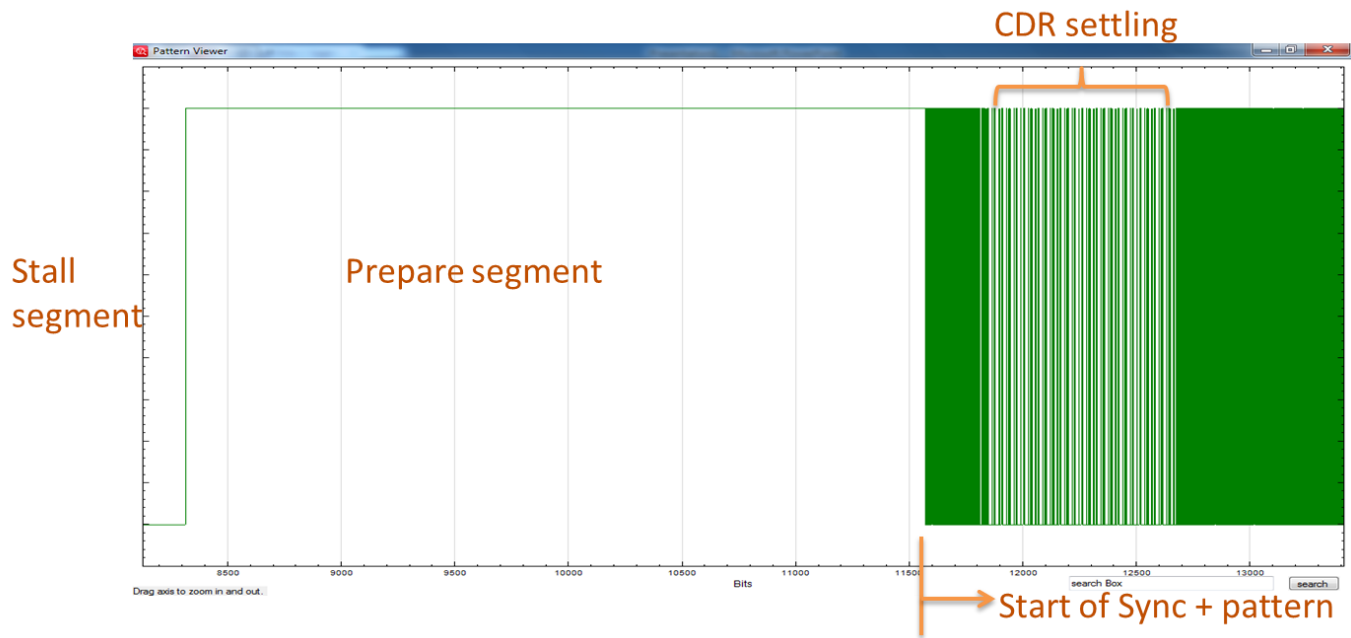
SV1C-MPHY Gear3 BER measurement in burst-mode

Product Name*	Ideal for…	Main Features
SV3C DPTX *(Item No. 4584)*	▪ D–PHY 1.2 receiver test (fw upgrade to v2.0) ▪ CSI–2/DSI protocol test ▪ Live video interoperability test ▪ Channel test & crosstalk generation ▪ System–level test	▪ Up to 2.5 Gbps (fw upgrade to 4.5 Gbps) ▪ Per–lane skew injection, jitter injection, LP voltage control, HS voltage control ▪ SSC injection (common on all lanes) ▪ High–resolution CSI/DSI frame generation & error injection
SV3C CPTX *(Item No. 4586)*	▪ C–PHY 1.0 receiver test (fw upgrade to v1.1) ▪ CSI–2/DSI protocol test ▪ Live video interoperability test ▪ Channel test & crosstalk generation ▪ System–level test	▪ Up to 3.0 Gsps (ready for v1.1) ▪ Per–wire skew injection, jitter injection, LP voltage control, HS voltage control ▪ Automatic encoding and mapping ▪ High–resolution CSI/DSI frame generation & error injection
SV3C DPTXCPTX *(Item No. 4588)*	▪ D–PHY 1.2 and C–PHY 1.0 receiver test ▪ CSI–2/DSI protocol test ▪ Live video interoperability test ▪ Channel test & crosstalk generation ▪ System–level test	▪ Ultimate product for dual–roadmap development strategy ▪ Single hardware supports both D–PHY and C–PHY receiver testing
SV3C DPRX *(Item No. 4585)*	▪ D–PHY 1.2 transmitter test ▪ BER test ▪ CSI–2/DSI protocol test ▪ Live video interoperability test ▪ FPGA streaming	▪ Up to 2.5 Gbps (fw upgrade to 4.5 Gbps) ▪ Dynamic termination control ▪ Burst–mode BER testing and protocol decode
SV3C CPRX *(Item No. 4587)*	▪ C–PHY 1.0 transmitter test (fw upgrade to v1.1) ▪ BER test ▪ CSI–2/DSI protocol test ▪ Live video interoperability test ▪ FPGA streaming	▪ Up to 3.0 Gsps (ready for v1.1) ▪ Built–in C–PHY CDR ▪ Dynamic termination control ▪ Built–in symbol decode & demap ▪ Burst–mode BER testing and protocol decode
SV1C DPTX *(Item No. 4208+4280)*	▪ D–PHY 1.1 receiver test ▪ CSI–2/DSI protocol test	▪ Up to 1.5 Gbps ▪ Global timing control and data–to–clock skew
SV1C DPRX *(Item No. 4208+4281)*	▪ D–PHY 1.1 transmitter test ▪ CSI–2/DSI protocol test	▪ Up to 1.5 Gbps ▪ Burst–mode BER testing & protocol decode
SV1C MPHY *(Item No. 4212+4284)*	▪ M–PHY G1/2/3 receiver & transmitter test (fw upgrade to G4) ▪ PWM & HS burst–mode BER test	▪ Up to 12.5 Gbps ▪ Burst–mode BER checking

* All products include 18 GHz cable assembly and IntrospectESP Software license

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