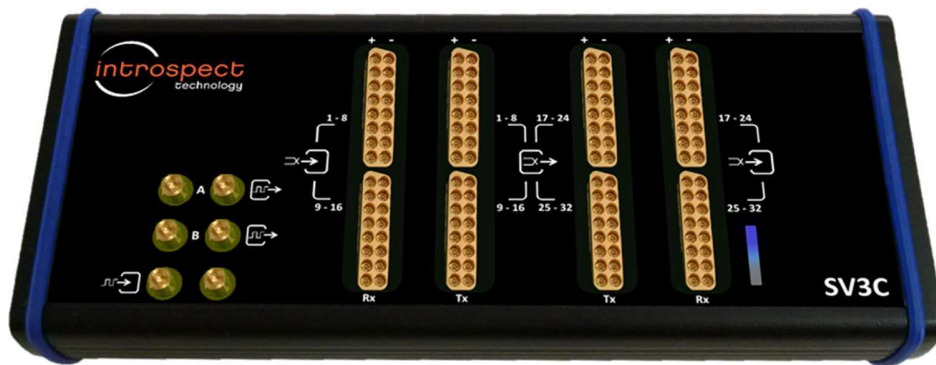




# SV3C Personalized SerDes Tester



[Data Sheet](#)

## Table of Contents

Table of Contents .....	1
List of Figures .....	2
List of Tables .....	2
Introduction .....	3
Overview .....	3
Key Benefits .....	3
Applications.....	4
Features .....	5
Any-Rate Clocking .....	5
Standard Error Detector Analysis.....	5
Per-Lane Clock Recovery and Unique Dual-Path Architecture .....	6
Digital Vector Ports and Utility Power Supply .....	7
Automation .....	8
Specifications .....	9

## List of Figures

Figure 1	SV3C at a glance: more integrated, more productive.....	3
Figure 2	Clock system architecture inside the SV3C.....	5
Figure 3	Sampling of analysis and report windows.....	6
Figure 4	Per-lane clock recovery and dual-path architecture.....	7
Figure 5	Molex 15-91-2125 ribbon cable connector.....	8
Figure 6	Samtec SEAC high-performance, high-density cable connector.....	8
Figure 7	Screen captures of Introspect ESP user environment.....	8

## List of Tables

Table 1	Low-speed connector pin counts.....	8
Table 2	General Specifications.....	9
Table 3	Transmitter Characteristics.....	10
Table 4	Receiver Characteristics.....	11
Table 5	Clocking Characteristics.....	12
Table 6	Pattern Handling Characteristics.....	13
Table 7	Instruction Sequence Cache.....	14
Table 8	DUT Control Capabilities.....	14

# Introduction

## Overview

The SV3C Personalized SerDes Tester is an ultra-portable, high-performance instrument capable of receiver and transmitter validation at data rates up to 14 Gbps and on up to 32 lanes simultaneously. Like the previous generation SV1C, the SV3C integrates multiple technologies in order to enable the self-contained test and measurement of SerDes interfaces such as PCI Express Gen 3, MIPI M-PHY, or USB3. This highly integrated tester also includes unique reconfiguration and protocol technologies that allow it to tackle advanced protocols.

Figure 1 shows a comparative illustration of the SV3C and highlights the main advancements it offers over the SV1C. Fitting in one hand and containing 32 independent stimulus generation ports, 32 independent capture and measurement ports and various clocking, synchronization and lane-expansion capabilities, the SV3C has been designed specifically to address the growing need of a parallel, system-oriented test methodology while offering world-class signal-integrity features such as jitter injection and jitter measurement.



- More high-speed lanes (4x)
- More low-speed ports (~4x)
- Miniature GPIO connector
- More flexible reconfiguration and protocol options
- Identical software and automation experience

Figure 1 SV3C at a glance: more integrated, more productive.

## Key Benefits

- Highest level of integration at 32 lanes in a handheld form factor
- Fully-synthesized integrated jitter injection on all lanes
- Flexible pre-emphasis, equalization, and clock recovery per lane
- Flexible loopback support per lane
- State of the art programming environment based on the highly intuitive Python language
- Single-ended or differential low-speed I/O for digital test vector processing
- Reconfigurable, protocol customization (on request)

## Applications

Parallel PHY validation of SerDes bus standards such as:

- PCI Express (PCIe)
- MIPI C-PHY
- MIPI M-PHY
- CPRI
- USB
- HDMI
- MIPI D-PHY
- XAUI
- JESD204B
- SATA

Interface test of electrical/optical media such as:

- Backplane
- Cable
- CFP MSA, SFP MSA, SFP+ MSA

Plug-and-play system-level validation such as:

- PCI Express (PCIe) Gen1, Gen2, Gen3
- USB 3.0, 3.0a, 3.0b
- SATA 3.0

Timing verification:

- PLL transfer function measurement
- Clock recovery bandwidth verification
- Frequency ppm offset characterization

Mixed-technology applications:

- High-speed ADC and DAC (JESD204) data capture and/or synthesis
- FPGA-based system development
- Channel and device emulation
- Clock-recovery triggering for external oscilloscope or BERT equipment

## Features

### Any-Rate Clocking

The SV3C includes internal frequency synthesizers capable of generating any test data rate. Additionally, the SV3C contains reference clock outputs for driving devices under test or generating synchronization references for other equipment. Figure 2 shows the global clock architecture of the SV3C. Shown in the figure is a Measurement System Clocking block that drives the large number of lanes available in the tester. For most applications, all lanes are operated at a single data rate. However, the clock system enables multiple lane clocking configurations depending on the various protocol and multi-site requirements.

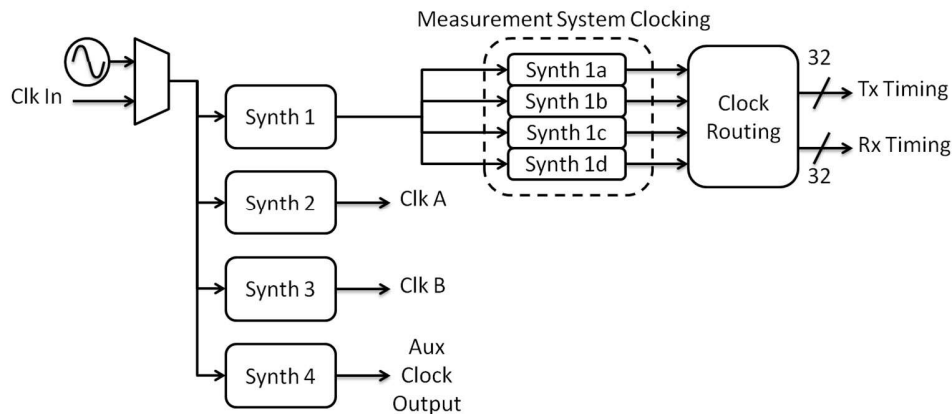


Figure 2 Clock system architecture inside the SV3C.

### Standard Error Detector Analysis

The SV3C instrument has an independent Bit Error Rate Tester (BERT) for each of its input channels. Each BERT compares recovered (retimed) data from a single input channel against a specified data pattern and reports the bit error count.

Apart from error counting, the instrument offers a wide range of measurement and analysis features including:

- Jitter separation
- Eye mask testing
- Voltage level, pre-emphasis level, and signal parameter measurement
- Shmoos of various kinds

Figure 3 illustrates a few of the analysis and reporting features of the SV3C. Starting from the top left and moving in a clock-wise manner, the figure illustrates bathtub acquisition and analysis, waveform capture, raw data viewing, and eye diagram plotting. As always, these analysis options are executed in parallel on all activated lanes.

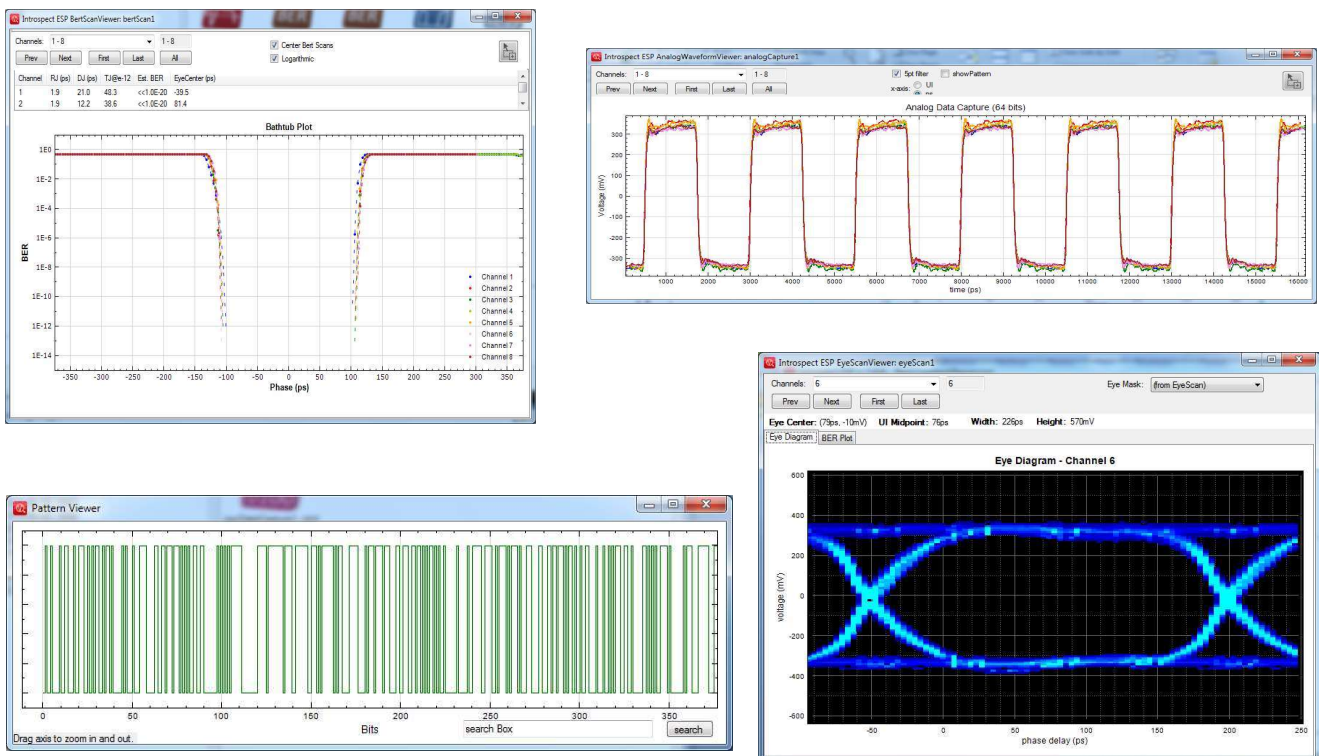


Figure 3 Sampling of analysis and report windows.

## Per-Lane Clock Recovery and Unique Dual-Path Architecture

True to the integrated nature of its design, each SV3C receiver has its own embedded analog clock recovery circuit. That is, 32 individual CDR circuits are monolithically integrated in this miniature test system, thus offering the lowest possible sampling latency in a test and measurement instrument.

The monolithic nature of the SV3C clock recovery helps achieve wide tracking bandwidth for measuring signals that possess spread-spectrum clocking or very high amplitude wander. Figure 4 shows a block diagram of the clock recovery

capability inside the SV3C Personalized SerDes Tester. Also shown in Figure 4 is the dual-path receiver architecture of the SV3C. This unique architecture allows the SV3C to operate as both a digital capture/analysis instrument and an analog measurement instrument. A feature rich clock management system allows for customization of the SV3C to specific customer requirements.

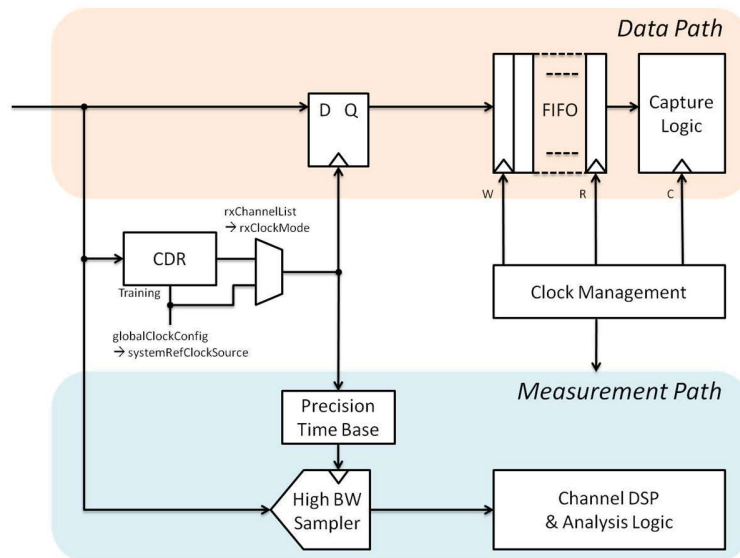


Figure 4 Per-lane clock recovery and dual-path architecture.

## Digital Vector Ports and Utility Power Supply

In order to support test automation and a self-contained bench environment, the SV3C Personalized SerDes Tester includes reconfigurable digital I/O pins for simple device controls or test vector processing. Such processing can include generating simple triggers and flags, controlling device resets and relay matrices, or generating sequenced ATE vector programs. The available I/O pins are customizable on request and can support input, output, single-ended, or differential configurations. Finally, the I/O is exported on two connectors for convenience. A miniature 12-pin ribbon cable connector is provided for rapid prototyping on low-speed signals (Figure 5). A second high-performance Samtec cable connector is also included for a more dense cable interface (Figure 6). Both connectors include a 5V utility supply for powering external adapter boards. Table 1 shows the available number of pins per connector.



Table 1 Low-speed connector pin counts.

	Molex Connector	Samtec Connector
Number of Pins	11	112

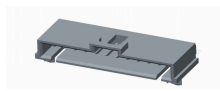


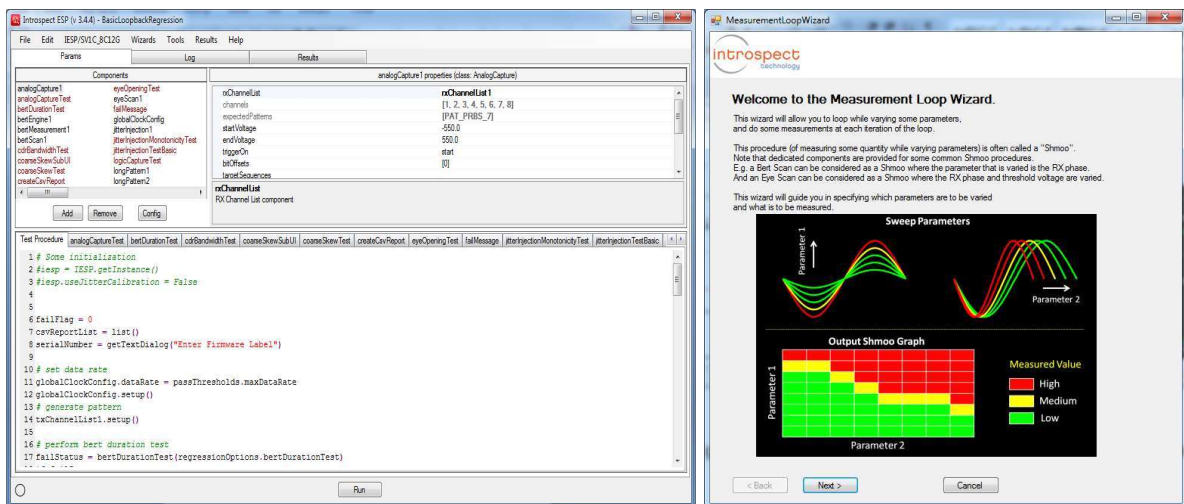
Figure 5 Molex 15-91-2125 ribbon cable connector.



Figure 6 Samtec SEAC high-performance, high-density cable connector.

## Automation

The SV3C is operated using the award winning Introspect ESP Software. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shot in Figure 7(a). Component-based design is Introspect ESP’s way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. For further help, the SV3C features wizard-based code generation for highly automated tasks such as measurement loops (illustrated in Figure 7(b)).



(a)

(b)

Figure 7 Screen captures of Introspect ESP user environment.

# Specifications

Table 2 General Specifications

Parameter	Value	Units	Description and Conditions
<b>Ports</b>			
Number of Differential Transmitters	32		Individually synthesized frequency and output format. Used as external Reference Clock input. Consult user manual for included capability. Contact factory for customization. Consult user manual for included capability. Contact factory for customization.
Number of Differential Receivers	32		
Number of Dedicated Clock Outputs	2		
Number of Dedicated Clock Inputs	1		
Number of Trigger Input Pins	Multiple		
Number of Flag Output Pins	Multiple		
<b>Data Rates and Frequencies</b>			
Minimum Programmable Data Rate	250	Mbps	Contact factory for extension to lower data rates.
Maximum Programmable Data Rate	14	Gbps	
Maximum Data Rate Purchase Options	4	Gbps	
	8.5	Gbps	
	12.5	Gbps	
	14	Gbps	
Data Rate Field Upgrade	4-14	Gbps	Contact factory for details.
Frequency Resolution of Programmed Data Rate	1	kHz	Finer resolution is possible. Contact factory for customization.
Minimum External Input Clock Frequency	25	MHz	
Maximum External Input Clock Frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)
Minimum Output Clock Frequency	10	MHz	
Maximum Output Clock Frequency	250	MHz	
Output Clock Frequency Resolution	1	kHz	
Supported External Input Clock I/O Standards			Support for LVDS, LVPECL, CML, HCSL, and CMOS.

Table 3 Transmitter Characteristics

Parameter	Value	Units	Description and Conditions
<b>Output Coupling</b>			
DC common mode voltage	750	mV	typical (different offsets are firmware programmable)
AC Output Differential Impedance	100	Ohm	typical
<b>Voltage Performance</b>			
Minimum Differential Voltage Swing	20	mV	312.5 Mbps to 5 Gbps, 50 ohm AC coupled termination. 5 Gbps to 12.5 Gbps, 50 ohm AC coupled termination.
Maximum Differential Voltage Swing	1000 800	mVpp mVpp	
Differential Voltage Swing Resolution	20	mV	500 mVpp signal, 20-80%, 50 ohm AC coupled termination.
Accuracy of Differential Voltage Swing	larger of: +/-10% of programmed value, and +/-10mV	%, mV	
Rise and Fall Time	50	ps	
<b>Pre-emphasis Performance</b>			
Pre-Emphasis Pre-Tap Range	-4 to +4	dB	Both high-pass and low-pass functions are available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Pre-Tap Resolution	Range / 32	dB	Only high-pass function is available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Post1-Tap Range	0 to 6	dB	
Pre-Emphasis Post1-Tap Resolution	Range / 32	dB	Both high-pass and low-pass functions are available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Post2-Tap Range	-4 to +4	dB	
Pre-Emphasis Post2-Tap Resolution	Range / 32	dB	
<b>Jitter Performance</b>			
Random Jitter Noise Floor	1	fs	Based on a single-lane measurement with high-bandwidth scope and with first-order clock recovery.
Minimum Frequency of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Frequency of Injected Deterministic Jitter	80	MHz	
Frequency Resolution of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Peak-to-Peak Injected Deterministic Jitter	1400	ps	This specification is separate from low-frequency wander generator and SSC generator.
Magnitude Resolution of Injected Deterministic Jitter	500	fs	Jitter injection is based on multi-resolution synthesizer, so this number is an effective resolution. Internal synthesizer resolution is defined in equivalent number of bits.
Injected Deterministic Jitter Setting	Per-bank		Common across all channels within a bank.
Maximum RMS Random Jitter Injection	0.1	UI	
Magnitude Resolution of Injected Jitter	0.1	ps	

Accuracy of Injected Jitter Magnitude	larger of: +/-10% of programmed value, and +/-10 ps	% , ps	
Injected Random Jitter Setting	Common		Common across all channels within a bank.
<b>Transmitter-to-Transmitter Skew Performance</b>			
Lane to Lane Integer-UI Minimum Skew	-20	UI	
Lane to Lane Integer-UI Maximum Skew	20	UI	
Effect of Skew Adjustment on Jitter Injection	None		
Lane to Lane Skew	+/- 30	ps	

Table 4 Receiver Characteristics

Parameter	Value	Units	Description and Conditions
<b>Input Coupling</b>			
AC Input Differential Impedance	100	Ohm	
<b>AC Performance</b>			
Minimum Detectable Differential Voltage	25	mV	
Maximum Allowable Differential Voltage	2000	mV	
Minimum Programmable Comparator Threshold Voltage	-550	mV	
Maximum Programmable Comparator Threshold Voltage	+550	mV	
Differential Comparator Threshold Voltage Resolution	10	mV	
Differential Comparator Threshold Voltage Accuracy	larger of: +/-10% of programmed value, and +/- 10mV	%, mV	
Measured Eye Width Accuracy	10%		Maximum error, 312.5 Mbps – 2.0 Gbps, 200 mVpp minimum input amplitude Maximum error, 2.0 Mbps - 5 Gbps, 200 mVpp minimum input amplitude Maximum error, 5 Gbps – 12.5 Gbps, 200 mVpp minimum input amplitude
	15%		
	25%		
<b>Resolution Enhancement &amp; Equalization</b>			
DC Gain	0	dB	
	2	dB	
	4	dB	
	6	dB	
	8	dB	
CTLE Maximum Gain	16	dB	
CTLE Resolution	1	dB	
DC Gain Control	Per-receiver		
Equalization Control	Per-receiver		
<b>Jitter Performance</b>			
Input Jitter Noise Floor in System Reference Mode	25	ps	Based on a single-lane measurement.

Input Jitter Noise Floor in Extracted Clock Mode	10	ps	Based on a single-lane measurement.
<b>Timing Generator Performance</b>			
Resolution at Maximum Data Rate	31.25	mUI	Resolution (as a percentage of UI) improves for lower data rates. Contact factory for details.
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error Range	+/- 5 Unlimited	ps	
<b>Skew</b>			
Lane to Lane Skew Measurement Accuracy	+/- 10	ps	

Table 5 Clocking Characteristics

Parameter	Value	Units	Description and Conditions
<b>Internal Time Base</b>			
Number of Internal Frequency References	5		Standard configuration creates one measurement path frequency reference, two output clock frequency references. Contact factory for clock domain customization.
<b>Embedded Clock Applications</b>			
Transmit Timing Modes	System Extracted		Clock can be extracted from one of the data receiver channels in order to drive all transmitter channels.
Receive Timing Modes	System Extracted		
Lane to Lane Tracking Bandwidth	4	MHz	All channels have clock recovery for extracted mode operation.
Single-Lane CDR Tracking Bandwidth	3 - 12	MHz	
<b>Forwarded Clock Applications</b>			
Transmit Timing Modes	System Forwarded		Contact factory for forwarded clock routing recommendations.
Receive Timing Modes	System Forwarded		Contact factory for forwarded clock routing recommendations.
Clock Tracking Bandwidth	4	MHz	Second order critically damped response.
<b>Spread Spectrum Support</b>			
Receive Lanes Track SSC Data	Yes		Requires operation in extracted clock mode.
Transmit Lanes Generate SSC Data	Yes		
Minimum Spread	0.1	%	
Maximum Spread	2	%	
Spread Programming Resolution	0.01	%	
Minimum Spreading Frequency	31.5	kHz	
Maximum Spreading Frequency	63	kHz	

Table 6 Pattern Handling Characteristics

Parameter	Value	Units	Description and Conditions
<b>Loopback</b>			
Rx to Tx Loopback Capability	Per channel		
Lane to Lane Latency Mismatch	0	UI	
<b>Preset Patterns</b>			
Standard Built-In Patterns	All Zeros D21.5 K28.5 K28.7 DIV.16 DIV.20 DIV.40 DIV.50 PRBS.5 PRBS.7 PRBS.9 PRBS.11 PRBS.13 PRBS.15 PRBS.21 PRBS.23 PRBS.31		
Pattern Choice per Transmit Channel	Per-transmitter		
Pattern Choice per Receive Channel	Per-receiver		
BERT Comparison Mode	Automatic seed generation for PRBS		Automatically aligns to PRBS data patterns.
<b>User-programmable Pattern Memory</b>			
Total Available Memory	4	GByte	Memory allocation is customizable. Contact factory.
Individual Force Pattern	Per-transmitter		
Individual Expected Pattern	Per-receiver		
Minimum Pattern Segment Size	512	bits	
Maximum Pattern Segment Size	Unlimited	bits	Up to memory capacity
Total Memory Space for Transmitters	1	GByte	Memory allocation is customizable. Contact factory.
Total Expected Memory Space for Receivers	1	GByte	Memory allocation is customizable. Contact factory.
<b>Pattern Sequencing</b>			
Sequence Control	Loop infinite Loop on count Play to end		
Number of Sequencer Slots per Pattern Generator	16		This refers to the number of sequencer slots that can operate at any given time. The instrument has storage space for 16 different sequencer programs.
Maximum Loop Count per Sequencer Slot	$2^{16} - 1$		
<b>Additional Pattern Characteristics</b>			
Pattern Switching	Wait to end of segment Immediate		When sourcing PRBS patterns, this option does not exist.
Raw Data Capture Length	8192	bits	Memory allocation is customizable. Contact factory.

Table 7 Instruction Sequence Cache

Parameter	Value	Units	Description and Conditions
<b>Simple Instruction Cache</b>			
Instruction Learn mode Instruction	Start Stop Replay		
<b>Advanced Instruction Cache</b>			
Local Instruction Storage	1M Instructions		
Instruction Sequence Segments	1000		

Table 8 DUT Control Capabilities

Parameter	Value	Units	Description and Conditions
<b>DUT IEEE-1149-1 (JTAG) Port (Option)</b>			
JTAG-Port Transmit Signals	TCK TRST TDI		
JTAG-Port Receive Signals	TDO		
JTAG-Port Transmit Voltage Swing (Fixed)	0 to 2.5	V	
JTAG-Port Receive Max Voltage Swing	0 to 2.5	V	
TDI Bit Memory	4k		
TDO Bit Memory	4k		
<b>DUT SPI Port (Option)</b>			
SPI Signals	SCLK SSN MISO MOSI		
Voltage Swing (Fixed)	0 to 2.5	V	

<b>Revision Number</b>	<b>History</b>	<b>Date</b>
<b>1.0</b>	Document release	August 1, 2014
<b>1.1</b>	Updated specifications tables; removed measurement throughput characteristics	August 14, 2014
<b>1.2</b>	Updated document template; updated specifications related to memory depth	April 13, 2017

The information in this document is subject to change without notice and should not be construed as a commitment by Introspect Technology. While reasonable precautions have been taken, Introspect Technology assumes no responsibility for any errors that may appear in this document.



© Introspect Technology, 2017  
Published on April 13, 2017  
EN-D013E-E-1703