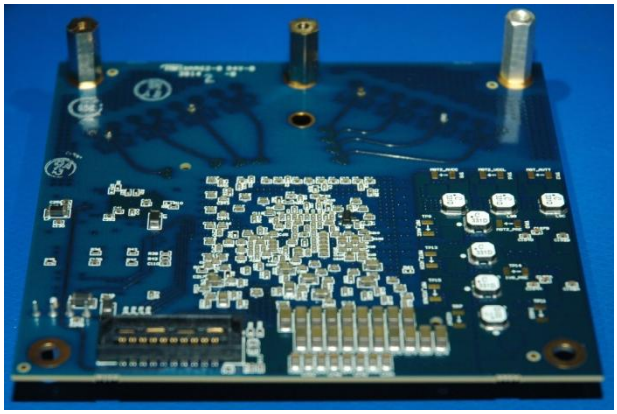
SV2D SerDes Transceiver Endpoint

Product Brief

28 Gbps, 8 Lane SerDes Tester in a Plug-In Module Form Factor

Top View



Bottom View

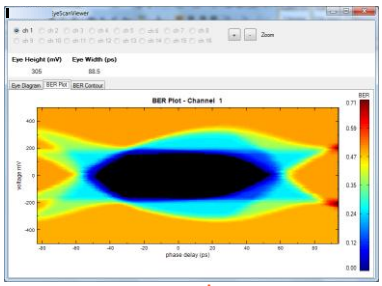
Highly-integrated 28 Gbps parallel tester that mounts directly on an application or test board and that operates through pin-controlled register commands. Featuring eight independent receivers and transmitters, the SV2D satisfies a growing need for parallel, system-oriented testing methodology that closely mimics the final application of the device under test.

Key Features:

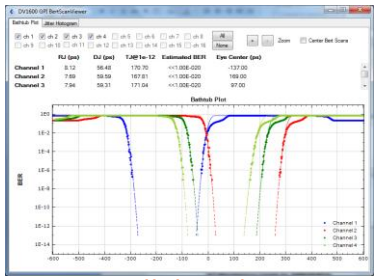
- **Data rates:** 19 Gbps to 28 Gbps fully-continuous operating range.
- **Lanes:** 8 Tx and 8 Rx, differential with per channel adjustment of voltage and timing.
- **DUT Tx/Rx measurements:** eye diagram, EQ, jitter, voltage sensitivity.
- **Ease of integration:** direct attachment with standard, high-performance connectors. Single 12-V DC power supply with internal regulation.
- **Ultra compact size:** 3.4” x 3.25” for placement in dense test boards.

Key Benefits:

- **Parallel:** a truly parallel system allows for the most comprehensive “stress test” that is possible. The SV2D tests complete 28 Gbps links simultaneously.
- **Self Contained:** an all-in-one system reduces space and helps create a compact tester-on-board solution.
- **Automation:** Scripting capability is ideal for debug tasks, verification and full-fledged production screening.



BER Plot



Parallel Analysis

Pattern Generator Functions

Feature	Description	Benefit
Pattern Generators	Per lane pre-built patterns, PRBS (5, 7, 9, 11, 15, 23, 31), custom user-defined pattern (up to 2 Mb), nested pattern sequencers (up to 16 sequencer programs)	Allows for flexible stimulus generation (e.g. training sequences or compliance patterns)
Analog Controls	Per lane, polarity inversion, voltage swing, 3-tap transmit pre-emphasis, bit-slip up to +/- 20 UI	Provides deep receiver stress characterization with truly independent multi-variable analysis

BERT and Scope Functions

Feature	Description	Benefit
Error Detectors	BERT engines work with all types of patterns listed under Pattern Generator section; single-shot (up to 2^{32} cycles) or continuous error counting modes; 32-bit error counters; automatic pattern alignment	Optimized architecture for production testing and data collection, ensuring rapid pattern alignment and error checking
Equalizer Control	Per lane continuous-time linear equalizers	Allows for design exploration, de-embedding, and correlation with simulation
Clock Recovery	Per-lane analog, hardware clock recovery unit with optimized connection to sampling circuitry	Offers a realistic test environment on any production ATE load board
Analysis Capability	Identify pattern; BERT measurement; BERT scan; eye diagram; analog waveform capture; jitter separation; transition & non-transition eyes	Rapid signal integrity analysis functions behind each transceiver channel

Lanes and Clocking

Feature	Description	Benefit
Lane Count	8 independent generator channels; 8 independent analyzer channels	Allows for truly parallel test
Clock Generators	Two programmable sub-rate clocks	Allows for synchronization with device
Clock References	Internal oscillator (no external clock) or external clock reference with built-in jitter cleaning	Allows for operating the SV2D as a synchronization master or as a syncronization slave

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