Using the SV5C 32 Channel DDR Form Factor

SV5C Personalized SerDes Tester

C SERIES

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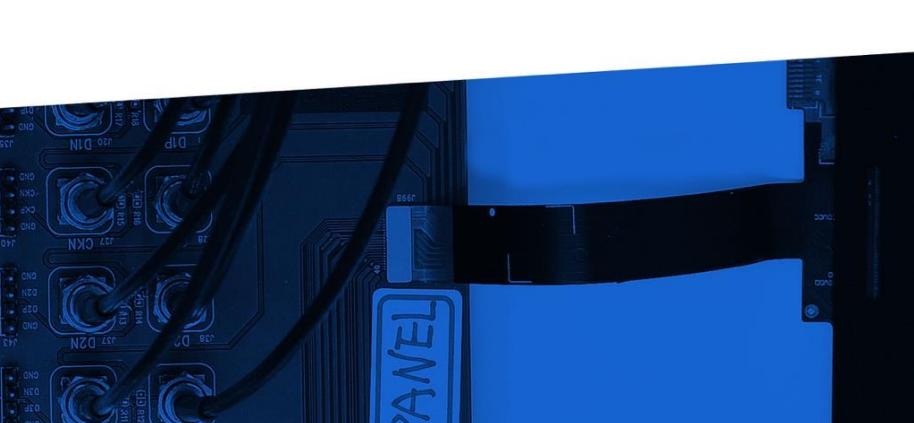
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Introduction

OVERVIEW

This document describes the required steps for combining two SV5C devices into a single, unified form factor. This form factor, SV5C_32C12G_DDR, is a superset of the SV5C_16C12G_DDR form factor and provides 32 phase aligned transmitter channels. The hardware requirements are given below.

REQUIREMENTS

- (QTY = 2) SV5C Personalized SerDes Testers
- (QTY = 2) 12 V power supply units (part number XP Power AHE220PS12)
- (QTY = 2) USB cables for connection between each SV5C and a PC (included with SV5C)
- (QTY = 4) 12 inch phase-matched cables, SMP female to SMP female (manufacturer part number Amphenol SV Microwave 7012-1292, or contact Introspect)
- (QTY = 2) 6 inch jumper wire, female to female 28AWG (example manufacturer part number Adafruit Industries # 1950)

> **IMPORTANT NOTE**
>
> For fully phase aligned operation across all 32 TX channels, a calibration must be performed on the two SV5C modules. This calibration may be performed in the factory before shipment of a pair of units, or it may be performed "in-field". Please refer to the document "EN-G034E-E-21272 SV5C In-Field Calibration Scripts" for in-field calibration instructions.

Step by Step Guide

CUSTOM FORM FACTOR CREATION

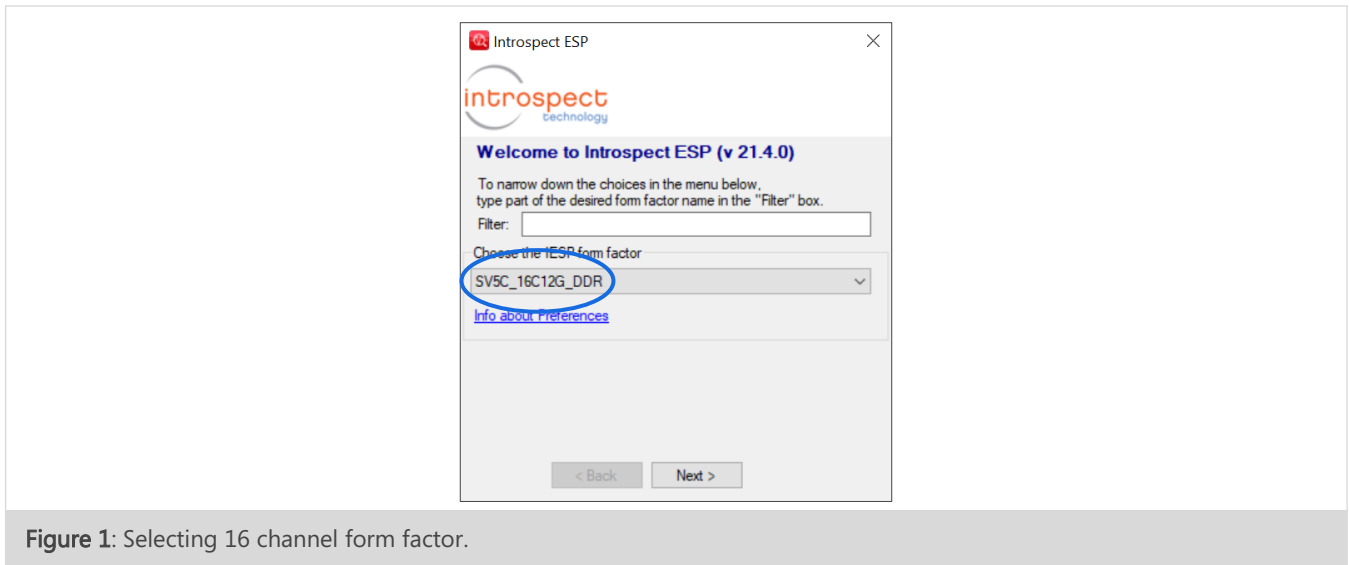1. Open the GUI with the SV5C_16C12G_DDR form factor, as shown in Figure 1.

Figure 1: Selecting 16 channel form factor.

2. Connect the USB cable from your PC to the first SV5C (referred to here as "Box 1"). After connecting to Box 1 via the Introspect GUI (IESP/SV5C_16C12G_DDR -> Connect), you will see serial numbers in the log, like those shown below:

```
Connecting to serialNum 'FTDI:INSV5M20050020A'
Connected to subPart 'SV5C_16C12G_DDR_A'
Connecting to serialNum 'FTDI:INSV5M20050020B'
Initializing IESP hardware/firmware
Doing post-connection initialization
```

3. Connect the USB cables from your PC to both SV5C boxes and open the GUI with the SV5C_32C12G_DDR form factor.

4. Open the "ConnectionConfig" tool (IESP/SV5C_32C12G_DDR -> ConnectionConfig). Select the FtdiSerialNumber for box 1 to be the number recorded in step 2, and use the other option in the drop-down menu for box 2, as shown in Figure 2:
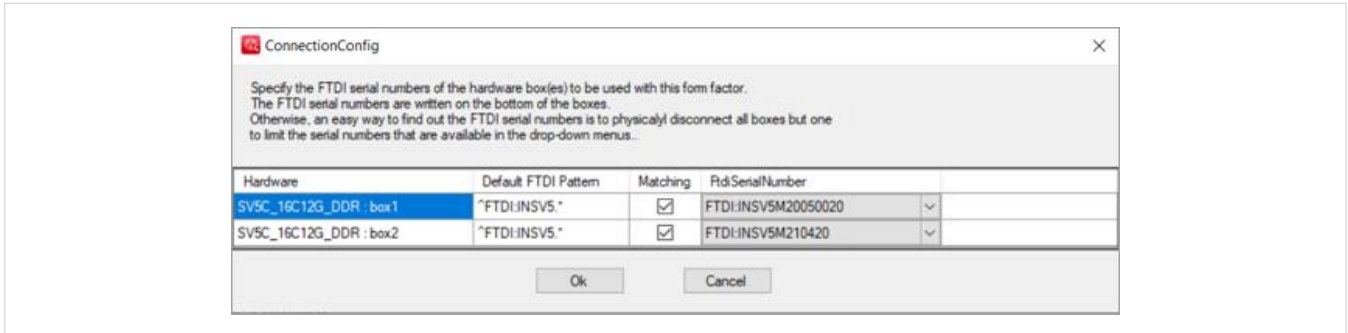

Figure 2: Adding serial numbers to 32 channel form factor.

5. Close the "ConnectionConfig" tool and connect to both SV5C boxes (IESP/SV5C_32C12G_DDR -> Connect). You should see a successful connection to both boxes like below.

```
Connecting to serialNum 'FTDI:INSV5M20050020A'
Connected to subPart 'SV5C_16C12G_DDR_box1_A'
Connecting to serialNum 'FTDI:INSV5M20050020B'
Connecting to serialNum 'FTDI:INSV5M210420A'
Connected to subPart 'SV5C_16C12G_DDR_box2_A'
Connecting to serialNum 'FTDI:INSV5M210420B'
Initializing IESP hardware/firmware
Doing post-connection initialization
```

SV5C CONNECTION DIAGRAMS

Diagrams showing the required connections of the two modules are given in the figure below. Figure 3(a) shows the full set of cable connections between Box 1 and Box 2. In addition to the reference clock connections, three sets of cable connections (one SMP pair, two GPIO jumper wires, and USB connections to the PC) are made on the left side of each SV5C, and the connection ports on this side are shown in Figure 3(b). Detailed connections for GPIO pins via jumper wires are shown Figure 3(c).
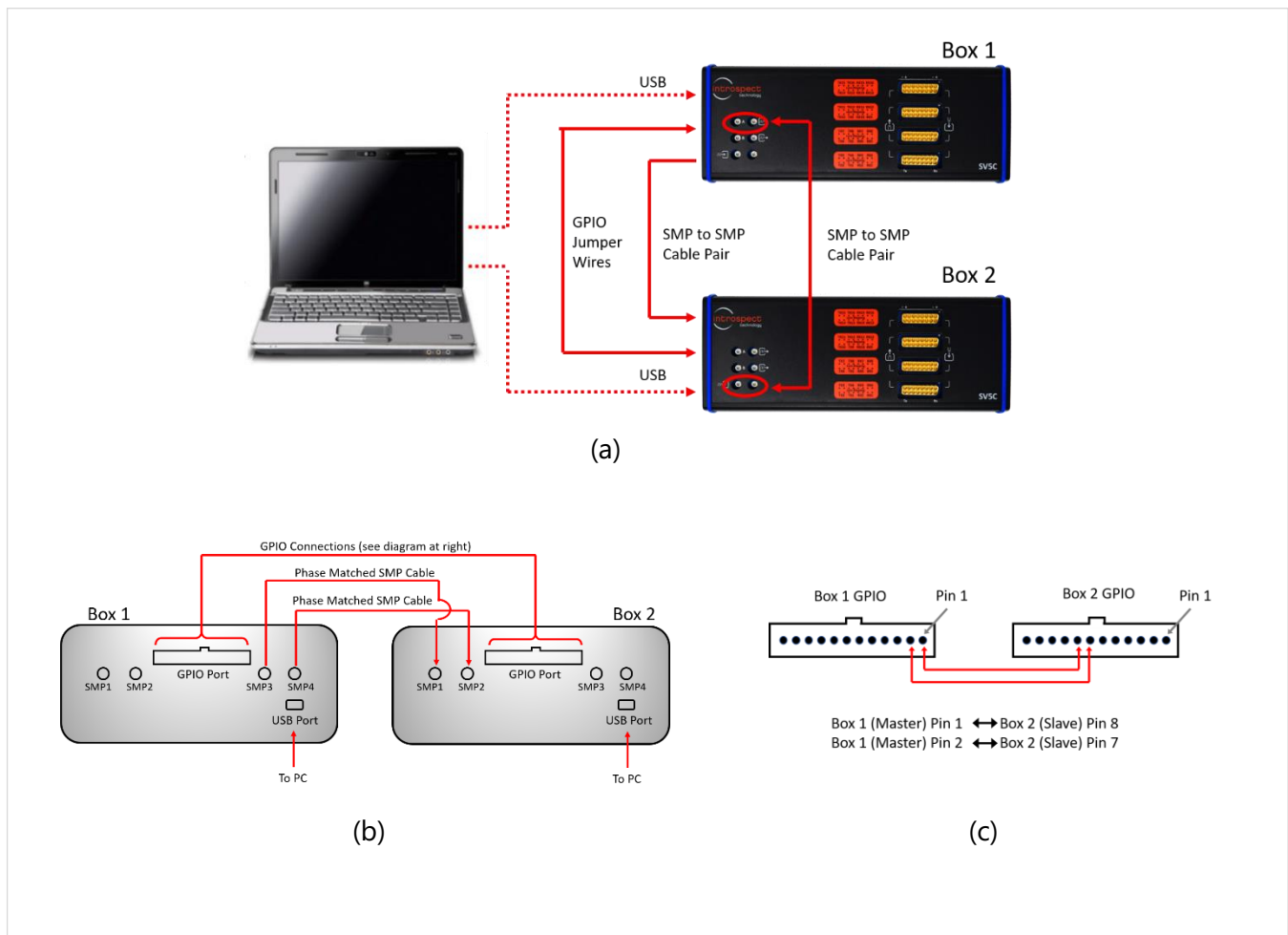

Figure 3: (a) Block diagram of required cable connections between SV5C modules (b) diagram of SV5C side connectors and required connections (c) pin diagram of SV5C side connector and GPIO jumper wire connections.

USING THE SV5C_32C12G_DDR FORM FACTOR

Open a new test procedure with the SV5C_32C12G_DDR form factor. In the new form factor, under globalClockConfig, you will see that two "referenceClocksConfig" components have automatically been created. This is as shown in the screen capture in Figure 4.

Note that the "refClocksConfig1" component controls "Box 1" has been configured to use its internal "systemRefClockSource" while the "refClocksConfig2" component controls "Box 2" has been configured to use an external reference clock provided by "Box 1". This matches the cable setup as shown in Figure 3(a).
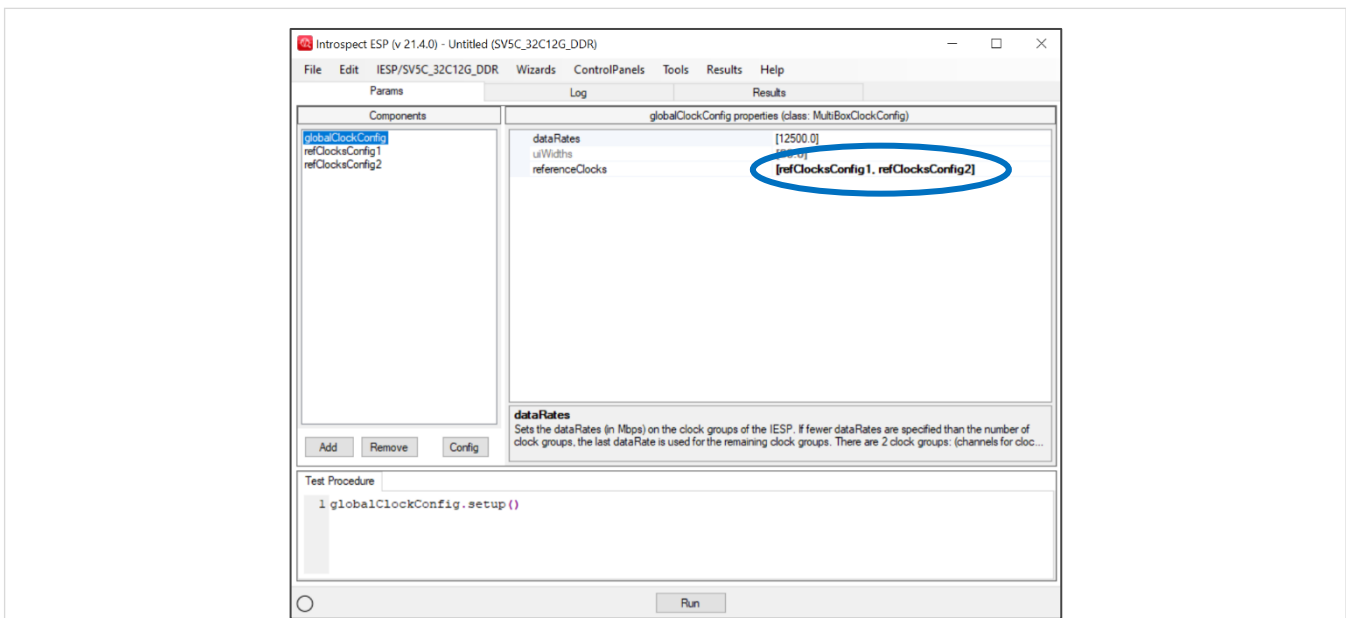

Figure 4: Reference clock component setup for 32 channel form factor.

Edit the "dataRates" attribute to include 2 dataRates as shown below. The "uiWidths" attribute will update automatically, as displayed in Figure 5.
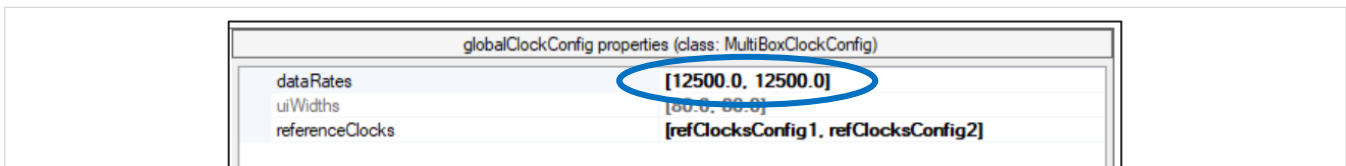

Figure 5: Data rate setting for 32 channel form factor.

Under the "components" window pane, press "Add" and add a "txChannelList" component. Once added, you may change the number of channels to the full range of 1-32. This is as shown in the screen capture in Figure 6. Note that channels 1-16 are on "Box 1", and channels 17-32 are on "Box 2".
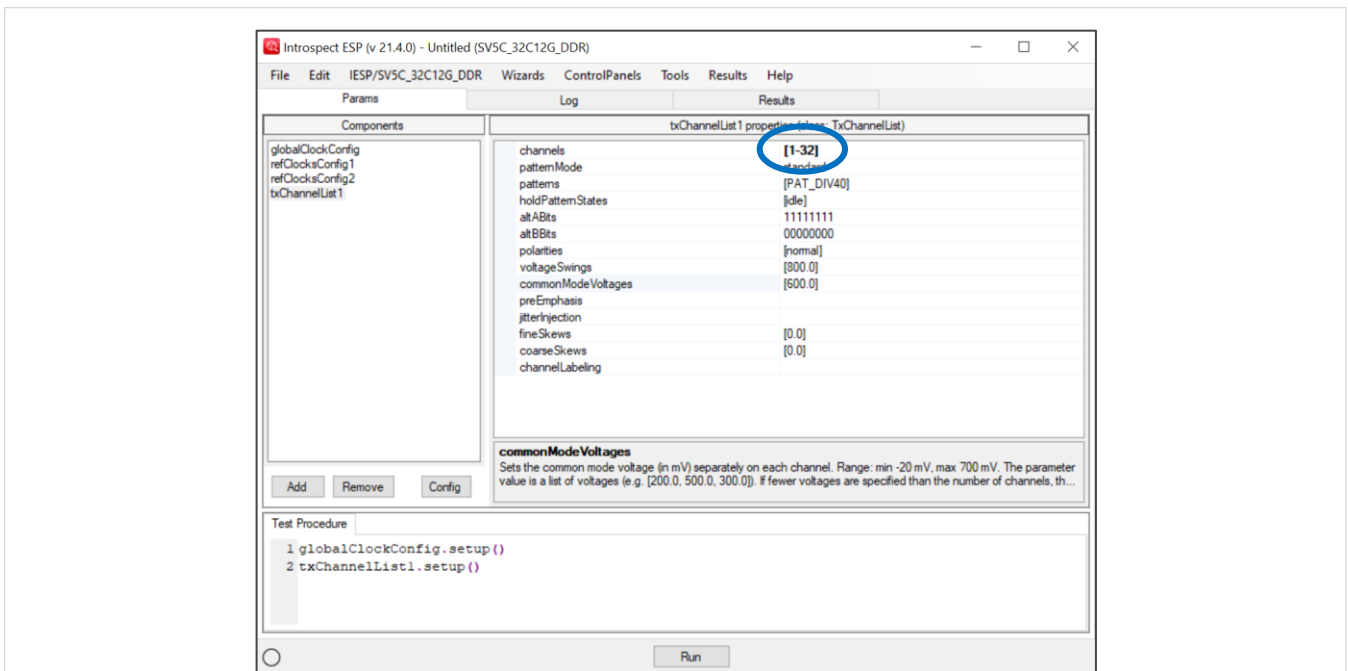

Figure 6: Tx channel setting for 32 channel form factor.

All other operations for the form factor SV5C_32C12G_DDR may be used as in the previous 16 channel form factor. Existing test procedures developed for the 16 channel form factor may be imported and channel lists modified as required.

IMPORTANT NOTE

If phase alignment across all 32 TX channels has been performed as in the in-field calibration document (see "EN-G034E-E-21272 SV5C In-Field Calibration Scripts"), then it is important to externally label the first SV5C unit (master) as "Box 1" and the second unit (slave) as "Box 2". This labelling must be kept consistent during subsequent usage. TX Channels 1-32, as shown in the channel list above, will not be aligned if the order of Box 1 and Box 2 is changed.

Revision Number	History	Date
1.0	Document release	June 10, 2020
1.1	Update custom form factor creation steps	September 13, 2021

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