Functionally Testing a DDR5 DIMM Is Not Difficult, but It Is Complicated!

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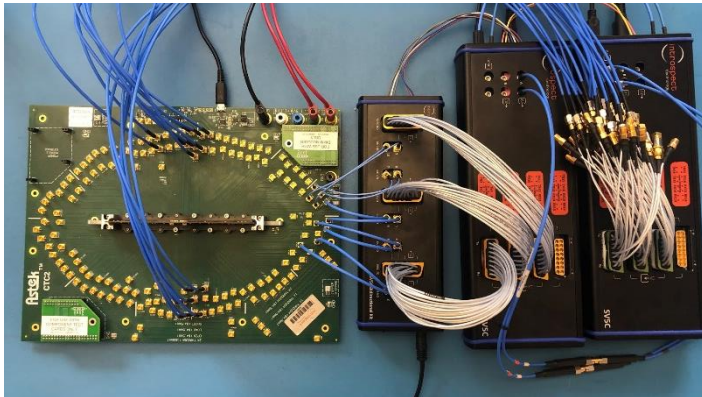# Table of Contents

Introduction

Double Data Rate (DDR) technology is a memory chip technology that is pervasively used in server and data center applications as well as in personal computers and gaming stations. Featuring high memory density and memory capacity as well as ever increasing transfer speeds, this technology has become critical to the deployment of high-performance computers, AI processors, and edge computers in data centers. And now as it enters its fifth (5th) generation in the form of the JEDEC DDR5 standard, this technology poses unique development challenges for memory module manufacturers as well as server manufacturers and system integrators. The primary reason for this is that DDR5 has introduced several new features to enable very high speed operation, including link equalization and highly sophisticated training algorithms.

This white paper introduces some of the challenges associated with testing memory modules based on the DDR5 standard. Specifically, we focus on the **functional test** aspect: that is, how to make certain that the memories function properly when written to and read from over the DDR5 interface. As will be shown, achieving a functional test entails overcoming several hurdles related to the increased data rates, additional protocol complexities, and higher densities. Subsequently, we describe Introspect Technology's **ATE-on-Bench** solution consisting of the SV5C Personalized SerDes Test System and illustrate how it is used to emulate a complete memory controller, albeit within a context that offers visibility into and control over the inner workings of the DDR5 state machines. Through the SV5C DIMM Test Suites, **virtual memory controllers** can be implemented and customized through Python programming. We then describe examples of how the device initialization steps and training algorithms are sequenced before functional read/write operations can be performed.

Functional Test Challenges

The following is a summary of new challenges that have been introduced by the DDR5 standard.

INCREASED SPEEDS

Unlike legacy DDR implementations, it is no longer possible to simply define a setup and hold time in the memory controller and expect memory read/write operations to be error free. Instead, DDR5 now defines statistical performance parameters such as bit error rate and eye diagram statistics. Additionally,

DDR5 links are expected to operate over printed circuit board (PCB) channels that result in closed eye diagrams, thus mandating advanced training algorithms.

ADDITIONAL PROTOCOL COMPLEXITY

The above training algorithms are all implemented by new protocol requirements to ensure a proper handshake between memory controllers and memory modules connected to them. Simply stated, it is no longer possible to power up a memory module and expect to perform read/write transactions with it. Rather, designers must now factor in protocol conformance in their shipped modules.

Because of all this protocol complexity, it is very important for DIMM manufacturers and memory controllers alike to have access to a third-party test instrument that can perform functional testing and that can provide enough granularity to modify and customize the training algorithms used in the DDR5 state machine.

HIGHER MEMORY DENSITIES

Naturally, since DDR5 memory modules now support higher memory capacity, testing them needs to be more exhaustive than in previous generations. That is, more read/write transactions are required to perform a full scan of the memory under test. Any functional test system is required to be able to do such memory scans either algorithmically or through banks of test pattern data.

Hardware Connection Diagram

Figure 1 shows a schematic representation of the hardware connections between a memory module under test and the SV5C **ATE-on-Bench** system. As can be seen, multiple SV5C modules can be combined to create a wide bus application. Additionally, the test system contains a Bidirectional Communications Kit (BDK), which is used for the data and strobe signals on the DIMM.

Figure 2 shows a photograph of the setup. As can be seen, the SV5C system offers a very compact solution that can sit right next to a DIMM under test. In this figure, the DIMM under test is placed on a CTC2 board that is defined by JEDEC, which allows for easy access to all signals on the DIMM.
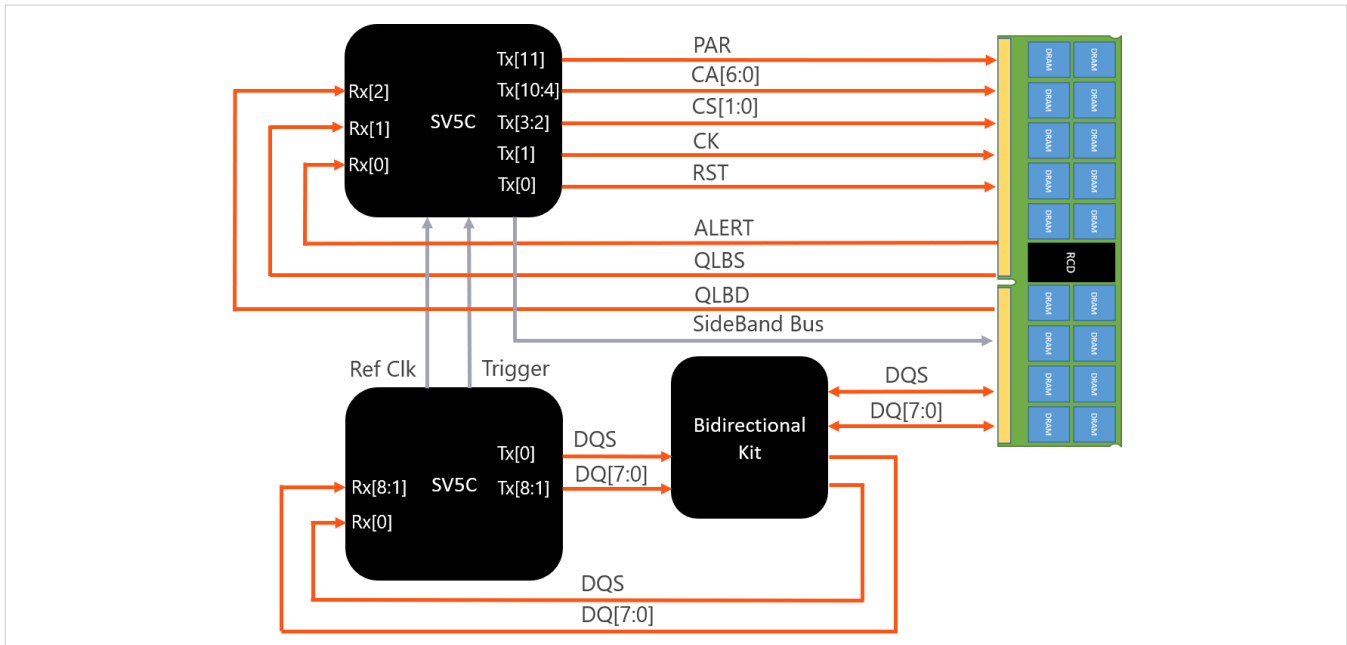
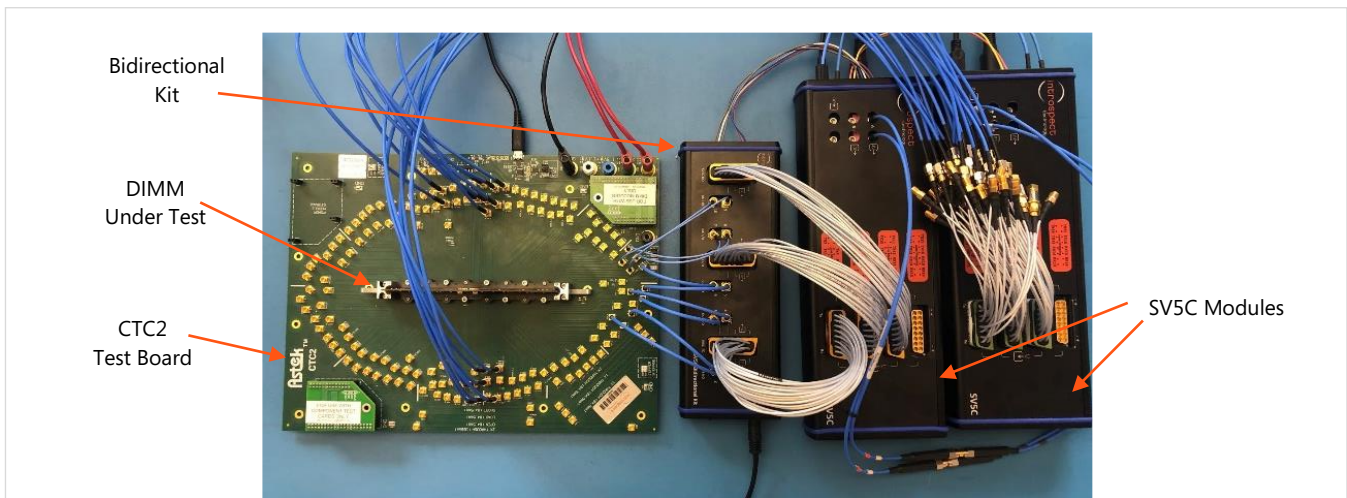**Figure 1:** Connection diagram for functional testing of a DDR5 RDIMM.

Figure 2: Photograph illustrating a real RDIMM setup where the RDIMM under test is placed on a CTC2 test board.

Introspect's Test Suite Concepts

The Test Suite software interface for the SV5C system offers Python functions representing different states in the DDR5 state diagram as well as states related to test system initialization and programming. The following sections describe how a memory controller is constructed using this interface, and they also show example transitions to go from training to functional read/write transactions.

DDR5 STATE DIAGRAMS AND THE VIRTUAL MEMORY CONTROLLER

Figure 3 shows the basic state diagram for the SV5C DIMM Test Suite. As can be seen, it mirrors very closely the state diagram for a typical memory controller. This is why it is referred to as a virtual memory controller in the context of this white paper.

In addition to the DDR5 states themselves, this figure shows states related to the SV5C test system. For example, the top left state is used to initialize the SV5C and program its data rate, among other things. Similarly, in the top right state, the SV5C can be programmed to change operating data rate without disrupting the DDR5 state diagram. All actions in the Test Suites can transition to the Idle state, thus keeping the DDR5 link active at all times with Deselect (DES) commands on the bus, just like in a real memory controller.
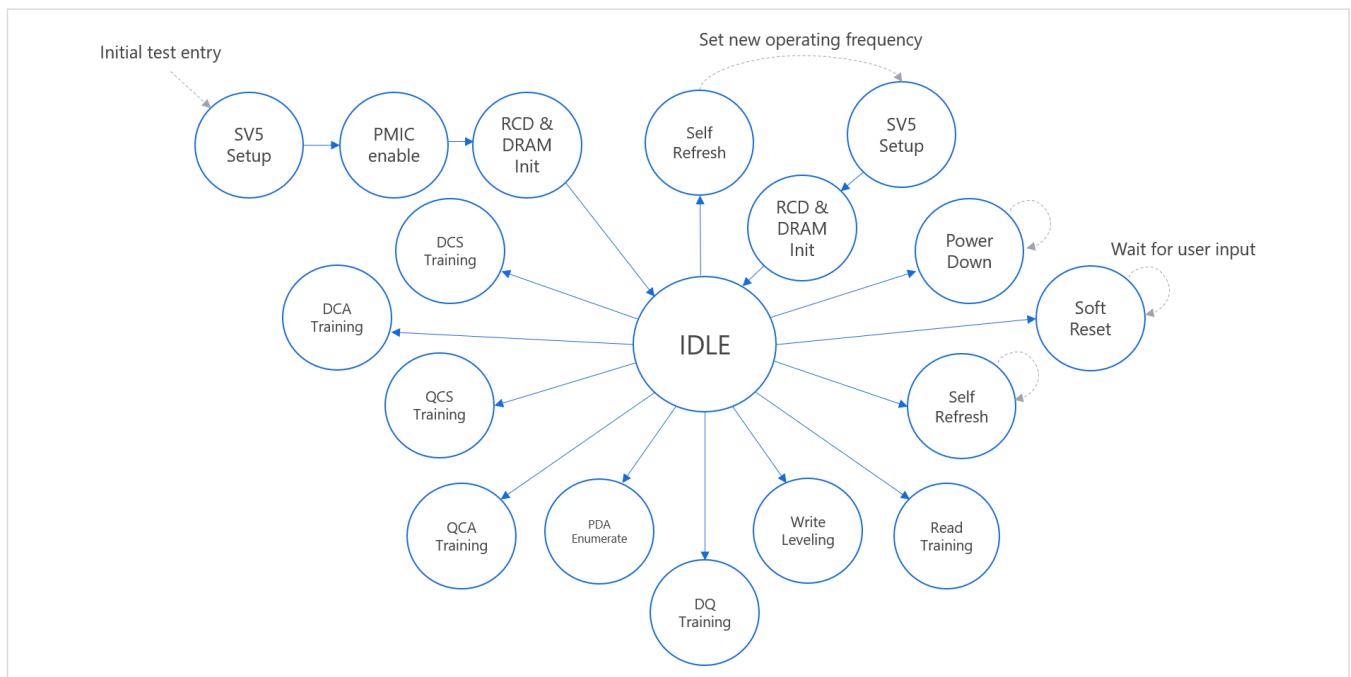

Figure 3: Introspect's Test Suite state diagram representation for DDR5 DIMM functional testing.

TRANSITIONING BETWEEN TRAINING STATES AND FUNCTIONAL STATES

Figure 4 shows how a DIMM under test can be transitioned to performing memory read/write test loops. Specifically, a single Python function can be added to the Test Suite, and this Python function would contain all of the memory test code. Importantly, this function attaches to the original state diagram of Figure 3 without requiring knowledge of the entire memory controller design.

The ability to add tests on top of the pre-built basic test cases is one of the most important features of the SV5C test system for DIMM testing. It means that the user can focus on the task at hand – writing to and reading from the memory – without having to worry about the details of the DDR5 state diagram, which include training, write leveling, and enumeration.
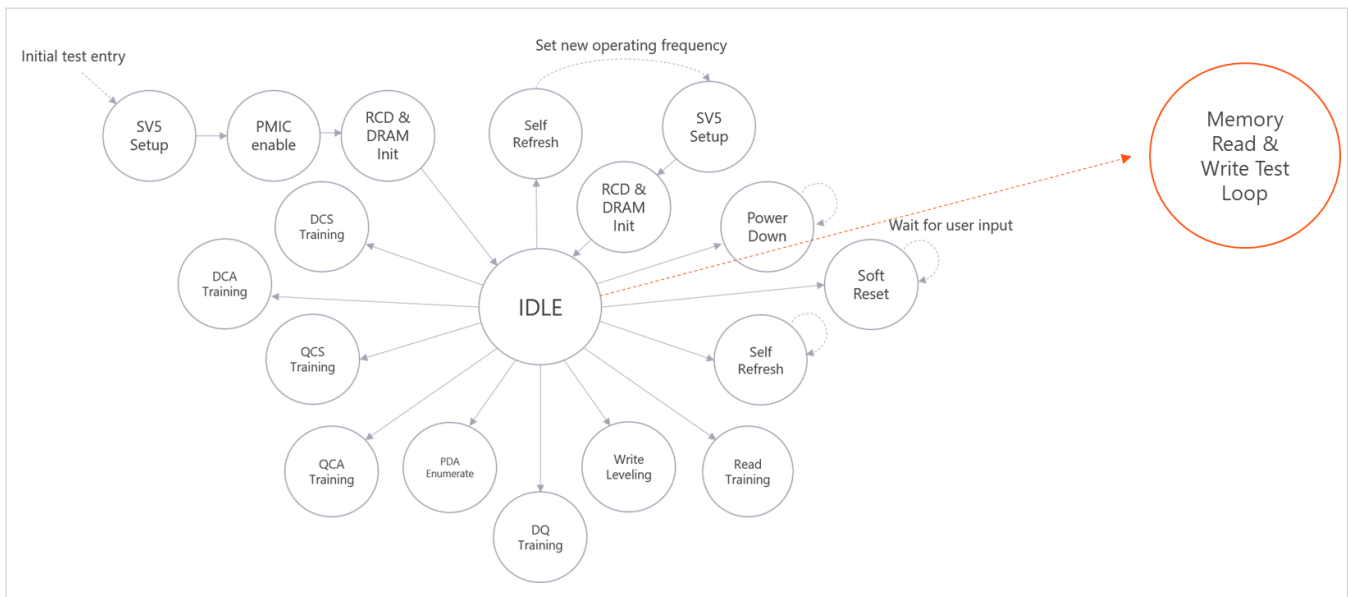

Figure 4: Once in a stable state, the DIMM under test can be transitioned to a memory read/write test loop.

EXAMPLE FLOW FROM INITIALIZATION TO MEMORY ACCESS

Finally, Figure 5 shows the complete flow from device initialization to performing memory read and write transactions. As can be seen, a lot of complicated steps are required. For the novice user or the one who is more interested in the memory array itself, these steps can be performed automatically by the SV5C test system. Additionally, the SV5C can store previously acquired training data, thus simplifying the execution even further.
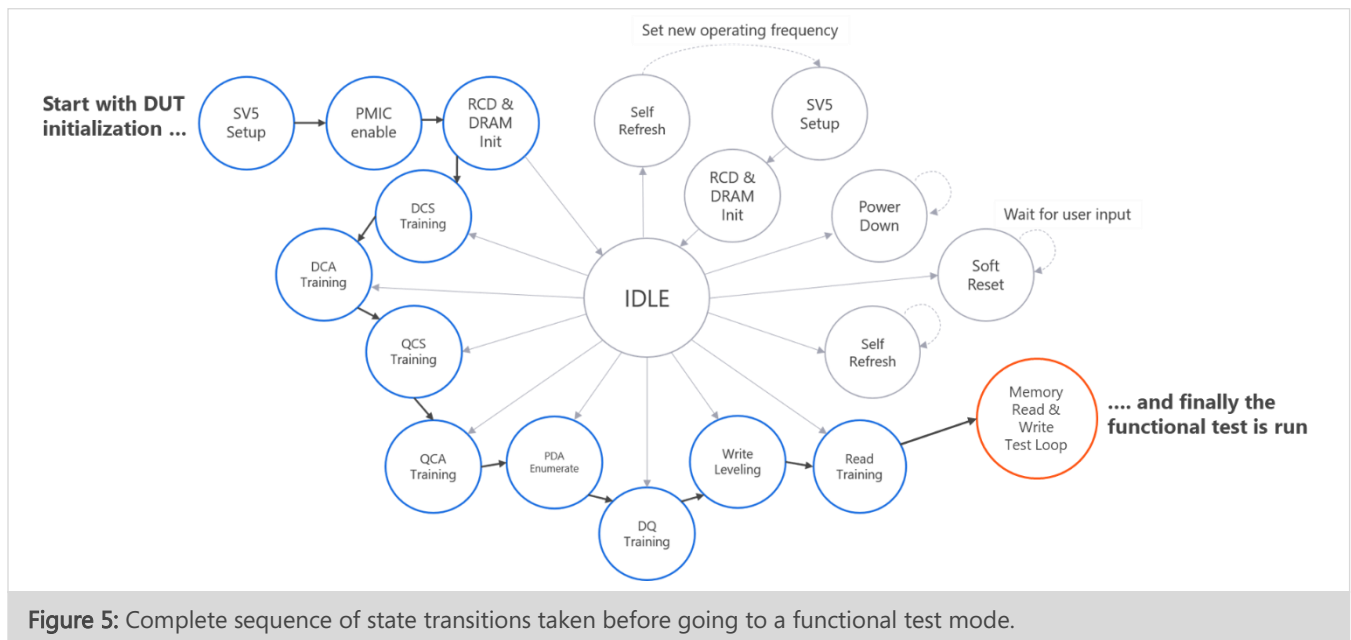

Figure 5: Complete sequence of state transitions taken before going to a functional test mode.

Conclusion

This white paper introduced some of the challenges associated with testing memory modules based on the DDR5 standard. We focused on the **functional test** aspect, and we described how some of the apparent complications associated with this new, high-performance standard can be solved when functionally testing DDR5 DIMMs. We showed that while the training sequences of the memory controller state diagram can be quite complicated, the SV5C **ATE-on-Bench** solution enables automatically sequencing a DIMM under test from initialization all the way to a state where memory read and write transactions can be performed.

To Learn More

The following is a list of recommended equipment for DDR5 functional testing:

- SV5C Personalized SerDes Tester
- SV5C Bidirectional Kit
- Introspect ESP Software
- Introspect Test Suite Software

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1.0	Document Release	October 12, 2020

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