SerialTek Kodiak™
Next-Generation Gen4 PCIe/NVMe Analyzer

SerialTek
an ellisys company

Technical Specifications

Kodiak Enclosure

- Dimensions: 443 x 67 x 305 mm (17 x 2.6 x 12")
- Weight: 7 kg (15 lbs)
- Mounting: 19" Rack Mount Option, Tilt Feet Option
- Ambient Operating Temperature: 5-35°C at up to 2133m (7000 feet) altitude

Displays and Indicators

- Front Panel LCD: 800x320 4.6" WCGA, Touchscreen
- System Status: RGB LED

Front-Panel Connectors

- Interposer Connection: 4x SFF-8644
- Ethernet (10 GbE): 2x SFP+ (10 GbE)
- Ethernet (1 GbE): RJ45
- PCIe Interface: 2x OCuLink
- USB Interface: 2x USB 3.1 Type A

Rear-Panel Connectors

- Power: IEC C13, 90-264 Vac, 47-63 Hz
- Clock Out: SMA, 50 Ω, 3.3 Vdc, 10 MHz
- Clock In (10 MHz): SMA, 50 Ω, 3.3 Vdc, 10 MHz
- Trigger Out: SMA, 50 Ω, 3.3 Vdc
- Trigger In: SMA, 50 Ω, 3.3 Vdc
- Maintenance: RJ45, USB Micro-B (Not for customer use)

Interposer Power Unit (Common)

- Input: 100-240 Vac/50-60 Hz
- Output: 5 Vdc
- Power: 50 W
- Plug: Molex 039-01-2060
- Safety: UL, CUL, CE, TUV-GS, PSE
- EMI: CE, FCC
- Environmental: ROHS, WEEE, VI

M.2 Interposer

- Dimensions: 154 mm(W) x 34 mm(H) x 232 mm(L) (6 x 1.3 x 9")
- Power connector: Molex 87427-0602
- Analyzer connectors: 2x SFF-8644
- Device connector: M.2 Socket 3, Key M, 22110, 2280, 2260, 2242, 2230
- Host module connectors: 2x MCIO 38 pin
- SMBUS injection connector: 2x5 pin 0.1" header, 3.3 Vdc
- REFCLK output connectors: 2x U.FL, AC coupled LPHCSL
- REFCLK output control connector: 2 pin 0.1" header, 3.3 Vdc
- REFCLK buffer control connector: 3 pin 0.1" header, 3.3 Vdc
- Sideband signal access connector: 2x9 pin 0.1" header, 3.3 Vdc

U.2/3 Interposer

- Dimensions: 194 x 29 x 337 mm (7.6 x 1 x 13")
- Power connector: Molex 87427-0602
- Analyzer connectors: 4x SFF-8644
- Device connector: SFF-8639 receptacle
- Host connectors: SFF-8639 plug
- SMBUS injection connector: 2x5 pin 0.1" header, 3.3 Vdc
- REFCLKA output connectors: 2x U.FL, AC coupled LPHCSL
- REFCLKA output control connector: 2 pin 0.1" header
- REFCLKA buffer control connector: 3 pin 0.1" header
- REFCLKB output connectors: 2x U.FL,AC coupled LPHCSL
- REFCLKB output control connector: 2 pin 0.1" header
- REFCLKB buffer control connector: 3 pin 0.1" header
- Sideband signal access connector: 2x9 pin 0.1" header, 3.3 Vdc

X4 Slot Interposer

- Dimensions: 25 x 116 x 248 mm (1 x 4.5 x 9.7")
- Power connector: Molex 87427-0602
- Analyzer connectors: 2x SFF-8644
- Device connector: PCIe CEM slot x16 straddle mount connector
- Host module connectors: PCIe CEM x4 Edge fingers
- SMBUS injection connector: 2x5 pin 0.1" header, 3.3 Vdc
- REFCLK output connectors: 2x U.FL, AC coupled LPHCSL
- REFCLK output control connector: 2 pin 0.1" header
- REFCLK buffer control connector: 3 pin 0.1" header
- Sideband signal access connector: 2x9 pin 0.1" header, 3.3 Vdc

Maintenance and Licensing

- Free lifetime software updates – no maintenance fees
- Free full-featured viewer software – easily share annotated traces between computers and colleagues and replay captured traffic
- Use SerialTek hardware on any computer – no additional licenses needed

Warranty

- Two-year limited warranty, Basic and Standard Editions
- Three-year limited warranty, Pro and Enterprise Editions
- Six-month limited warranty, Interposers

Minimum Requirements

- Intel Core, 2 GHz or compatible processor
- 4 GBytes of RAM
- 1280 x 1024 display resolution with at least 65,536 colors
- 64-bit OS only (Windows 7, Ubuntu 14, Centos7 or higher)
- 1GbE controller
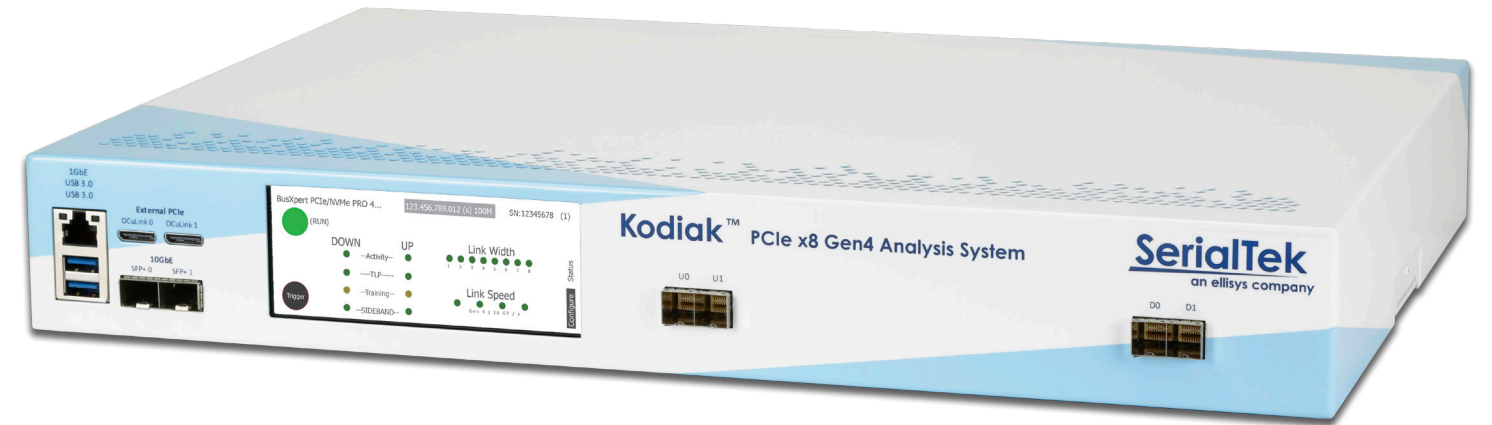
Kodiak™
Next-Generation Gen4 PCIe®/NVMe™ Analyzer

Innovative ▪ Cutting-Edge ▪ Integrated

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More information at: www.serialtek.com/kodiak

DS1000-PK1A-A-062019

PCIe/NVMe Analysis Platform with Embedded Hardware, Real-Time Protocol Processor™, Calibration-Free SI-Fi™ Probing and Automatic Equalization, Internal SSD Storage, Touchscreen LCD, and Standard PCIe Cabling.

State-of-the-Art Architecture

The Kodiak PCIe Gen4 Analysis System represents the state-of-the-art in protocol analyzer design. The Kodiak platform includes an array of high-performance innovations, made possible by an advanced design that breaks free from cumbersome legacy data upload practices in favor of ultra-responsive embedded data processing.

Interface responsiveness is markedly advanced, searches involving massive amounts of data are fast, and hardware filtering is flexible and powerful.

The Kodiak platform, with its field-proven BusXpert (TM) software application, is built to tackle the challenges presented by the complexities of rapidly advancing storage and datacenter I/O technologies.

Real-Time Protocol Processor

Kodiak employs an innovative system register processing concept called Real-Time Protocol Processor (RTPP™). This proprietary feature dynamically and automatically queries and saves PCI configuration space, host controller registers, and NVMe queues, whether the analyzer is actively recording or idle. This alleviates the need for time-consuming and highly impractical reboots, and provides the ability to precisely decode, trigger, and filter using current values.

Multiple Form Factor Support

SI-Fi™ interposer form factors include AIC (x4), M.2 (x4), U.2 (x4), and U.3 (x4). Additionally, U.2, U.3, single-port (1x4), and dual-port (2x2) analysis can be combined into one interposer unit, providing significant cost savings in enterprise environments where all form factors are required. SI-Fi™ interposers also support all relevant sidebands, including SMBus (e.g., NVMe-MI) from the host or from external / third-party injection or generation tools.

Flexible Trace Storage and Retrieval

Kodiak includes two 10GbE SFP+ ports and a GbE port to offload traces to a host computer or network and internal SSD trace storage of up to 2TB (with read-only access for other users). Direct attach storage choices include two USB 3.1 ports and two PCIe 3.0 OCuLink ports.

Transparency in Probe Design is Key

Driven by the need for ever-faster data transfers, PCI Express signaling has become exceptionally complex in design and difficult to monitor unobtrusively. Signal conditioning methods used for PCIe Gen1 and Gen2 now seem primitive compared to the complex approaches used for PCIe Gen3 and Gen4. Further challenges are presented by NVMe, which adds critical requirements like hot-plug and NVM Subsystem Reset (NSSR), where the PCIe signals are renegotiated. SerialTek's proprietary SI-Fi™ technology directly meets and overcomes these challenges with the features and capabilities needed to work efficiently.

With SerialTek's SI-Fi™ interposer technology, the transmitter threshold and pre-emphasis from one link partner reaches the receiver of the other link partner, so the link properly trains to optimum conditions, making the interposer as transparent as possible.

At the core of this technology is a highly specialized linear amplifier design where PCIe analog signals are received at a differential input and distributed to two separate phase-matched differential outputs with a nominal, idealized gain of 0dB. This approach results in easier set up of the analyzer and product under test and avoids a variety of limitations inherent to other probing approaches where link training sequences don't pass through the interposer.

SerialTek's SI-Fi™ interposer technology expands and enables coverage in critical test areas, including link training (LTSSM), Power Management, Hot Plug, Reset, and other situations where the physical link/lane characteristics may change.

No Need for Calibration

Competing PCIe Gen4 analyzers and interposers require tuning, or calibration, which leads to reliability issues as modern PCIe link training sequences can occur dynamically, not just at boot-up.

With SI-Fi™ technology and Kodiak's adaptive EQ capabilities, users can save hours in setup time. And if the link characteristics change (e.g., Hot Plug or NSSR), Kodiak can follow those changes dynamically, ultimately saving your test.

Powerful SerialTek Features

- No tuning (calibration) required
  - Kodiak's Rx automatically equalizes (EQs) the PCIe signals at all data rates
- Embedded trace processing architecture and fastest performance
- Real-Time Protocol Processor
  - Automatically captures PCI Config Space, Controller Registers, and NVMe Queues
  - No boot trace needed
  - Native NVMe triggers by device (BDF), Queues, and Packet/Event
  - Native NVMe filters by device (BDF), Controller Registers, Queues, and Packet/Event
- Deep Trace Buffers
  - 36GB, 72GB, 144GB
- Internal Trace Storage (SSD)
  - 512GB, 1TB, 2TB
  - Read-only access for non-primary users
- Direct Attach Storage
  - Two OCuLink (PCIe 3.0) ports
  - Two USB 3.1 ports
- Network and Direct Connectivity
  - Two 10GbE SFP+ (optical/copper)
  - One 1GbE RJ-45
- Single-port (1x4) and dual-port (2x2) analysis in one platform
- Real-time access to traces in memory (prior to downloading)
  - Users can review and analyze captured traces without downloading the trace
- Touchscreen LCD for analyzer setup and status

Interposers with SI-Fi™ Technology

- No tuning (calibration) required
  - Host and Device signals pass through the interposer, allowing for real-world PCIe link training and easier setup
- SI-Fi™ interposer probes expand coverage to enable testing in critical areas, including link training (LTSSM), Power Management, Hot Plug, Reset, and other situations where the physical link/lane characteristics may change
- AIC (x4), M.2 (x4), U.2 (x4), and U.3 (x4)
  - U.2, U.3, single-port (1x4), and dual-port (2x2) in one interposer
- Access to all sidebands, including SMBus

Real-Time Protocol Processor™

Automatically identifies & updates:

- PCIe configuration space
- Controller data structures (queue attributes, etc.)
- NVMe queue creation and deletion

Uses

- Capture and decode PCIe and NVMe protocols without a boot trace
- Easy analyzer set up
- Correctly decode trace if any of the above attributes change
- Native NVMe triggering: by event (packet), device (BDF), and queue - eliminates false triggers
- Native NVMe Filtering: by device (BDF), controller registers, and queue
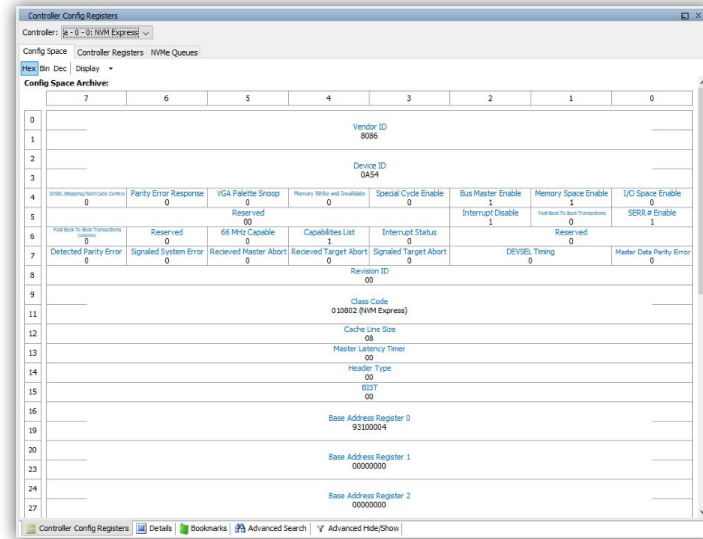
Create triggers easily with searchable drag/drop interface

Simple and advanced multi-ti-state and multi-sequencer triggering

Real-time view of all available devices (BDFs) and NVMe queues
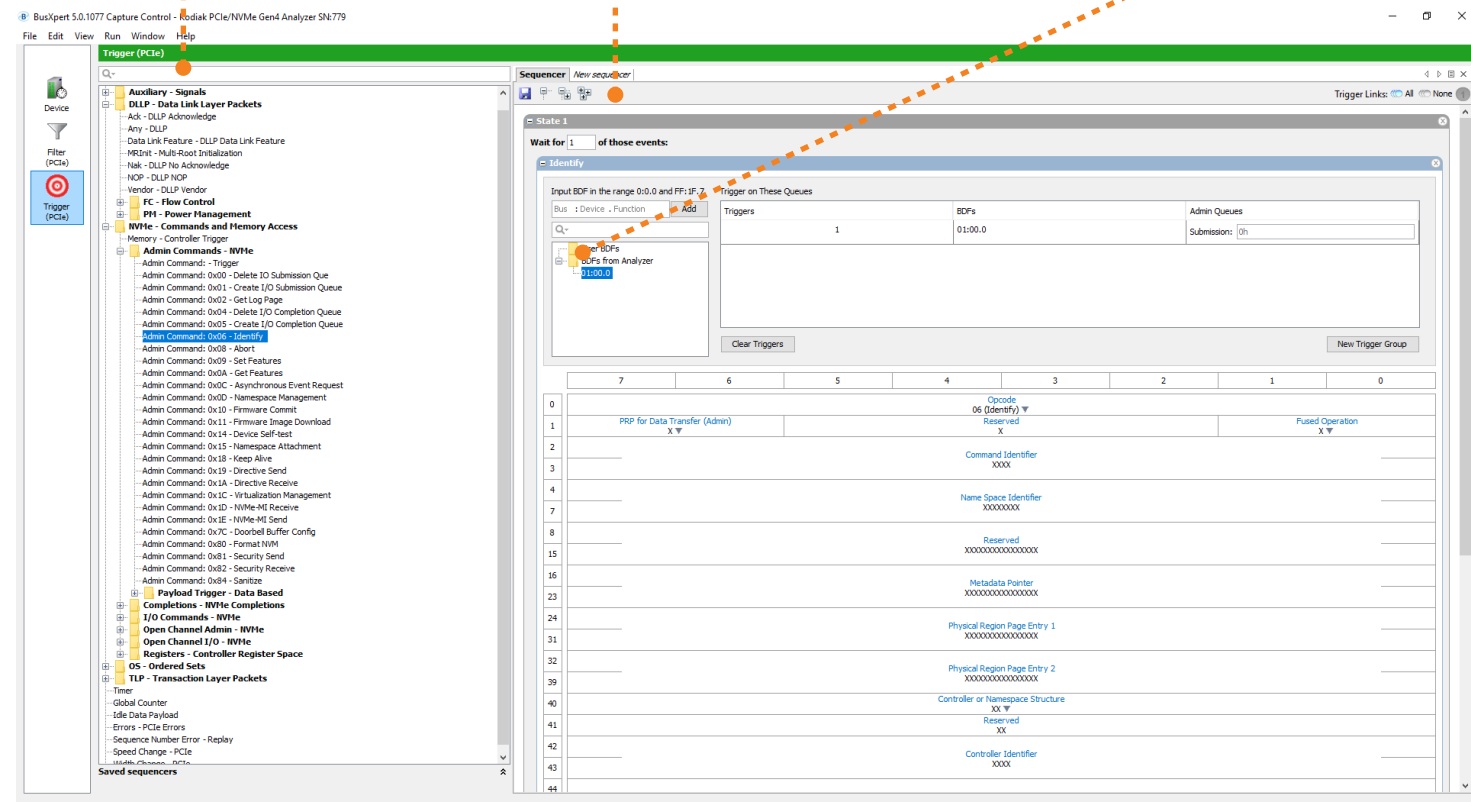
BusXpert Software

Easy Configuration

SerialTek's Java-based BusXpert software supports Microsoft and Linux OS's, is easy to configure, and has the most powerful trigger and filter capabilities in the market. Link speed, link width, lane polarity, and lane inversion are automatically detected or user configurable, and link speed and width changes are also trigger-able. Simple (single-state) & advanced* (multi-state) trigger options are available. Triggering by event, device (BDF), NVMe queue(s), counters, and timers is standard.

*configuration-dependent
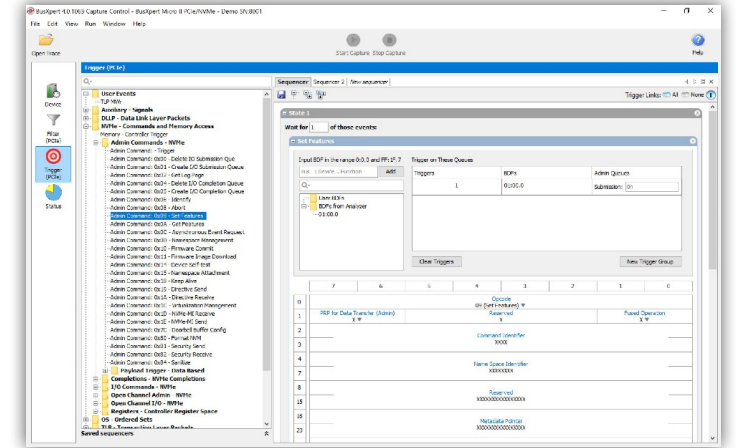
Transaction View

Transaction View is a hierarchical display ideal for viewing the combination of Request packets that deliver PCIe and NVMe commands and the associated completion packets returned from targets at the transaction level. Transaction view sorts transactions based on when the request/command was sent, and then all related packets are sorted by time-stamp and displayed clearly with different colors, including red when errors are detected. Since PCIe and NVMe support multiple lanes, links, and open transactions, this view is ideal to easily analyze commands, completion status, setup, handshaking, and the data transferred each transaction. Columns contain data fields from the packets relevant to the transaction and are selectable by the user.
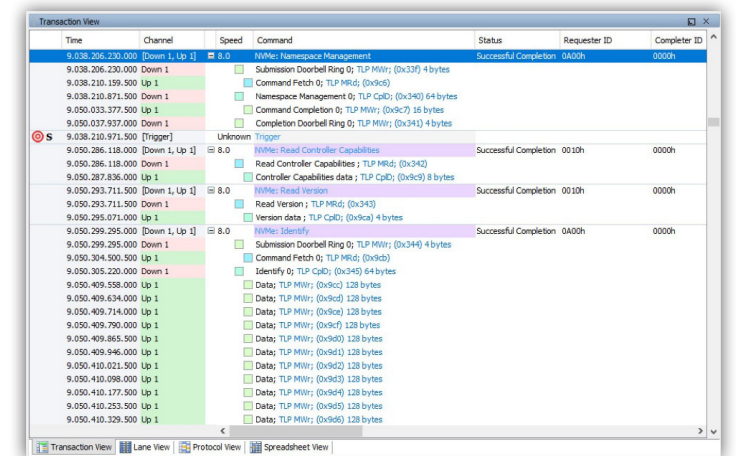
Spreadsheet View

Spreadsheet View is a chronological display of all PCIe and NVMe events sorted by timestamp, including ordered sets, DLLPs, TLPs, NVMe commands, link status, sideband signals/protocols (e.g., SMBus, MCTP, NVMe-MI), and more. Spreadsheet view displays data in rows and columns, where the row represents a packet and the columns represent values for the data fields and other relevant information such as speed or link width.

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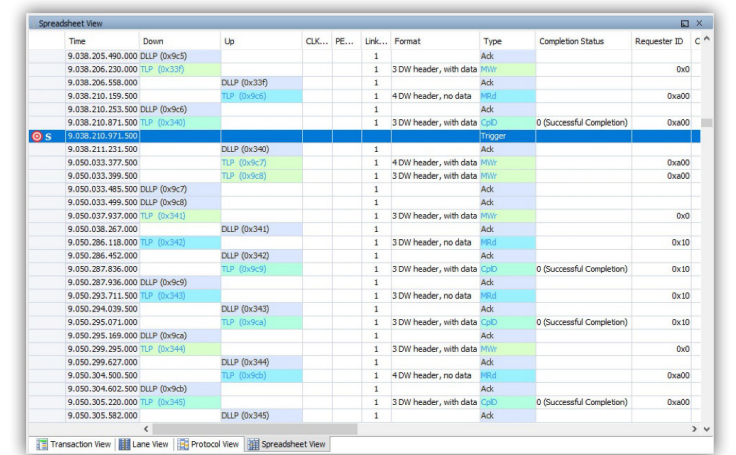
Protocol Views
Low-level and stack protocol elements are hierarchically and chronologically displayed in easily configurable views.

User-Configurable Views & Layouts
Easily modify protocol views by adding or removing columns or arranging the windows by dragging and dropping to desired area.

Fast & Advanced Search
Quickly find events using a contextual search field. Includes multi-state search, multi-trace search, and copy/paste from the trace views.

Fast & Advanced Hide/Show
Quickly show/hide links, sidebands, LTSSM, and protocol events. Includes multi-state filtering and copy/paste from the trace views.

Setup and One-Click Record
Quick access allows for creating or modifying the capture settings, or starting a new capture with a single click.

File Edit View Go To Run Window Help

0110 1010

View | Expand

Search: NVMe=Admin Command 0x06 - Identify

Capture Control   Start Capture   Help

Show Links: All None Dn 1 Up 1   Show Sideband: All None Dn 1 Up 1   Show LTSSM: All None Dn 1 Up 1   NVMe Configuration: Hardware Software   Hide: Idle TLP DLLP TS1 TS2 FTS EIOS EIEOS SKP SDS EDS CSKP   Advanced   Hide: PCIe Details NVMe Details

Transaction Protocol: NVMe PCIe NVMe+Config

Spreadsheet View

	Time	Speed	Link Width	Down	Up	Link ID	Type	Summary	Format	Completion Status	Requester ID	Completer ID	Data Previe
	91.699.898.040.000	16.0	x4		TLP (0x39e)	1	MWr	Submission Doorbell Ring 0	3 DW header, with data		0x0		0x0000000
	91.699.898.120.000	16.0	x4	DLLP (0x39e)		1	Ack						
	91.699.898.881.000	16.0	x4		TLP (0x392)	1	MRd	Command Fetch 0	4 DW header, no data		0xa00		
	91.699.898.917.500	16.0	x4	DLLP (0x392)		1	Ack						
X S	91.699.899.264.500	16.0	x4	TLP (0x39f)		1	CplD	Identify 0	3 DW header, with data	0 (Successful Completion)	0xa00	0x0	0x0002000
	91.699.899.355.000	16.0	x4	DLLP (0x39f)		1	Ack						
O	91.700.199.211.000	16.0	x4		TLP (0x393)	1	MWr		4 DW header, with data		0xa00		0x144d144
	91.700.199.279.500	16.0	x4	DLLP (0x393)		1	Ack						
	91.700.199.283.000	16.0	x4		TLP (0x394)	1	MWr		4 DW header, with data		0xa00		0x0307001
	91.700.199.355.500	16.0	x4	DLLP (0x394)		1	Ack						
	91.700.199.359.000	16.0	x4		TLP (0x395)	1	MWr		4 DW header, with data		0xa00		0x0000446
	91.700.199.427.500	16.0	x4	DLLP (0x395)		1	Ack						
	91.700.199.431.000	16.0	x4		TLP (0x396)	1	MWr		4 DW header, with data		0xa00		0x0000000
	91.700.199.500.000	16.0	x4	DLLP (0x396)		1	Ack						
	91.700.199.503.000	16.0	x4		TLP (0x397)	1	MWr		4 DW header, with data		0xa00		0x0000000
	91.700.199.575.500	16.0	x4	DLLP (0x397)		1	Ack						
	91.700.199.577.000	16.0	x4		TLP (0x398)	1	MWr		4 DW header, with data		0xa00		0x0000000
	91.700.199.647.500	16.0	x4	DLLP (0x398)		1	Ack						
	91.700.199.649.000	16.0	x4		TLP (0x399)	1	MWr		4 DW header, with data		0xa00		0x0000000
	91.700.199.717.500	16.0	x4	DLLP (0x399)		1	Ack						
	91.700.199.721.000	16.0	x4		TLP (0x39a)	1	MWr		4 DW header, with data		0xa00		0x0000000
	91.700.199.789.500	16.0	x4	DLLP (0x39a)		1	Ack						
	91.700.199.793.000	16.0	x4		TLP (0x39b)	1	MWr		4 DW header, with data		0xa00		0x0000026

Spreadsheet View | LTSSM View

Controller Config Registers

Controller: a - 0 - 0: NVM Express

Config Space | Controller Registers | NVMe Queues

Hex Bin Dec | Display

Config Space Archive:

	7	6	5	4	3	2	1	0
0				Vendor ID 144D				
1								
2				Device ID A808				
3								
4	EXBL Stepping/Wait Cycle Control 0	Parity Error Response 1	VGA Palette Snoop 0	Memory Write and Invalidate 0	Special Cycle Enable 0	Bus Master Enable 1	Memory Space Enable 1	I/O Space Enable 0
5				Reserved 00		Interrupt Disable 1	Fast Back To Back Transactions 1	SERR# Enable 1
6	Fast Back To Back Transactions Capable 0	Reserved 0	66 MHz Capable 0	Capabilities List 1	Interrupt Status 0		Reserved 0	
7	Detected Parity Error 0	Signaled System Error 0	Received Master Abort 0	Recieved Target Abort 0	Signaled Target Abort 0	DEVSEL Timing		Master Data Parity Error 0
8				Revision ID 00				
9								
11				Class Code 010802 (NVM Express)				
12				Cache Line Size 00				
13				Master Latency Timer 00				
14				Header Type 00				
15				BIST 00				
16				Base Address Register 0 81400004				
19								
20				Base Address Register 1 00000000				
23								
24				Base Address Register 2 00000000				
27								
28				Base Address Register 3 00000000				
31								
32				Base Address Register 4 00000000				

Transaction View

	Time	Channel	Speed	Command	Status	Requester ID	Completer ID	Tag	Transfer Size	Duration	Transaction ID	Address/Reg	Submission Queue II
X O S	91.699.898.040.000	[Down 1, Up 1]	16.0	NVMe: Identify	Successful Completion	0A00h	0000h	0000h	4,096	0.000.342.227.500	0A0000h	8000003F559...	00000000h
	91.699.898.040.000	Down 1		Submission Doorbell Ring 0; TLP MWr; (0x39e) 4 bytes									
	91.699.898.881.000	Up 1		Command Fetch 0; TLP MRd; (0x392)									
X S	91.699.899.264.500	Down 1		Identify 0; TLP CplD; (0x39f) 64 bytes									
O	91.700.199.211.000	Up 1		Data; TLP MWr; (0x393) 256 bytes									
	91.700.199.283.000	Up 1		Data; TLP MWr; (0x394) 256 bytes									
	91.700.199.359.000	Up 1		Data; TLP MWr; (0x395) 256 bytes									
	91.700.199.431.000	Up 1		Data; TLP MWr; (0x396) 256 bytes									
	91.700.199.503.000	Up 1		Data; TLP MWr; (0x397) 256 bytes									
	91.700.199.577.000	Up 1		Data; TLP MWr; (0x398) 256 bytes									
	91.700.199.649.000	Up 1		Data; TLP MWr; (0x399) 256 bytes									
	91.700.199.721.000	Up 1		Data; TLP MWr; (0x39a) 256 bytes									
	91.700.199.793.000	Up 1		Data; TLP MWr; (0x39b) 256 bytes									
	91.700.199.869.000	Up 1		Data; TLP MWr; (0x39c) 256 bytes									
	91.700.199.937.000	Up 1		Data; TLP MWr; (0x39d) 256 bytes									

Transaction View | Data 1 | Statistics | Lane View | Histogram | Advanced Search | Advanced Hide/Show | Bookmarks

Details | Controller Config Registers | Protocol View

Time X->O: 299,946,500 ps   Trigger: <>   Event Start: 91.699.899.264.500   Event Speed: 16.0 GT/s (x4)

Precision Timestamping
Every event is given a precise timestamp and synchronized across all views. Measuring is easily set via right-clicking the mouse.

Transaction View
All events are precisely timestamped and synchronized across all views. Easily measure between two points (X-O).

Spreadsheet View
Time-ordered, color-coded display of PCIe and NVMe protocol traffic, data, status, and precision timing measurements.

Real-Time Register Processor
Automatically queries/saves PCI configuration space, controller registers, and NVMe queues, whether recording or idle.

Lane View

Lane View is commonly used for debugging lane configuration, lane inversion, reversal, and swizzling. When greater than x1, PCIe uses lane striping, where one byte of a DLLP or TLP are sent down each lane and every lane is used. Lane View is a low-level display of every byte for every packet and their striping. During link negotiation, it is easy to follow ordered sets (e.g., TS1, TS2) and find link training issues.

LTSSM View

LTSSM View is an interactive state diagram comprised of the top-level LTSSM states: detect, polling, configuration, L0, L0s, L1, L2, recovery, loopback, hot reset, and disabled. The upstream and downstream sub-states are color-coded and also displayed side-by-side for the current top-level state in the diagram or area selected in one of the trace views. The LTTSM details below each sub-state also describe the state, sub-state, or transition that is currently selected, including state.substate entry time (start time)/exit time (end time), duration (end time minus start time), and description of the current state.substate from the PCIe specification.

Protocol View

Protocol View is a chronologically aggregated view of packets transmitted on the upstream and downstream lanes, across all layers. This view can be synchronized with other views, such as the Details View, and is ideal for debugging a broad range of issues from protocol events to low-level errors. Data is viewable in K/D format, scrambled, or unscrambled. Timing measurements, fast searches, and bookmarking are available.

Data Viewer

Data Viewer displays the packet or payload for the event selected in either Spreadsheet, Transaction, Lane, or Protocol views. The address for each packet is conveniently displayed first (top-left) and the user can compare up to four packets/payloads. Data is viewable in Hex, Bin, Dec, Bytes, Words, and DWords, and Big Endian or Little Endian. Data viewer is also searchable.

Details View

Details View displays decoded fields for the packet or transaction selected in either Spreadsheet, Transaction, Lane, or Protocol Views. PCIe, NVMe, NVMe-MI, SMBus, and other decodes are formatted and displayed per their respective specifications. NVMe events are displayed either with the TLP or independently via a one-click hide option in the BusXpert software ribbon. Data can be displayed in various formats and widths.

Additional Software Functions

- PCIe and NVMe Statistics: Overall view of the types of traffic captured, navigate into areas of interest, look for max/min performance areas, etc.

- Histogram: User-configurable, graphical representation of trace data

- Bookmarks: X-O markers and timing calculator

- Quick Search: Contextual type search field

- Advanced Search (Multi-state)*: Build search events from the search library or copy/paste from one of the trace views

- Quick Hide/Show on the BusXpert software ribbons

- Advanced Hide/Show (Multi-state)*

*configuration-dependent

SI-Fi™ Interposers

SerialTek's Gen4 (16.0 GT/s) PCI Express® (PCIe®) and Non-volatile Memory Express® (NVMe®) interposers with SI-Fi™ allow users to monitor an unprecedented variety of PCIe and NVMe bus traffic with unparalleled power and ease.

Enabled by SerialTek's proprietary SI-Fi™ technology, users can save hours over legacy approaches requiring interposer calibration. This technology improves critical test coverage by providing high signal integrity, even over changing conditions, such as link training (LTSSM), power management, hot plug, reset, and other tests where the physical link/lane characteristics may change.

Each lane's analog signal is received at the probe's differential input and distributed to two separate phase matched differential outputs with a nominal gain of 0dB, allowing the host and device signals to pass through the interposer, allowing for real-world PCIe link training and easier set-up of the analyzer and DUT.

SI-Fi™ PCIe Gen4 Interposers continue SerialTek's TCO approach. With the focus on signal integrity, flexible, low-cost, SFF-8644-based cables connect each interposer to the analyzer. These cables are readily available and rated greater than 20GHz, resulting in uncompromised SI at all PCIe transfer rates.

All sideband signals are passed through the interposer from root complex (host) to controller (device), and all are made available to the analyzer for trigger, decode, and analysis.

Key Features

- SI-Fi™ Interposers require no calibration
- Supports PCI Express Gen 1.0, 2.0, 3.0, and 4.0
- Accurate capture of PCIe data traffic at line rates including 16.0 GT/s (Gen4), 8.0 GT/s (Gen3), 5.0 GT/s (Gen2), and 2.5 GT/s (Gen1)
- Single U.2 / U.3 interposer supports both single-port and dual-port capture (only one analyzer is needed for dual-port)
- "Passive" tapping to avoid masking, hiding, or "cleaning up" electrical and/or link issues
- Low-cost, flexible, high-performance cabling for reliable analyzer to interposer connections

U.2 and U.3 Overview

- U.2 and U.3 available in one interposer or separate interposers
- U.2 / U.3 interposer supports single-port (1×4) and dual-port (2×2) drives
- U.2 / U.3 interposers available in standard and extended lengths
- Dual-port: analyze both ports with only one analyzer

Configurations and Purchase Information

Editions	Real-Time Protocol Processor	SI-Fi Probing	Embedded Processing	Internal Storage	Trace Buffer	Network Connection	NVMe-MI	Advanced Triggering	Advanced Filtering	Advanced Search	x8 Upgrade-able	Dual-port (2x2)	Cascading
Basic	x	x			36GB	1GbE		1 State	1 State	1 State			
Standard	x	x	Fast	512GB	36GB	10GbEx1	x	1 State	1 State	1 State			
Pro	x	x	Faster	1TB	72GB	10GbEx2	x	x	x	x	x		
Enterprise	x	x	Fastest	2TB	144GB	10GbEx2	x	x	x	x	x	x	x

All Gen4 configurations except Enterprise can be upgraded to a higher configuration

Description	Code
Kodiak Gen4 Enterprise Edition PCIe/NVMe x4 Protocol Analyzer	**PK1A-G4-04-ENT**
Kodiak Gen4 Pro Edition PCIe/NVMe x4 Protocol Analyzer	**PK1A-G4-04-PRO**
Kodiak Gen4 Standard Edition PCIe/NVMe x4 Protocol Analyzer	**PK1A-G4-04-STD**
Kodiak Gen4 Basic Edition PCIe/NVMe x4 Protocol Analyzer	**PK1A-G4-04-BAS**
Kodiak Gen3 Enterprise Edition PCIe/NVMe x4 Protocol Analyzer	**PK1A-G3-04-ENT**
Kodiak Gen3 Pro Edition PCIe/NVMe x4 Protocol Analyzer	**PK1A-G3-04-PRO**
Kodiak Gen3 Standard Edition PCIe/NVMe x4 Protocol Analyzer	**PK1A-G3-04-STD**
Kodiak Gen3 to Gen4 Protocol Analyzer Upgrade	**PK1A/G4-UPG**
Kodiak Pro to Enterprise Edition Protocol Analyzer Upgrade	**PK1A/ENT-UPG**
Kodiak Standard to Pro Edition Protocol Analyzer Upgrade	**PK1A/PRO-UPG**
Kodiak Basic to Standard Edition Protocol Analyzer Upgrade	**PK1A/STD-UPG**

SI-Fi Interposers

Description	Code
PCIe Gen4 x4 Slot Interposer with SI-Fi technology	**PEI-G4-04-SLS**
PCIe Gen4 x4 U.2 single (1x4) and dual-port (2x2) Interposer (standard length).	**PEI-G4-04-U2S**
PCIe Gen4 x4 U.2 single (1x4) and dual-port (2x2) Interposer (extended length)	**PEI-G4-04-U2E**
PCIe Gen4 x4 U.3 single (1x4) and dual-port (2x2) Interposer (standard length)	**PEI-G4-04-U3S**
PCIe Gen4 x4 U.3 single (1x4) and dual-port (2x2) Interposer (extended length)	**PEI-G4-04-U3E**
PCIe Gen4 x4 U.2 and U.3, single (1x4) and dual-port (2x2) Interposer (standard length)	**PEI-G4-04-UXS**
PCIe Gen4 x4 U.2 and U.3, single (1x4) and dual-port (2x2) Interposer (extended length)	**PEI-G4-04-UXE**
PCIe Gen4 M.2 Interposer	**PEI-G4-04-M2S**