TESTMESH TMA-100

Preliminary Available from Q4/2022

Millions of Cycles in a Flash

All-in One Instrument for NVM Technology Evaluation

For Every NVM Technology and Architecture

- Package and wafer level operation
- For single-cell devices and test arrays with analog interface
 - · On transistor and resistor based cells
 - · Emulates charge pumps, sense amplifier, digital logic

Speed-Optimized Architecture

- Hardware support for fast algorithmic cycling
- Waveform and range switch in microseconds
- 1-bit ADC for fast decision
- · Sequencer for array address generation



Accurate Signals and Measurements



- 200 Msample/sec Arbitrary and Functional Waveforms
 - 10 nsec sampling time multi-channel PMU
 - · Low-leakage, fast sensing circuits
 - External SMU integration option

Fast Track to Your NVM



ready-to-go technology evaluation at the best cost of ownership

Feature	Performance
Waveforms	 up to 12 channels Arbitrary and algorithmic waveforms Multiple waveform storage with fast switching -12V+12V, 5 nsec step time, 100mA, 0 or 50 Ohm impedance
PMU	 Operation modes Voltage force current measurement Current force voltage measurement High impedance voltage measurement Pass-through voltage measurement Pass-through current measurement Measurement ranges ±1uA, ±10uA, ±100uA, ±1mA, ±10mA, ±100mA, 2A ±1.2V, ±12V Range switch time < 10us Sampling 10 nsec sampling time On-the-fly averaging, peak detection, 1-bit decision 2k sample buffer
Digital IO	 64 channels with per-pin direction control Vih 1.2V 5.5V programmable in groups of 8 100 MHz engine (full speed in the low voltage range)
Power Supplies	 4 channels 0.5V7V, 2A each Programmable current limit Built-in ramp generator
References	 Dual-channel voltage reference ±12V 20mA Single-channel current reference ±1mA 5V
Architecture	 Dedicated PMU for each group of 4 waveform generators Additional PMU for the digital IOs, supplies and references Switch matrix for output configuration Integration of external SMU

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