

QUICK START GUIDE

Using the SV5C 32 Channel DDR Form Factor

SV5C Personalized SerDes Tester

C SERIES







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Introduction

OVERVIEW

This document describes the required steps for combining two SV5C devices into a single, unified form factor. This form factor, SV5C_32C12G_DDR, is a superset of the SV5C_16C12G_DDR form factor and provides 32 phase aligned transmitter channels. The hardware requirements are given below.

REQUIREMENTS

- (QTY = 2) SV5C Personalized SerDes Testers
- (QTY = 2) 12 V power supply units (part number XP Power AHE220PS12)
- (QTY = 2) USB cables for connection between each SV5C and a PC (included with SV5C)
- (QTY = 4) 12 inch phase-matched cables, SMP female to SMP female (manufacturer part number Amphenol SV Microwave 7012-1292, or contact Introspect)
- (QTY = 2) 6 inch jumper wire, female to female 28AWG (example manufacturer part number Adafruit Industries # 1950)

IMPORTANT NOTE

For fully phase aligned operation across all 32 TX channels, a calibration must be performed on the two SV5C modules. This calibration may be performed in the factory before shipment of a pair of units, or it may be performed "in-field". Please refer to the document "EN-G034E-E-21272 SV5C In-Field Calibration Scripts" for in-field calibration instructions.





Step by Step Guide

CUSTOM FORM FACTOR CREATION

1. Open the GUI with the SV5C_16C12G_DDR form factor, as shown in Figure 1.

	Controspect ESP ×	
	\frown	
	introspect technology	
	Welcome to Introspect ESP (v 21.4.0)	
	To narrow down the choices in the menu below, type part of the desired form factor name in the "Filter" box.	
	Filter:	
	Choose the IESP form factor	
	SV5C_16C12G_DDR ~	
	Info about Preferences	
	< Back Next >	
Figure 1: Selecting 16 channel form factor	r.	

 Connect the USB cable from your PC to the first SV5C (referred to here as "Box 1"). After connecting to Box 1 via the Introspect GUI (IESP/SV5C_16C12G_DDR -> Connect), you will see serial numbers in the log, like those shown below:

Connecting to serialNum 'FTDI:INSV5M20050020A' Connected to subPart 'SV5C_16C12G_DDR_A' Connecting to serialNum 'FTDI:INSV5M20050020B' Initializing IESP hardware/firmware Doing post-connection initialization

3. Connect the USB cables from your PC to both SV5C boxes and open the GUI with the SV5C_32C12G_DDR form factor.



4. Open the "ConnectionConfig" tool (IESP/SV5C_32C12G_DDR -> ConnectionConfig). Select the FtdiSerialNumber for box 1 to be the number recorded in step 2, and use the other option in the drop-down menu for box 2, as shown in Figure 2:

Specify the FTDI serial numbers The FTDI serial numbers are writ Otherwise, an easy way to find o to limit the serial numbers that are	ten on the bottom of the boxes. ut the FTDI serial numbers is to p	hysicalyl disc		
Hardware	Default FTDI Pattern	Matching	RdiSerialNumber	
SV5C_16C12G_DDR : box1	"FTDHNSV5."		FTDI:INSV5M20050020	~
SV5C_16C12G_DDR : box2	^FTDI:INSV5.*		FTDI:INSV5M210420	~
	Ok	1 1	Cancel	

5. Close the "ConnectionConfig" tool and connect to both SV5C boxes (IESP/SV5C_32C12G_DDR -> Connect). You should see a successful connection to both boxes like below.

```
Connecting to serialNum 'FTDI:INSV5M20050020A'
Connected to subPart 'SV5C_16C12G_DDR_box1_A'
Connecting to serialNum 'FTDI:INSV5M20050020B'
Connected to subPart 'SV5C_16C12G_DDR_box2_A'
Connecting to serialNum 'FTDI:INSV5M210420B'
Initializing IESP hardware/firmware
Doing post-connection initialization
```



SV5C CONNECTION DIAGRAMS

Diagrams showing the required connections of the two modules are given in the figure below. Figure 3(a) shows the full set of cable connections between Box 1 and Box 2. In addition to the reference clock connections, three sets of cable connections (one SMP pair, two GPIO jumper wires, and USB connections to the PC) are made on the left side of each SV5C, and the connection ports on this side are shown in Figure 3(b). Detailed connections for GPIO pins via jumper wires are shown Figure 3(c).





USING THE SV5C_32C12G_DDR FORM FACTOR

Open a new test procedure with the SV5C_32C12G_DDR form factor. In the new form factor, under globalClockConfig, you will see that two "referenceClocksConfig" components have automatically been created. This is as shown in the screen capture in Figure 4.

Note that the "refClocksConfig1" component controls "Box 1" has been configured to use its internal "systemRefClockSource" while the "refClocksConfig2" component controls "Box 2" has been configured to use an external reference clock provided by "Box 1". This matches the cable setup as shown in Figure 3(a).

Components globalClockCorfig properties (class: MultBoxClockCorfig) Interface [12500.0] uWidths ureform referenceClocks Interface Interface [12500.0] uWidths ureform referenceClocks Interface dataRates [Interface uWidths ureform dataRates [Interface dataRates Sets the dataRates in Mbps) on the clock groups of the IESP. If fewer dataRates are specified than the number of clock groups, the last dataRate is used for the remaining clock groups. (channels for cloc) Text Procedure 1 globalClockConfig.setup ()	File Edit IESP/SV5C_32C12G_DDI Params	R Wizards ControlPanels Tools	Results Help Results	
Image: Set Stand Set Standing Ind CocksConfig1 Ind CocksConfig1 Ind CocksConfig1 Ind CocksConfig2 Ind CocksConfig1 Ind CocksConfig1 Ind CocksConfig2 Ind CocksConfig1 Ind CocksConfig2 Ind CocksCond	Components			Config)
Test Procedure	globalClockConfig refClocksConfig1	dataRates uWidths referenceClocks	[12500.0] InterClocksCorfig1.	refClocksCorfig2
		Sets the dataRates (in Mbps) on the clo clock groups, the last dataRate is used	ick groups of the IESP. If fewer dataRate for the remaining clock groups. There are	s are specified than the number of 2 clock groups: (channels for cloc
		up ()		

Figure 4: Reference clock component setup for 32 channel form factor.

Edit the "dataRates" attribute to include 2 dataRates as shown below. The "uiWidths" attribute will update automatically, as displayed in Figure 5.

	globalClockCo	nfig properties (class: MultiBoxClockConfig)	
d	dataRates	[12500.0, 12500.0]	
	uiWidths	[80:0, 80:0]	
n	referenceClocks	[refClocksConfig1, refClocksConfig2]	
Figure 5: Data rate settin	g for 32 channel form facto	or.	



Under the "components" window pane, press "Add" and add a "txChannelList" component. Once added, you may change the number of channels to the full range of 1-32. This is as shown in the screen capture in Figure 6. Note that channels 1-16 are on "Box 1", and channels 17-32 are on "Box 2".

File Edit IESP/SV5C_32C12G_DDR Params	Wizards ControlPanels Tools Results Help Log Results	
Components	txChannelList 1 properties (class: TxChannelList)	
JobalCockdConfig refDockdConfig refDockdConfig1 refCockdConfig2 bxChannelList1	Channels channels [I-32] pattern Mode Iacda pattern Mode Iacda holdPattern States [ide] attABits 00000000 polatities [normal] votageSwings [800.0] common/ModeVotages [600.0] preEmphasis jiterhjection fmeSkews [0.0] coarseSkews [0.0]	
Add Remove Config	commonModeVoltages Sets the common mode voltage (in mV) separately on each channel. Range: min -20 mV, value is a list of voltages (e.g. [200.0, 500.0, 300.0]). If fewer voltages are specified than t	max 700 mV. The parameter the number of channels, th
l globalClockConfig.setup 2 txChannelListl.setup()	P () Run	

All other operations for the form factor SV5C_32C12G_DDR may be used as in the previous 16 channel form factor. Existing test procedures developed for the 16 channel form factor may be imported and channel lists modified as required.

IMPORTANT NOTE

If phase alignment across all 32 TX channels has been performed as in the in-field calibration document (see "EN-G034E-E-21272 SV5C In-Field Calibration Scripts"), then it is important to externally label the first SV5C unit (master) as "Box 1" and the second unit (slave) as "Box 2". This labelling must be kept consistent during subsequent usage. TX Channels 1-32, as shown in the channel list above, will not be aligned if the order of Box 1 and Box 2 is changed.



Revision Number	History	Date
1.0	Document release	June 10, 2020
1.1	Update custom form factor September 13, 2021 creation steps	

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