SV3C – DPTX MIPI D-PHY Generator

4-Lane, up to 6.5 Gbps Instrument for MIPI D-PHY Generation

The SV3C-DPTX MIPI D-PHY Generator is an ultraportable, high-performance instrument that enables exercising and validating MIPI D-PHY receiver ports. Capable of generating any traffic and being completely data-rate agile, the D-PHY generator includes analog parameter controls that enable gaining deep insights into receiver sensitivity performance and skew / jitter tolerance. Featuring 4 lanes which enables testing of an entire MIPI physical layer receiver port and full protocol testing of both CSI and DSI packets.



Key Features:

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- Data rates: 80 Mbps to 6.5 Gbps fullycontinuous operating range, including automatically generating and handling LP and HS data.
- Lanes: 4 Tx and 1 Clock
- Signal impairments: each pattern generator channel offers independent voltage, timing and jitter injection.
- Pattern Generation: Generate traffic including DSI and CSI, color-bar and active image frames.
- Easy to Use: Introspect ESP enables interactive operation or full automation

Key Benefits:

- Parallel: with increasing crosstalk issues, a truly parallel system allows for the most comprehensive "stress test" that is possible. The SV3C tests all your lanes simultaneously.
- Self Contained: an all-in-one system reduces bench space and helps create a portable test and measurement environment; the SV3C integrates multiple tools into one.
- Automated: scripting capability is ideal for debug tasks, firmware verification, and full-fledged production screening of devices and system modules.



Typical application: Receiver Stressing

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Transmitter Parameters

| Parameter | Value | Description |
|-------------------------------------|--------------------------------|---|
| Number of Differential Transmitters | 4+1 | 4 data lanes plus 1 clock lane |
| HS Differential Voltage Swing | 20 – 600 mV | |
| LP Differential Voltage Swing | 650 – 1300 mV -100 – 600 mV | Logic High Range Logic Low Range |
| Transmitter Skew Adjust | +/- 20 UI | |
| Total Memory Space | 4 GByte | Space allocated to transmit patterns and images |

Pattern Generator Functions

| Feature | Description | Benefit |
|----------------------|--|---|
| Pattern Generators | Pre-built image formats, RAW, RGB, and YUV, HS- Only, HS-Only+PRBS, and packet loop pattern sequencers | Allows for flexible stimulus generation (e.g. training sequences or compliance patterns) |
| Analog Controls | Polarity inversion, voltage swing, transmit pre-emphasis, duty cycle, bit-slip | Provides deep receiver stress characterization with truly independent multi-variable analysis |
| Synthesis Capability | Sinusoidal jitter injection, random jitter injection, de- emphasis generation | Allows for comprehensive receiver testing with internally synthesized noise sources |





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