SV1C Personalized SerDes Tester

Data Sheet

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Introduction

Overview

The SV1C Personalized SerDes Tester is an ultra-portable, high-performance instrument that creates a new category of tool for high-speed digital product engineering teams. It integrates multiple technologies in order to enable the self-contained test and measurement of complex SerDes interfaces such as PCI Express Gen 3, MIPI M-PHY, Thunderbolt, or USB3. Coupled with a seamless, easy-to-use development environment, this tool enables product engineers with widely varying skills to efficiently work with and develop SerDes verification algorithms. The SV1C fits in one hand and contains 8 independent stimulus generation ports, 8 independent capture and measurement ports and various clocking, synchronization and lane-expansion capabilities. It has been designed specifically to address the growing need of a parallel, system-oriented test methodology while offering world-class signal-integrity features such as jitter injection and jitter measurement.

With a small form factor, an extensive signal-integrity feature set, and an exceptionally powerful software development environment, the SV1C is not only suitable for signal-integrity verification engineers that perform traditional characterization tasks, but it is also ideal for FPGA developers and software developers who need rapid turnaround signal verification tools or hardware-software interoperability confirmation tools. The SV1C integrates state of the art functions such as digital data capture, bit error rate measurement, clock recovery, jitter decomposition and jitter generation.

Key Benefits

- True parallel bit-error-rate measurement across 8 lanes
- Fully-synthesized integrated jitter injection on all lanes
- Fully-automated integrated jitter testing on all lanes
- Optimized pattern generator rise-time for receiver stress test applications
- Flexible pre-emphasis and equalization
- Flexible loopback support per lane
- Hardware clock recovery per lane
- State of the art programming environment based on the highly intuitive Python language
- Integrated device control through SPI, I2C, or JTAG
- Reconfigurable, protocol customization (on request)

Applications

Parallel PHY validation of serial bus standards such as:

- PCI Express (PCIe)
- UHS-2
- MIPI M-PHY
- CPRI
- USB
- HDMI
- Thunderbolt
- XAUI
- JESD204B
- SATA

Interface test of electrical/optical media such as:

- Backplane
- Cable
- CFP MSA, SFP MSA, SFP+ MSA

Plug-and-play system-level validation such as:

- PCI Express
- DisplayPort sink/source
- MIPI M-PHY

Timing verification:

- PLL transfer function measurement
- Clock recovery bandwidth verification
- Frequency ppm offset characterization

Mixed-technology applications:

- High-speed ADC and DAC (JESD204) data capture and/or synthesis
- FPGA-based system development
- Channel and device emulation

Clock-recovery triggering for external oscilloscope or BERT equipment

Physical Connectors

Figure 1 shows the high-speed differential transmit and receive data pins, reference clock connectors, power and USB ports on the SV1C chassis. The auxiliary triggers and programmable SCSI ports are optional features.

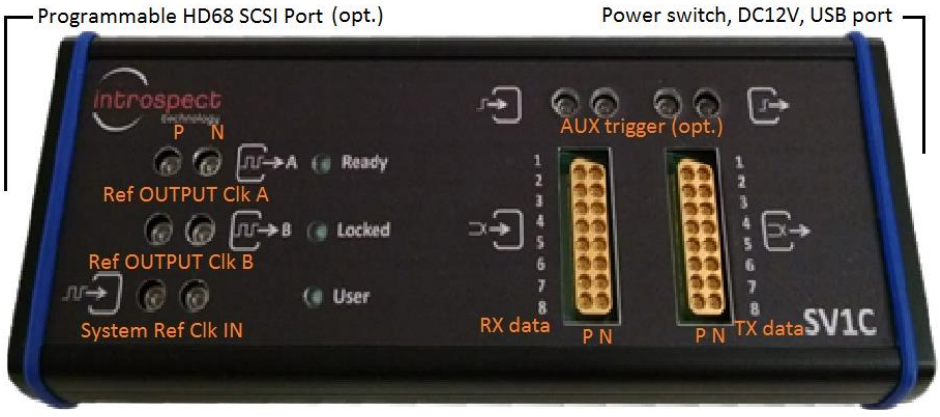


Figure 1 SV1C connectors

Features

Multi-Lane Loopback

The SV1C is the only bench-top tool that offers instrument-grade loopback capability on all differential lanes. The loopback capability of the SV1C includes:

- Retiming of data for the purpose of decoupling DUT receiver performance from DUT transmitter performance
- Arbitrary jitter or voltage swing control on loopback data

Figure 2 shows two common loopback configurations that can be used with the SV1C. In the first configuration, a single DUT's transmitter and receiver channels are connected together through the SV1C. In the second configuration, arbitrary pattern testing can be performed on an end-to-end communications link. The SV1C is used to pass data through from a traffic generator (such as an end-point on a real system board) to the DUT while stressing the DUT receiver with jitter, skew, or voltage swing.

Figure 2 Illustration of loopback applications.

Multiple-Source Jitter Injection

The SV1C is capable of generating calibrated jitter stress on any data pattern and any output lane configuration. Sinusoidal jitter injection is calibrated in the time and frequency domain in order to generate high-purity stimulus signals as shown in Figure 3.

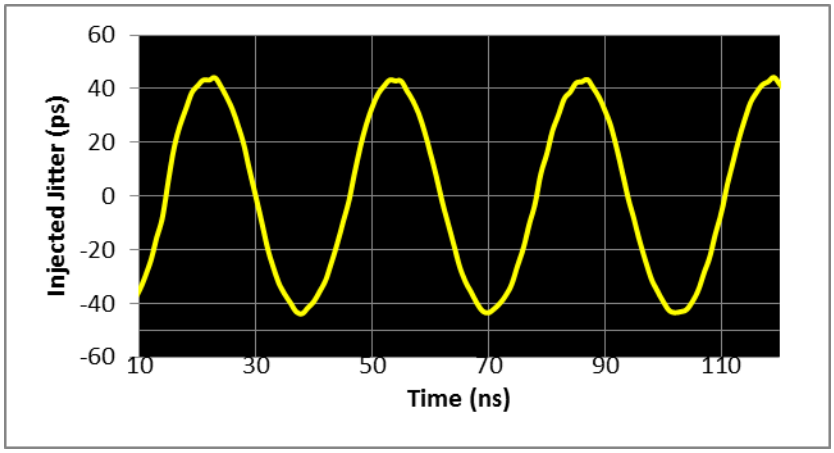


Figure 3 Illustration of calibrated jitter waveform.

The jitter injection feature is typically exploited in order to perform automated jitter tolerance testing as shown in the example in Figure 4. As is the case for other features in the SV1C Personalized SerDes Tester, jitter tolerance testing happens in parallel across all lanes. For advanced applications, the SV1C also includes RJ injection and a third-source arbitrary waveform jitter synthesizer.

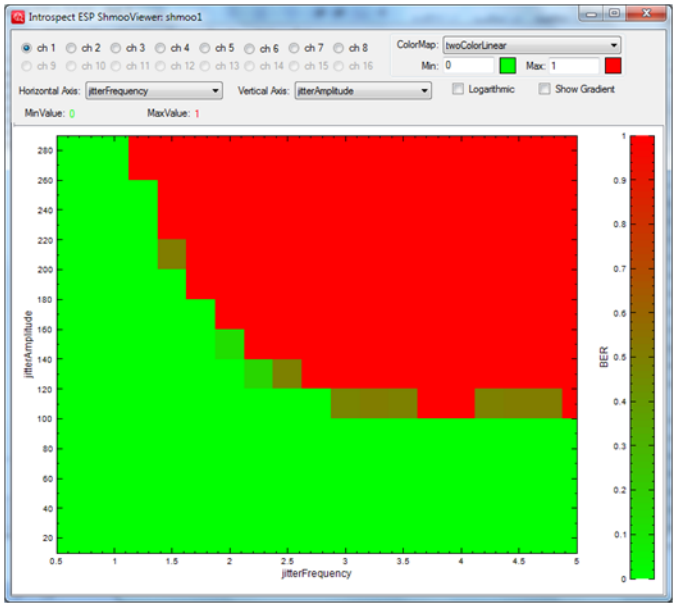


Figure 4 Illustration of jitter tolerance curve.

Pre-Emphasis Generation

Conventionally offered as a separate instrument, per-lane pre-emphasis control is integrated on the 8-lane SV1C tester. The user can individually set the transmitter pre-emphasis using a built-in Tap structure. Pre-emphasis allows the user to optimize signal characteristics at the DUT input pins.

Each transmitter in the SV1C implements a discrete-time linear equalizer as part of the driver circuit. An illustration of such equalizer is shown in Figure 5, and sample synthesized waveform shapes are shown in Figure 6.

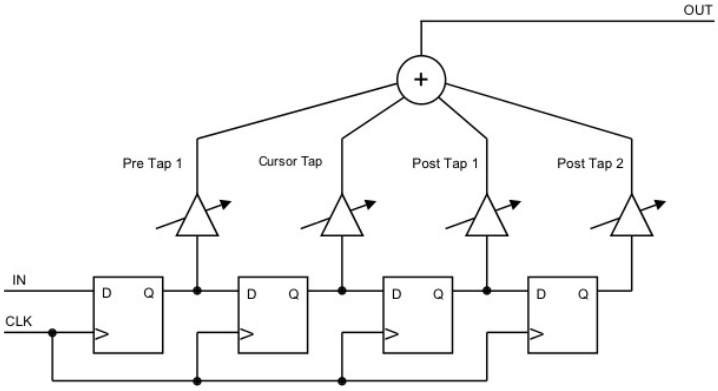


Figure 5 Illustration of pre-emphasis design.

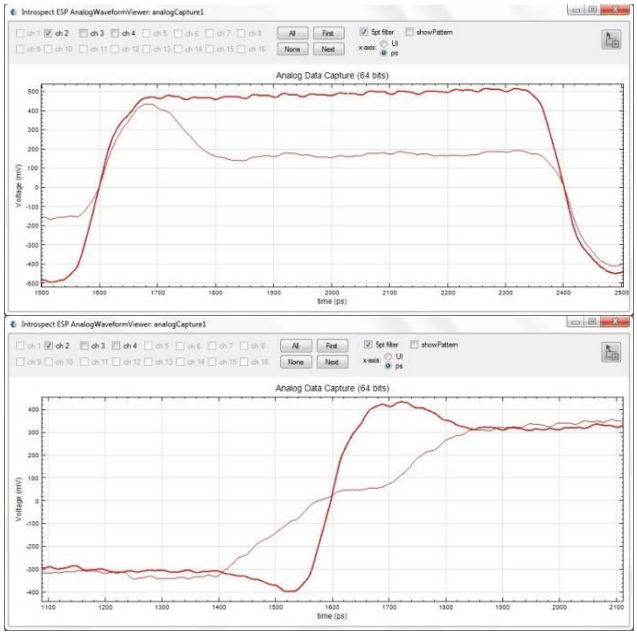


Figure 6 Illustration of multiple waveform shapes that can be synthesized using the pre-emphasis function of the SV1C.

Programmable SSC Generation and Frequency Synthesis

The SV1C incorporates precision frequency synthesis technology that allows for the generation of programmable SSC waveforms at any data rate. The SSC waveforms are superimposed on the pattern generator outputs, and they coexist with other jitter injection sources of the SV1C. Thus, a truly complete jitter cocktail can be produced for the most thorough receiver validation. Figure 7 illustrates the SSC capability of the SV1C. In the figure, the SV1C is programmed to synthesize four slightly different modulation frequencies showcasing the precision programmability of the tool.

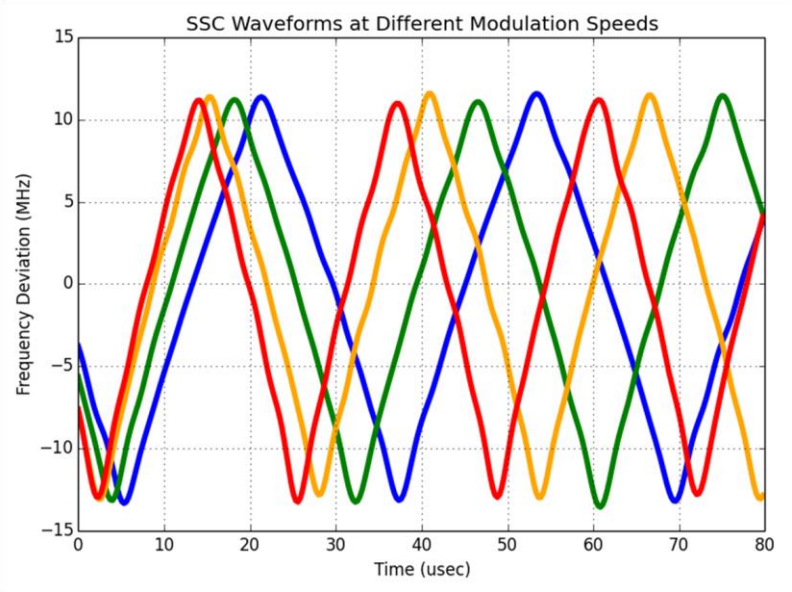


Figure 7 Programmable SSC generation.

Per-Lane Clock Recovery and Unique Dual-Path Architecture

Like pre-emphasis, conventional tools often require separate clock recovery instrumentation. In the SV1C, each receiver has its own embedded analog clock recovery circuit. Additionally, the clock recovery is monolithically integrated directly inside the receiver's high-speed sampler, thus offering the lowest possible sampling latency in a test and measurement instrument. The user does not have to make special connections or carefully match cable lengths. The monolithic nature of the SV1C clock recovery helps achieve wide tracking bandwidth for measuring signals that possess spread-spectrum clocking or very high amplitude wander. Figure 8 shows a block diagram of the clock recovery capability inside the SV1C Personalized SerDes Tester.

Also shown in Figure 8 is the dual-path receiver architecture of the SV1C. This unique architecture allows the SV1C to operate as both a digital capture/analysis instrument and an analog measurement instrument. A feature rich clock management system allows for customization of the SV1C to specific customer requirements.

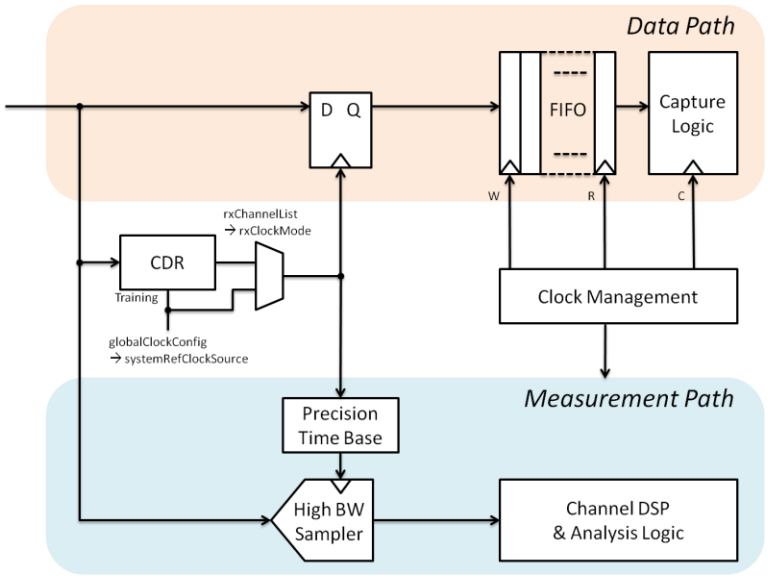


Figure 8 Per-lane clock recovery and dual-path architecture.

Auxiliary Control Port

The SV1C includes a low-speed auxiliary control port that is based on a standard SCSI connector (Figure 9). This port enables controlling DUT registers through JTAG, I2C, or SPI. Additionally, the port includes reconfigurable trigger and flag capability for synchronizing the SV1C with external tools or events.

Figure 9 Photograph of the auxiliary control port on the SV1C.

Analysis

The SV1C instrument has an independent Bit Error Rate Tester (BERT) for each of its input channels. Each BERT compares recovered (retimed) data from a single input channel against a specified data pattern and reports the bit error count.

Apart from error counting, the instrument offers a wide range of measurement and analysis features including:

- Jitter separation
- Eye mask testing
- Voltage level, pre-emphasis level, and signal parameter measurement
- Frequency measurement and SSC profile extraction

Figure 10 illustrates a few of the analysis and reporting features of the SV1C. Starting from the top left and moving in a clock-wise manner, the figure illustrates bathtub acquisition and analysis, waveform capture, raw data viewing, and eye diagram plotting. As always, these analysis options are executed in parallel on all activated lanes.

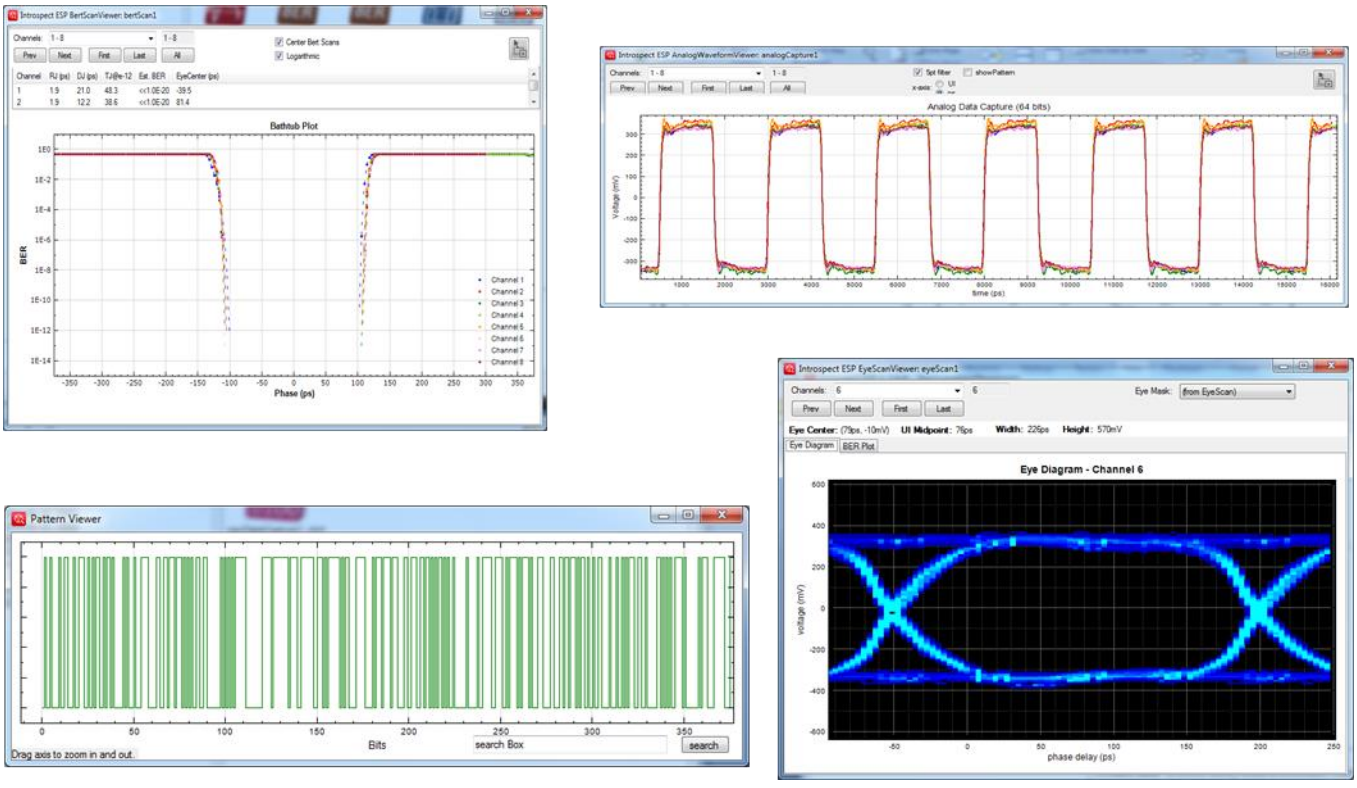
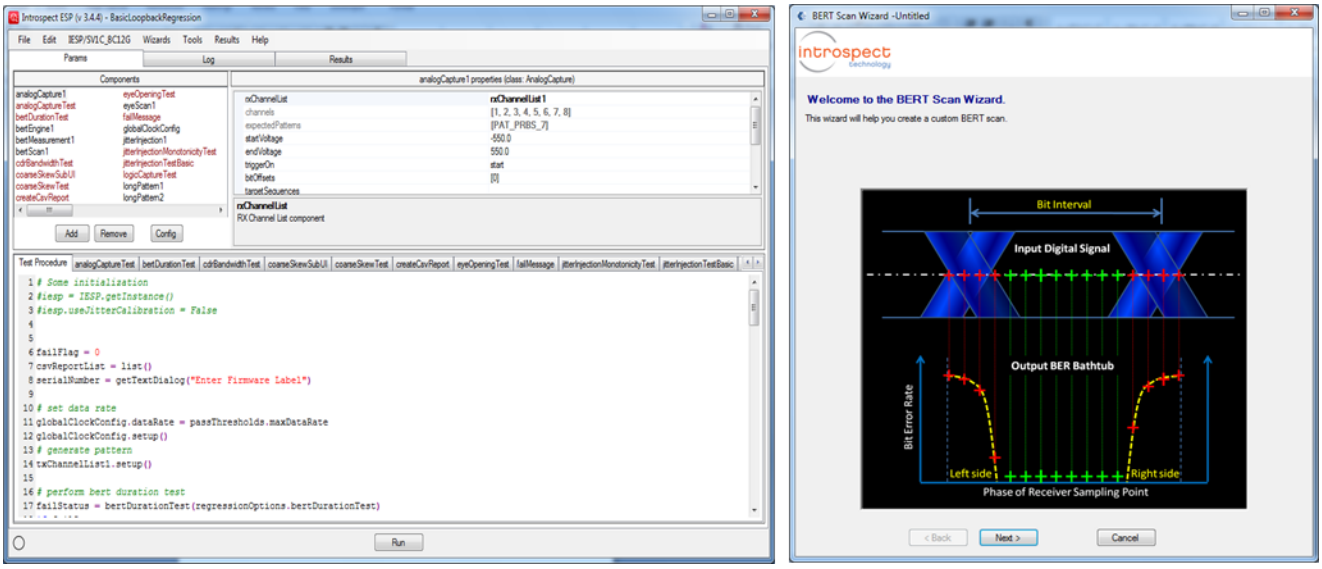


Figure 10 Sampling of analysis and report windows.

Automation

The SV1C is operated using the award winning IntrospectESP Software. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shot in Figure 11(a). Component-based design is IntrospectESP's way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. For further help, the SV1C features automatic code generation for common tasks such as Eye Diagram or Bathtub Curve generation as shown in Figure 11(b).



(a) *(b)*

Figure 11 Screen capture of IntrospectESP user environment.

Specifications

Table 1 General Specifications

Parameter	Value	Units	Description and Conditions
Ports			
Number of Differential Transmitters	8		
Number of Differential Receivers	8		
Number of Dedicated Clock Outputs	2		Individually synthesized frequency and output format.
Number of Dedicated Clock Inputs	1		Used as external Reference Clock input.
Number of Trigger Input Pins	Multiple		Consult user manual for included capability. Contact factory for customization.
Number of Flag Output Pins	Multiple		Consult user manual for included capability. Contact factory for customization.
Data Rates and Frequencies			
Minimum Programmable Data Rate	1	Mbps	
Maximum Programmable Data Rate	14	Gbps	
Maximum Data Rate Purchase Options	4	Gbps	
	8.5	Gbps	
	12.5	Gbps	
	14	Gbps	
Data Rate Field Upgrade	4-12.5	Gbps	Contact factory for details.
Frequency Resolution of Programmed Data Rate	1	kHz	Finer resolution is possible. Contact factory for customization.
Clock Input			Support for LVDS, LVPECL, CML, HCSL, and CMOS.
Frequency Range	25 – 250	MHz	
Single-ended Input Impedance	20/40/60	kΩ	min / typ / max
Common mode/Threshold voltage	0.9/--/1.4 @ 1.8V	V	min / typ / max
	1.0/--/1.7 @ 2.5V	V	min / typ / max
	3.3/--/1.95 @ 1.95V	V	min / typ / max
Minimum Differential Voltage Swing	200 / 250	mVpp	f_{in} < 212.5MHz / f_{in} > 212.5MHz
Clock Outputs			
Frequency Range	10 - 250	MHz	in steps of 1kHz
Common mode/Threshold voltage	1.45/1.2/0.875/0.375/-	V	typical LVPECL/LVDS2.5-3.3V/LVDS1.8V/HCSL/CML
Differential Voltage Swing	0.8/0.35/0.35/0.725/0.86	Vpp	typical LVPECL/LVDS2.5-3.3V/LVDS1.8V/HCSL/CML also supports single-ended CMOS format

Table 2 Transmitter Characteristics

Parameter	Value	Units	Description and Conditions
Output Coupling			
DC common mode voltage	750	mV	typical (different offsets are firmware programmable)
AC Output Differential Impedance	100	Ohm	typical
Voltage Performance			
Minimum Differential Voltage Swing	20	mV	
Maximum Differential Voltage Swing	1000	mVpp	312.5 Mbps to 5 Gbps, 50 ohm AC coupled termination.
	800	mVpp	5 Gbps to 12.5 Gbps, 50 ohm AC coupled termination.
Differential Voltage Swing Resolution	20	mV	

Accuracy of Differential Voltage Swing	larger of: +/-10% of programmed value, and +/-10mV	%, mV	
Rise and Fall Time	50	ps	Typical, 500 mVpp signal, 20-80%, 50 ohm AC coupled termination.
	75	ps	Typical, 500 mVpp signal, 10%-90%, 50 ohm AC coupled termination.
Pre-emphasis Performance			
Pre-Emphasis Pre-Tap Range	-4 to +4	dB	Both high-pass and low-pass functions are available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Pre-Tap Resolution	Range / 32	dB	
Pre-Emphasis Post1-Tap Range	0 to 6	dB	Only high-pass function is available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Post1-Tap Resolution	Range / 32	dB	
Pre-Emphasis Post2-Tap Range	-4 to +4	dB	Both high-pass and low-pass functions are available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Post2-Tap Resolution	Range / 32	dB	
Jitter Performance			
Random Jitter Noise Floor	1000	fs	Based on measurement with high-bandwidth scope and with first-order clock recovery.
Minimum Frequency of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Frequency of Injected Deterministic Jitter	80	MHz	
Frequency Resolution of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Peak-to-Peak Injected Deterministic Jitter	1400	ps	This specification is separate from low-frequency wander generator and SSC generator.
Magnitude Resolution of Injected Deterministic Jitter	500	fs	Jitter injection is based on multi-resolution synthesizer, so this number is an effective resolution. Internal synthesizer resolution is defined in equivalent number of bits.
Injected Deterministic Jitter Setting	Per-bank		Common across all channels within a bank.
Maximum RMS Random Jitter Injection	0.1	UI	
Magnitude Resolution of Injected Jitter	0.1	ps	
Accuracy of Injected Jitter Magnitude	larger of: +/-10% of programmed value, and +/-10 ps	%, ps	
Injected Random Jitter Setting	Common		Common across all channels within a bank.
Transmitter-to-Transmitter Skew Performance			
Lane to Lane Integer-UI Minimum Skew	-20	UI	
Lane to Lane Integer-UI Maximum Skew	20	UI	
Effect of Skew Adjustment on Jitter Injection	None		
Lane to Lane Skew	+/- 30	ps	

Table 3 Receiver Characteristics

Parameter	Value	Units	Description and Conditions
Input Coupling			
AC Input Differential Impedance	100	Ohm	
AC Performance			
Minimum Detectable Differential Voltage	25	mV	
Maximum Allowable Differential Voltage	2000	mV	
Minimum Programmable Comparator Threshold Voltage	-550	mV	
Maximum Programmable Comparator Threshold Voltage	+550	mV	
Differential Comparator Threshold Voltage Resolution	10	mV	
Differential Comparator Threshold Voltage Accuracy	larger of: +/-10% of programmed value, and +/-10mV	%, mV	
Measured Eye Width Accuracy	10%		Maximum error, 312.5 Mbps – 2.0 Gbps, 200 mVpp minimum input amplitude
	15%		Maximum error, 2.0 Mbps - 5 Gbps, 200 mVpp minimum input amplitude
	25%		Maximum error, 5 Gbps – 12.5 Gbps, 200 mVpp minimum input amplitude
Resolution Enhancement & Equalization			
DC Gain	0	dB	
	2	dB	
	4	dB	
	6	dB	
	8	dB	
CTLE Maximum Gain	16	dB	
CTLE Resolution	1	dB	
DC Gain Control	Per-receiver		
Equalization Control	Per-receiver		
Jitter Performance			
Input Jitter Noise Floor in System Reference Mode	25	ps	
Input Jitter Noise Floor in Extracted Clock Mode	10	ps	
Timing Generator Performance			
Resolution at Maximum Data Rate	31.25	mUI	Resolution (as a percentage of UI) improves for lower data rate. Contact factory for details.
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	Unlimited		
Skew			
Lane to Lane Skew Measurement Accuracy	+/- 10	ps	

Table 4 Clocking Characteristics

Parameter	Value	Units	Description and Conditions
Internal Time Base			
Number of Internal Frequency References	2		Relevant for future customization.
Embedded Clock Applications			
Transmit Timing Modes	System Extracted		Clock can be extracted from one data receiver channels to drive all transmitter channels.
Receive Timing Modes	System Extracted		All channels have clock recovery for extracted mode operation.
Lane to Lane Tracking Bandwidth	4	MHz	
Single-Lane CDR Tracking Bandwidth	3 - 12	MHz	
Forwarded Clock Applications			
Transmit Timing Modes	System Forwarded		Channel 1 acts as forwarded clock for samplers.
Receive Timing Modes	System Forwarded		Channel 1 acts as forwarded clock for samplers.
Clock Tracking Bandwidth	4	MHz	Second order critically damped response.
Spread Spectrum Support			
Receive Lanes Track SSC Data	Yes		Requires operation in extracted clock mode.
Transmit Lanes Generate SSC Data	Yes		Consult factory for availability.
Minimum Spread	0.1	%	
Maximum Spread	2	%	
Spread Programming Resolution	0.01	%	
Minimum Spreading Frequency	31.5	kHz	
Maximum Spreading Frequency	63	kHz	

Table 5 Pattern Handling Characteristics

Parameter	Value	Units	Description and Conditions
Loopback			
Rx to Tx Loopback Capability	Per channel		
Lane to Lane Latency Mismatch	0	UI	
Preset Patterns			
Standard Built-In Patterns	All Zeros D21.5 K28.5 K28.7 DIV.16 DIV.20 DIV.40 DIV.50 PRBS.5 PRBS.7 PRBS.9 PRBS.11 PRBS.13 PRBS.15 PRBS.21 PRBS.23 PRBS.31		
Pattern Choice per Transmit Channel	Per-transmitter		
Pattern Choice per Receive Channel	Per-receiver		
BERT Comparison Mode	Automatic seed generation for PRBS		Automatically aligns to PRBS data patterns.
User Programmable Pattern Memory			
Total Available Memory	2	GByte	Memory allocation is customizable. Contact factory.
Individual Force Pattern	Per-transmitter		
Individual Expected Pattern	Per-receiver		
Minimum Pattern Segment Size	512	bits	
Total Memory Space for Transmitters	1	Mbits	Memory allocation is customizable. Contact factory.
Total Expected Memory Space for Receivers	1	Mbits	Memory allocation is customizable. Contact factory.
Pattern Sequencing			
Sequence Control	Loop infinite Loop on count Play to end		
Number of Sequencer Slots per Pattern Generator	4		This refers to the number of sequencer slots that can operate at any given time. The instrument has storage space for 16 different sequencer programs.
Maximum Loop Count per Sequencer Slot	$2^{16} - 1$		
Additional Pattern Characteristics			
Pattern Switching	Wait to end of segment Immediate		When sourcing PRBS patterns, this option does not exist.
Raw Data Capture Length	8192	bits	

Table 6 Measurement and Throughput Characteristics

Parameter	Value	Units	Description and Conditions
BERT Sync			
Alignment Modes	Pattern PRBS		Module can align to any user pattern or preset pattern.
Minimum SYNC Error Threshold	3	bits	
Maximum SYNC Error Threshold	2^{32}-1	bits	
Minimum SYNC Sample Count	1024	bits	
Maximum SYNC Sample Count	2^{32}	bits	
SYNC Time	20	ms	Assumes a PRBS7 pattern that is stored in a user pattern segment and worst case misalignment between DUT pattern and expected pattern; data rate is 3.25 Gbps.
BERT			
Error Counter Size	32	bits	Sample counts in the BERT are programmed in increments of 32 bits.
Maximum Single-Shot Duration	2^{32}-1	bits	Repeat mode is available to continuously count over longer durations.
Continuous Duration	Indefinite		
Alignment			
CDR Lock Time	5	us	
Self-Alignment Time	50	ms	

Table 7 Instruction Sequence Cache

Parameter	Value	Units	Description and Conditions
Simple Instruction Cache			
Instruction Learn mode Instruction	Start Stop Replay		
Advanced Instruction Cache			
Local Instruction Storage	1M Instructions		
Instruction Sequence Segments	1000		

Table 8 DUT Control Capabilities

Parameter	Value	Units	Description and Conditions
DUT IEEE-1149-1 (JTAG) Port (Option)			
JTAG-Port Transmit Signals	TCK TRST TDI		
JTAG-Port Receive Signals	TDO		
JTAG-Port Transmit Voltage Swing (Fixed)	0 to 2.5	V	
JTAG-Port Receive Max Voltage Swing	0 to 2.5	V	
TDI Bit Memory	4k		
TDO Bit Memory	4k		
DUT SPI Port (Option)			
SPI Signals	SCLK SSN MISO MOSI		
Voltage Swing (Fixed)	0 to 2.5	V	

Revision Number	History	Date
1.0	Document release	Feb 27, 2013
1.1	Updated jitter injection specs, SSC specs, clock recovery specs; added block diagram descriptions	Oct 07, 2013
1.2	Minor edits	Oct 07, 2013
1.3	Update to specifications	Nov 12, 2013
1.4	Update to specifications	Apr 15, 2014
1.5	Update to specifications; removed test sequences	Aug 1, 2014
1.6	Updated document template	Jun 11, 2015
1.7	Added physical connectors info	Mar 11, 2016
1.8	Update to specifications	Nov 30, 2016
1.9	Update to specifications	Apr 07, 2017

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