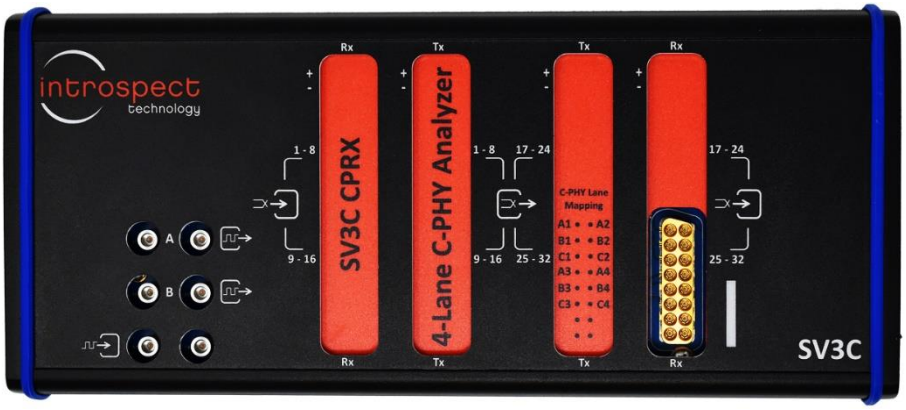
introspect technology

DATA SHEET

SV3C-CPRX

4-Lane C-PHY Analyzer

C SERIES



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Introduction

OVERVIEW

The SV3C-CPRX C-PHY Analyzer is an ultra-portable, high-performance instrument that enables exercising and validating MIPI C-PHY transmitter ports. Capable of analyzing any traffic and being completely data-rate agile, the C-PHY Analyzer includes complete hardware de-mapping and decoding, three-wire C-PHY CDR, and offers sophisticated capture and compare modes.

The C-PHY Analyzer operates using the highly versatile Introspect ESP Software environment. This environment allows for automating transmitter tests such as BER or protocol timings.

This document includes electrical specifications. It also describes the block diagram of the C-PHY Analyzer and provides detailed information about the various measurement and operating modes. Please refer to Introspect ESP Software documentation for additional operating instructions.

KEY FEATURES

- Parallel physical layer validation of MIPI C-PHY transmitters
- Protocol analysis for CSI-2, DSI, and DSI-2
- IP and software validation testing
- Interface test
- Plug-and-play system-level validation

KEY BENEFITS

- Any-rate operation across 4 simultaneous data lanes
- Complete C-PHY decode and de-map capability
- Protocol Analyzer suite for CSI-2, DSI, and DSI-2
- Precision time stamps to help understand each physical layer event
- Advanced triggering based on physical-layer and protocol-layer events
- Burst-mode and continuous mode analysis
- Multi-target BER (wire, wirestate, symbol, and data) and packet error rate testing
- Data streaming for FPGA-based protocol development
- State of the art programming environment
- Reconfigurable, protocol customization (on request)

ORDERING INFORMATION

TABLE 1: ITEM NUMBERS FOR THE SV3C-CPRX ANALYZER AND RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
4585	SV3C-DPRX - SV3C D-PHY Analyzer Bundle	Covers the MIPI D-PHY physical layer
4587	SV3C-CPRX - SV3C C-PHY Analyzer Bundle (this product)	Covers the MIPI C-PHY physical layer
4590	SV3C-DPRXCPRX - SV3C Combo C-PHY/D-PHY Analyzer Bundle	Combo D-PHY and C-PHY capability
4594	SV3C-DPRX Upgrade	Firmware and software license upgrade from 4585 to 4590

Feature Description

COMPLETE C-PHY RECEIVER IMPLEMENTATION

The SV3C-CPRX is a complete, integrated, 4-lane C-PHY receiver providing the analog front-end circuitry for C-PHY as well as a complete protocol back-end. As shown in Figure 1, each lane contains low power (LP) threshold voltage detectors, dynamically controlled C-PHY termination resistors, and fully differential high-speed (HS) receivers. The real-time behavior of the CPRX enables broad acquisition capabilities on physical-layer and protocol-layer events as detailed in Figure 2. The figure illustrates two common setups for deploying the CPRX, which can be used as either a terminating receiver or to probe live links.

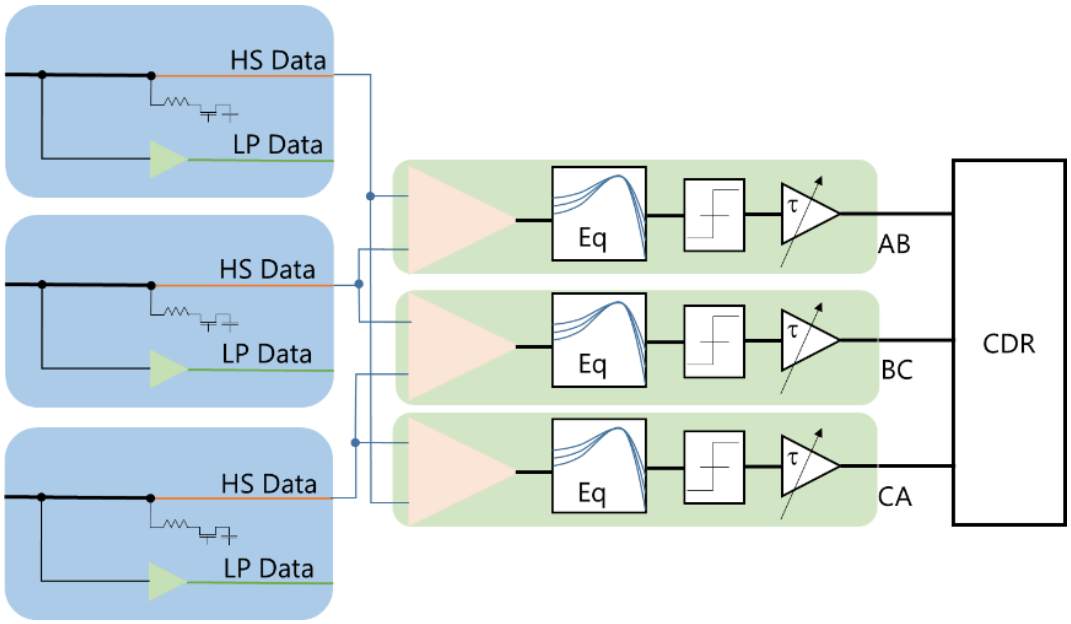


Figure 1: Receiver detail illustrating LP detection and automatic termination switches.

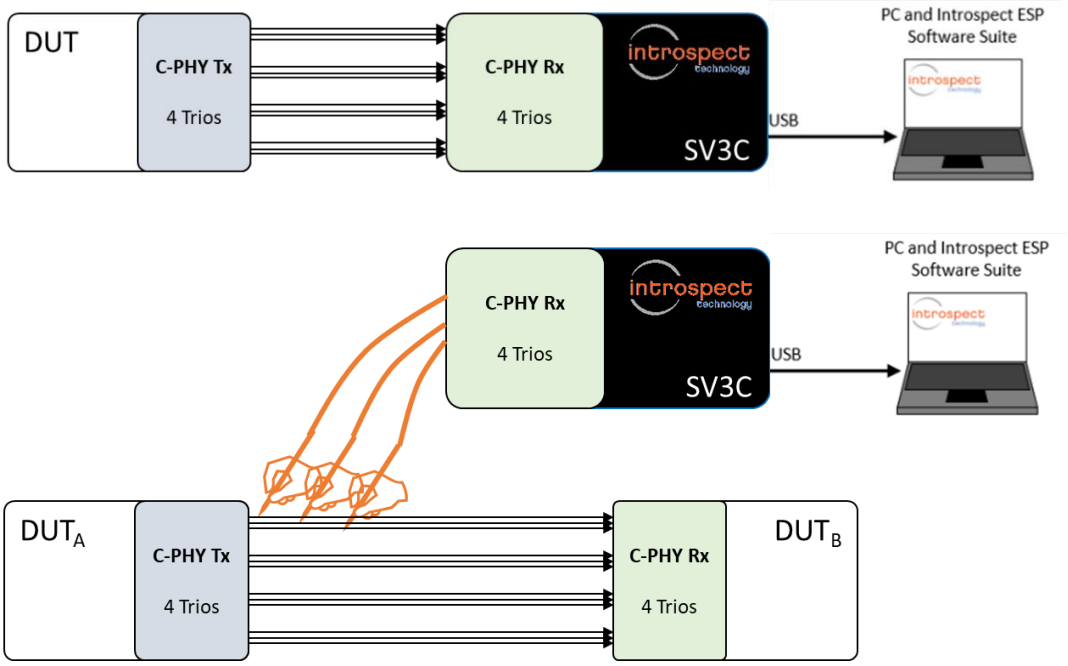


Figure 2: Example setups for deploying CPRX.

PROTOCOL ANALYSIS AND PRECISION TIME STAMPS

The SV3C-CPRX is a complete protocol analyzer for both camera and display serial interfaces. Either protocol can be selected within a single session, and the analyzer automatically adjusts its viewer displays based on the protocol being measured (Figure 3). At the same time, irrespective of the protocol, five viewers provide insight into PHY and protocol events while hyperlinks make for quick and intuitive navigation across the layers, namely:

- **HS Bursts** – View each high-speed burst, by lane, with quick statistics of the time of arrival in nanoseconds, SYNC offset and captured wire states, symbols, and data integers in each
- **CSI/DSI Packets** – Merged traffic from all lanes is shown as unique packets. Headers are decoded for easy, high-level viewing, and errors (header CRC, payload CRC, ECC) are automatically highlighted
- **LP States** – Each LP state is captured along with its time of arrival and duration; this viewer is extremely effective for building a visualization of the physical layer events
- **Frame Viewer** – Images are automatically reconstructed, even if incomplete, with details such as pixel format, virtual channel, and image dimensions

To enable the acquisition of high definition video streams under realistic traffic conditions, the SV3C-CPRX relies on event-based captures, assigning a time stamp to each pertinent event of the physical layer and protocol layer. This allows for optimized data storage and extremely efficient long-term data analysis. In terms of display, each viewer contains a column dedicated to the precision time stamps of a given burst, packet, LP event or frame. Correlating events in time makes it easy to identify anomalous transitions, unexpected short- or long-packets, and other physical layer perturbations, as depicted in Figure 3.

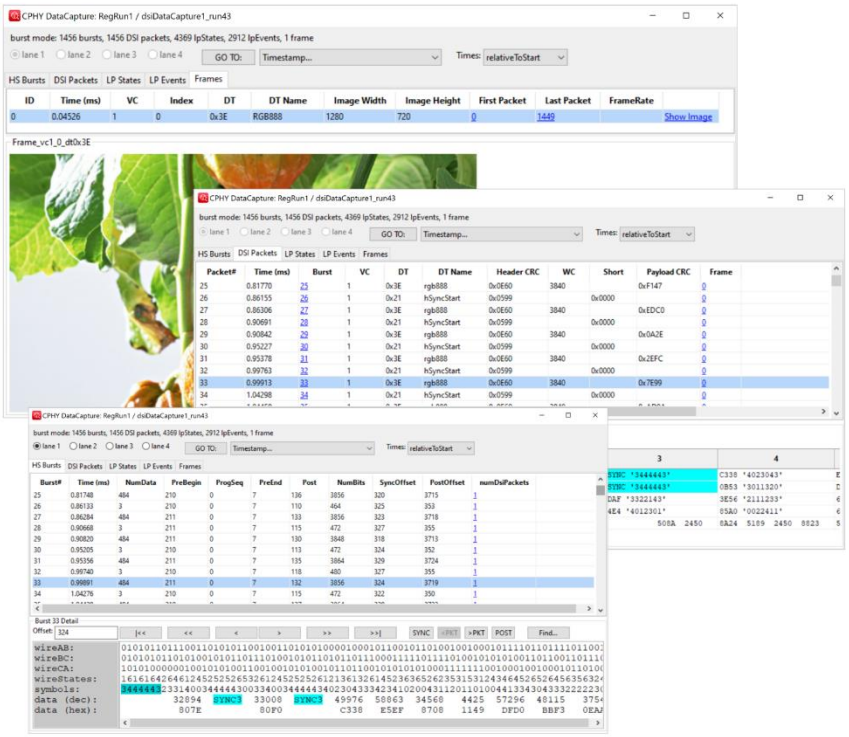


Figure 3: Protocol analyzer views.

HARDWARE CRC CHECKING AND PACKET ERROR RATE TESTING

Another fundamental feature of the SV3C-CPRX C-PHY Analyzer is its hardware-based packet error-rate detector. Similar to traditional BER, the PERT enables the measurement of real C-PHY transmissions from CSI-2 generators or DSI/DSI-2 generators. As illustrated in Figure 4, the Analyzer detects and filters all signal waveforms and compares only the packet data transmitted between SOT and EOT, registering errors after the data has been merged between lanes, thereby comparing errors in packets rather than bits.

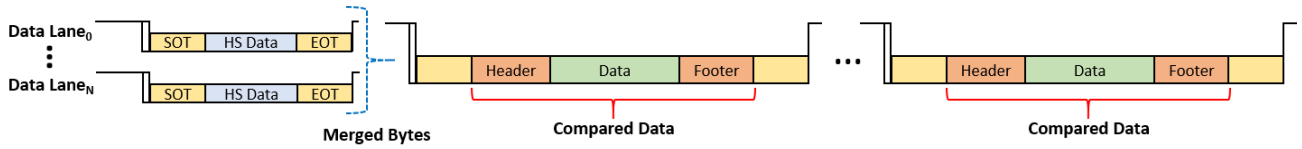


Figure 4: Illustration of packet error rate testing.

ADVANCED TRIGGER MODES

Figure 5 shows the user interface for defining the trigger mechanisms within the analyzer. At the highest level, the analyzer can be programmed to perform immediate captures (in which all data is measured irrespective of whether there are LP transitions or not) or burst-mode captures (Figure 6). The benefit of the immediate capture mode is that it allows for pattern learning and detecting multiple non-deterministic / non-repetitive packets. On the other hand, triggered captures offer a more focused view of C-PHY global timing parameters. In this mode, the C-PHY analyzer sets the termination resistors into automatic mode. Then, the analyzer waits for a valid LP to HS entry sequence before enabling a capture. If no valid HS-entry transition is detected, the capture returns an empty array. However, when a valid HS-entry transition is detected, the capture starts immediately.

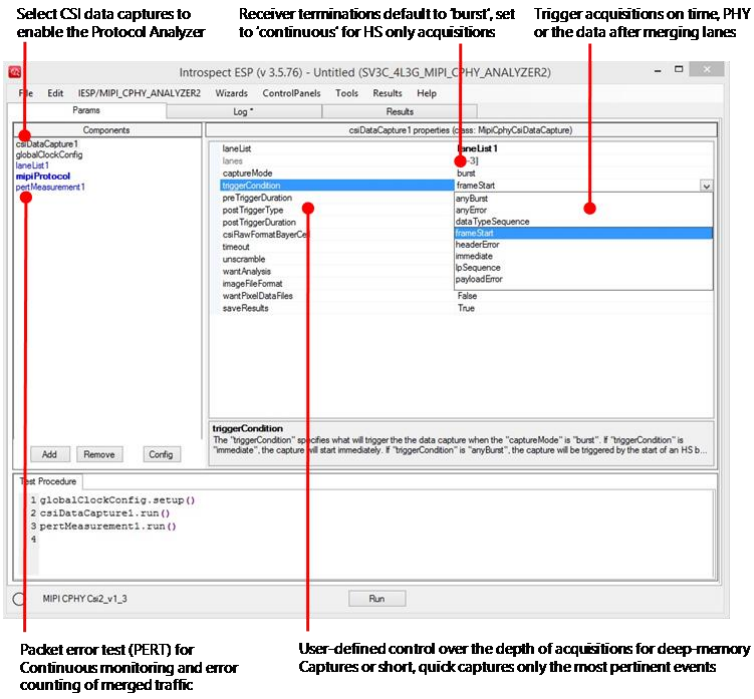


Figure 5: Introspect's ESP GUI for the SV3C CPRX. Top left: Components, shows CSI, DSI and PHY data acquisition. Top right: Properties, showing CSI Data capture. Bottom: test procedure ready to execute a CSI Data Capture, then PERT.

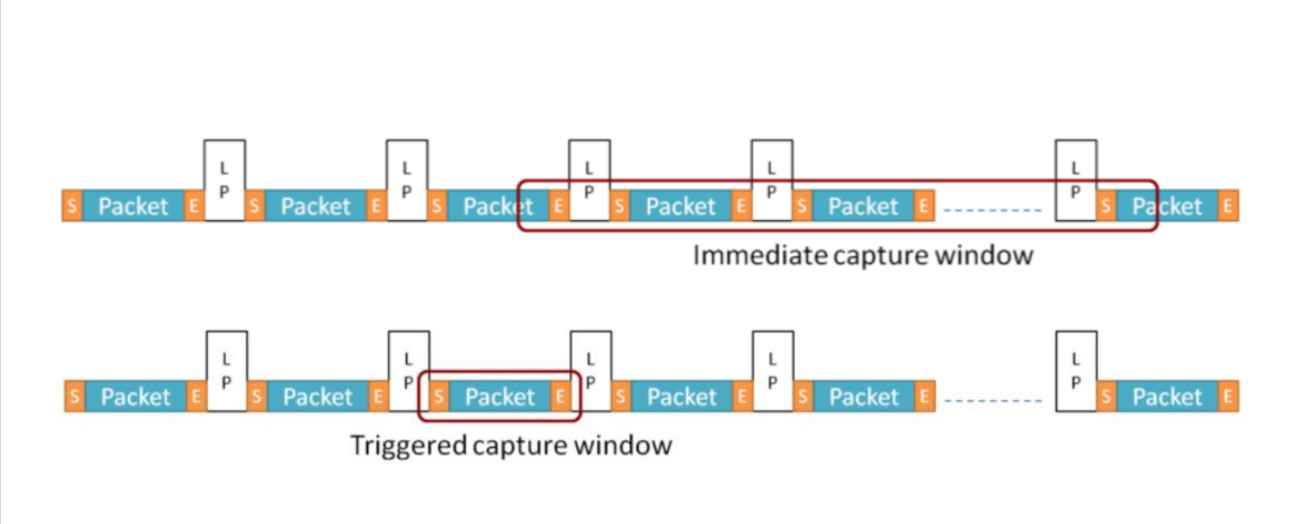


Figure 6: Illustration of multi-packet, per-lane PHY-level capture (Top), and triggered packet capture (Bottom).

Acquisitions and their depth are defined in time, by PHY events or by bytes of merged high-speed traffic. Figure 7 illustrates two methods of triggering acquisitions by PHY events. In Figure 7 (top), an acquisition begins on the first high-speed burst witnessed and completed after user-defined *N* bursts are recorded. In Figure 7 (bottom), a capture begins immediately and the analyzer records for a user-defined period of *N* nanoseconds. Figure 8 illustrates three examples of triggering acquisitions on merged, high-speed data. The CPRX supports one to four data lanes and independently merges and monitors bytes. Acquisition start is user-defined as the first event observed: (a) error within a packet header, (b) variable data type identifier, here chosen as 0x01 and (c) frame start packet (CSI only). The depth of the acquisition for each is arbitrarily chosen according to the number of *N* received: (d) bursts, (e) bytes and (f) frame end packets.

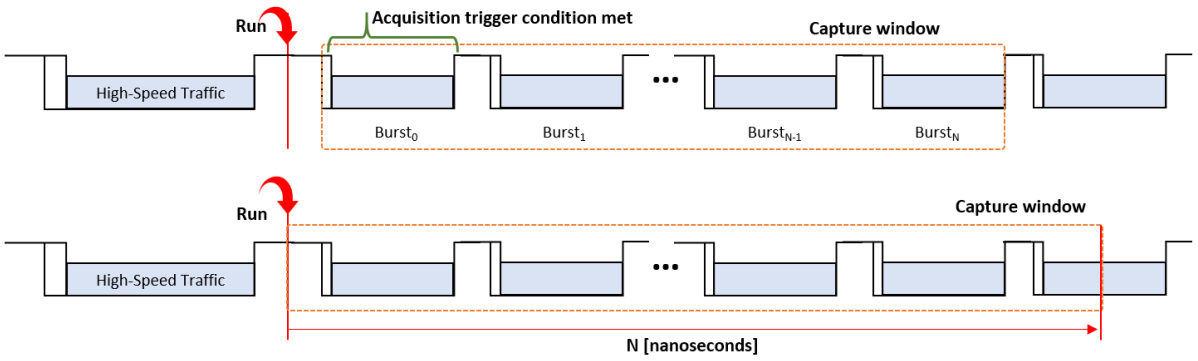


Figure 7: Illustration of two PHY-based acquisitions. Above, recording is triggered on first observed burst and depth is determined by user-defined N bursts. Below, acquisition begins immediately, and depth is for a user-defined period of N nanoseconds.

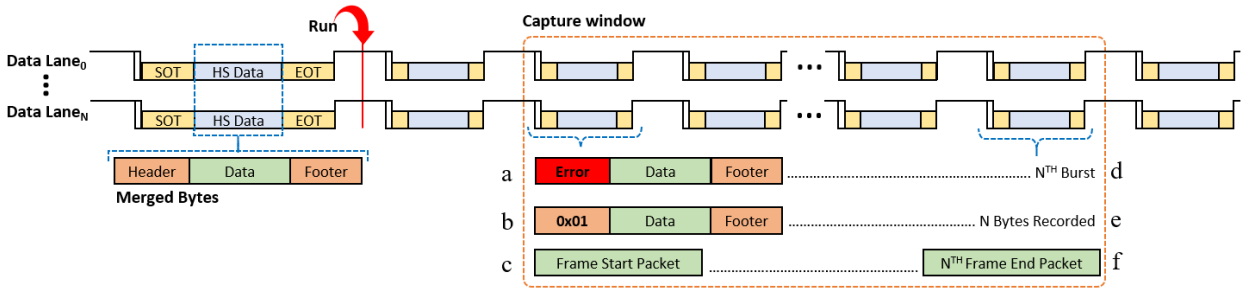


Figure 8: Illustration of three acquisitions triggered on merged high-speed traffic events: (a) header error, (b) user-defined data type identifier and (c) frame start packet. Three methods of acquisition depth are shown: (d) user-defined N bursts, (e) bytes, and (f) frames.

Finally, for completeness, Table 2 and Table 3 provide a list of trigger mechanism that are available in the Analyzer.

TABLE 2: CPRX METHODS FOR TRIGGERING A C-PHY ACQUISITION

TRIGGER CONDITON	TYPE	TRIGGER DESCRIPTION
anyBurst	PHY	the first high-speed burst witnessed over any data lane
immediate	Time-base	time-base acquisition, beginning immediately when run
lpSequence	PHY	user-defined sequence of LP states, e.g. “111,001,000” reflects a proper LP-HS entry sequence
anyError	CSI, DSI	the first error is registered: header, CRC or payload
hsDataTypeSequence	CSI, DSI	user-defined integer value to be identified in a packet header
headerError	CSI, DSI	protocol layer, the first error recognized in a packet header
payloadError	CSI, DSI	protocol layer, the first error recognized in a packet payload
frameStart	CSI	CSI-only, any packet with header data type 0x00 indicating the beginning of a frame
verticalSyncStart	DSI	DSI-only, any packet with header data type 0x01 indicating the beginning of a frame
dataType	CSI, DSI	protocol layer, data type to trigger on which can be either HS or LP

TABLE 3: UNITS AVAILABLE FOR DEFINING DEPTH OF AN ACQUISITION, ACCOMPANIED WITH A USER-DEFINED VALUE

POSTTRIGGERTYPE	TYPE	DESCRIPTION
durationInNs	Time-base	time-base acquisition, defined in nanoseconds
numberOfBursts	PHY	the total number of unique bursts acquired, across all data lanes
numberOfBytes	PHY	the total number of bytes recorded between SOT and EOT of all bursts
numberOfLpCommands	PHY	the first error is registered: header, CRC or payload
numberOfLpStates	PHY	number of unique LP states, e.g. "111,001,000" would be 3
numberOfFrameEnds	CSI	protocol layer, the number of frame-end packets recorded
numberOfVerticalSyncStarts	DSI	protocol layer, the number of packets with data type identifier 0x01

AUTOMATION

The SV3C-CPRX C-PHY Analyzer is operated using the award-winning Introspect ESP Software, a Python-based scripting environment. Shown in Figure 9, it includes a comprehensive suite of components and methods for executing capture and analysis of C-PHY transmissions, and a canvas for automating test procedures and rich analysis. The Python library is open, and an optional .NET DLL library provides access for integration with DUTs, other test equipment using Python, or alternative programming languages.

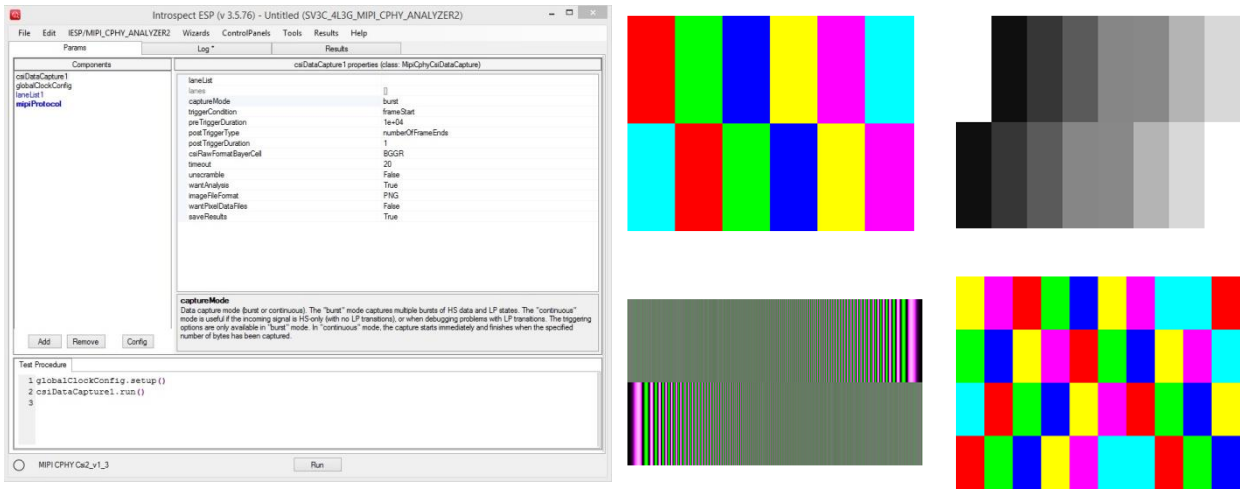


Figure 9: Introspect ESP Software environment, left, and right, examples of image captures.

BUILT-IN WIRE-STATE STREAMING

The SV3C CPHY is configured to automatically output wire state data on a low-speed parallel bus as it analyzes packets. These wire states can be directly received by a DUT with CSI-2 protocol state machine (e.g. FPGA prototyping board). Figure 10 provides details on this operation according to three distinct timing regions.

Region 1 in the diagram represents the interval in which the CPHY analyzer ignores wire state data, which begins after the received CPHY signal has entered the LP111 state and ends after the received CPHY signal has entered the LP000 state. Within this region, the received wire state is ignored and the streamed data output is set to zero.

Region 2 of the diagram indicates two short intervals, before and after the packet, occurring during the last 30 ns of the LP001 state and the first 50 ns of the LP111 state. During these intervals, some or all of the wires are at the same voltage level, causing the wire differential receivers to detect noise. Therefore, wire states are not valid in this region.

Region 3 of the diagram indicates the interval during which wire state data is valid and accurately streamed.

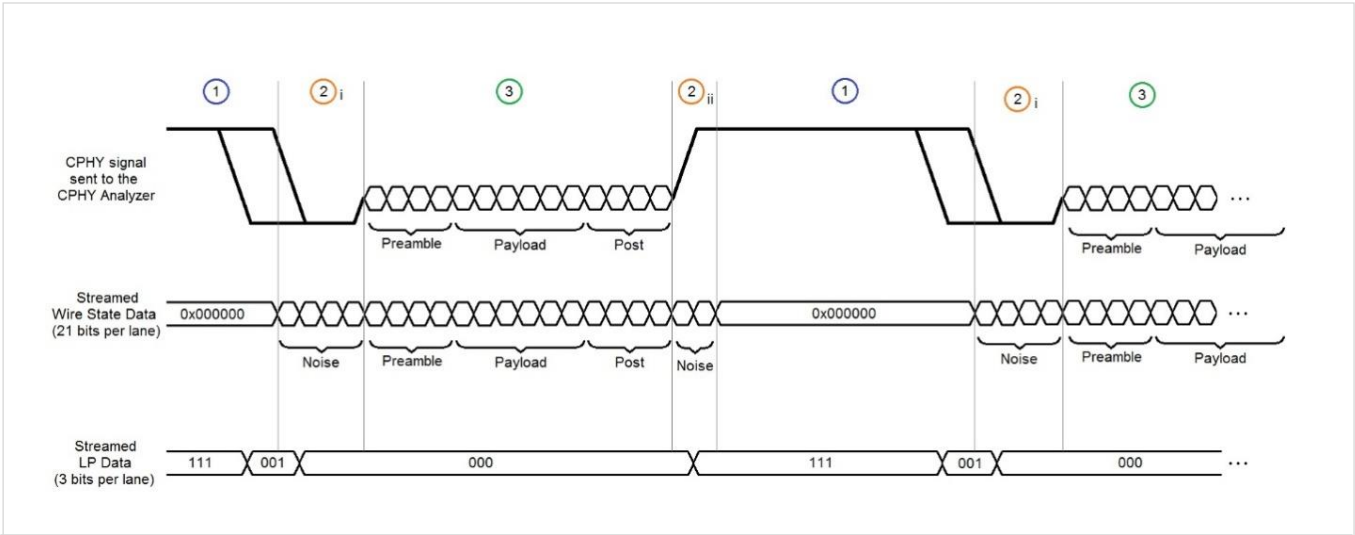


Figure 10: Wire-state streaming waveform and timing diagram.

The low-speed parallel data is available on the 240 pin Searay connector on the left side of the SV3C CPHY module. The pinout for this connector is provided in the pinout section of this document in Table 6.

The maximum data rate for which wirestate streaming is guaranteed is 1.4 Gsps, and this simply has to do with the bandwidth of single-ended general purpose I/O on typical DUT boards. A timing diagram of the streaming waveform is illustrated in Figure 11.

The resulting stream clock frequency (in MHz) is equal to the lane rate in Msps divided by 7 (200 MHz for the case shown in the figure). Data should be aligned on the rising edge of the clock. The minimum and maximum data delay with respect to the clock is 1.2 ns as shown.

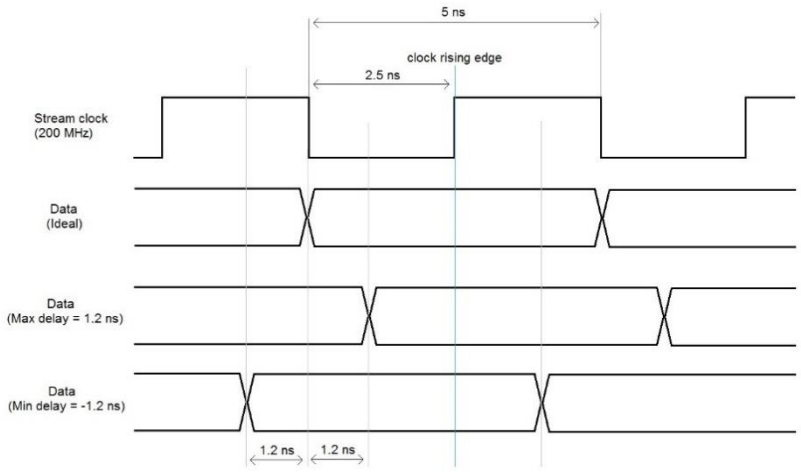


Figure 11: Wire-state streaming timing diagram at 1.4 Gsps.

Physical Description and Pinout

Figure 12 shows a diagram of the SV3C-CPHY with physical ports as shown, and Figure 13 shows a diagram of the 240 pin Searay connector on the left side of the SV3C system. A more detailed listing of the ports is provided in Table 4.

Figure 12: Illustration of SV3C-CPRX C-PHY Analyzer connectors.

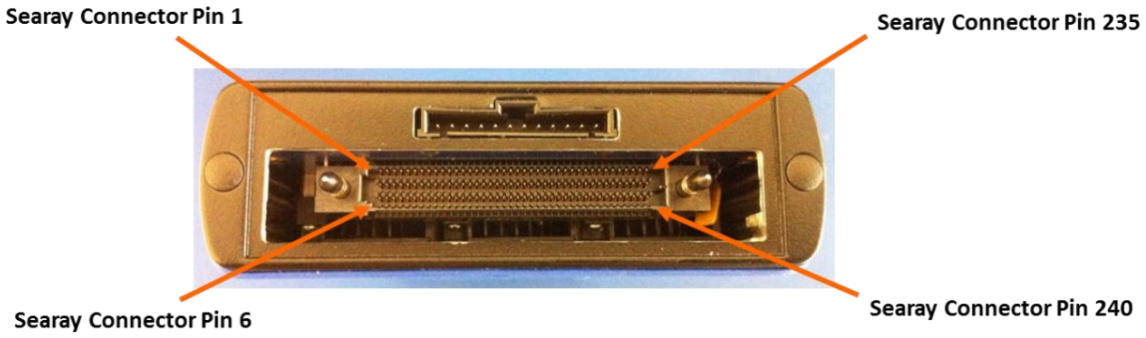


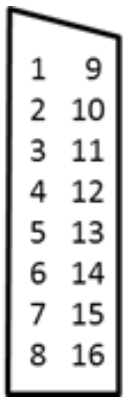
Figure 13: Illustration of Searay 240 pin connector.

TABLE 4: LISTING OF SV3C-CPRX C-PHY CONNECTORS

PORT / INDICATOR NAME	CONNECTOR TYPE
240 pin Searay Connector	Samtec Connector Part Number CON-SAMTEC-SEAF-40-01-L-06-2-RA-LP-TR
Ref Clock In Ref Clock Out A Ref Clock Out B	SMP Differential Pair SMP Differential Pair SMP Differential Pair
Rx Lane Trios 1 – 4	MXP
USB Port	USB
Power Switch / Connector	–

The pinout for the RX lane trios is provided in and the 240 pin Searay connector is provided in Table 6.

TABLE 5: MAPPING OF SV3C-CPRX C-PHY MXP LANE TRIOS



CONNECTOR PIN NUMBER	CORRESPONDING RX LANE TRIOS
1,2,3	Lane 1 A, B, C
9,10,11	Lane 2 A, B, C
4,5,6	Lane 3 A, B, C
12,13,14	Lane 4 A, B, C

TABLE 6: MAPPING OF 240 PIN SEARAY CONNECTOR

SEARAY CONNECTOR PIN	FUNCTION WHEN STREAMING WIRE STATES	FUNCTION WHEN STREAMING DATA
7	Clock	Clock
8	Lane 1, LP A	Lane 1, LP A
9	Lane 1, LP B	Lane 1, LP B
10	Lane 1, LP C	Lane 1, LP C
19	Lane 1, Wire state 1, C>A	Lane 1, Integer bit 0
20	Lane 1, Wire state 1, B>C	Lane 1, Integer bit 1
21	Lane 1, Wire state 1, A>B	Lane 1, Integer bit 2
22	Lane 1, Wire state 2, C>A	Lane 1, Integer bit 3
31	Lane 1, Wire state 2, B>C	Lane 1, Integer bit 4
32	Lane 1, Wire state 2, A>B	Lane 1, Integer bit 5
33	Lane 1, Wire state 3, C>A	Lane 1, Integer bit 6
34	Lane 1, Wire state 3, B>C	Lane 1, Integer bit 7
43	Lane 1, Wire state 3, A>B	Lane 1, Integer bit 8
44	Lane 1, Wire state 4, C>A	Lane 1, Integer bit 9
45	Lane 1, Wire state 4, B>C	Lane 1, Integer bit 10
46	Lane 1, Wire state 4, A>B	Lane 1, Integer bit 11
55	Lane 1, Wire state 5, C>A	Lane 1, Integer bit 12
56	Lane 1, Wire state 5, B>C	Lane 1, Integer bit 13
57	Lane 1, Wire state 5, A>B	Lane 1, Integer bit 14
58	Lane 1, Wire state 6, C>A	Lane 1, Integer bit 15
67	Lane 1, Wire state 6, B>C	Lane 1, “is_packet_data”
68	Lane 1, Wire state 6, A>B	
69	Lane 1, Wire state 7, C>A	
70	Lane 1, Wire state 7, B>C	
79	Lane 1, Wire state 7, A>B	
80	Lane 2, LP A	Lane 2, LP A
81	Lane 2, LP B	Lane 2, LP B
82	Lane 2, LP C	Lane 2, LP C
91	Lane 2, Wire state 1, C>A	Lane 2, Integer bit 0
92	Lane 2, Wire state 1, B>C	Lane 2, Integer bit 1
93	Lane 2, Wire state 1, A>B	Lane 2, Integer bit 2

94	Lane 2, Wire state 2, C>A	Lane 2, Integer bit 3
103	Lane 2, Wire state 2, B>C	Lane 2, Integer bit 4
104	Lane 2, Wire state 2, A>B	Lane 2, Integer bit 5
105	Lane 2, Wire state 3, C>A	Lane 2, Integer bit 6
106	Lane 2, Wire state 3, B>C	Lane 2, Integer bit 7
115	Lane 2, Wire state 3, A>B	Lane 2, Integer bit 8
116	Lane 2, Wire state 4, C>A	Lane 2, Integer bit 9
117	Lane 2, Wire state 4, B>C	Lane 2, Integer bit 10
118	Lane 2, Wire state 4, A>B	Lane 2, Integer bit 11
127	Lane 2, Wire state 5, C>A	Lane 2, Integer bit 12
128	Lane 2, Wire state 5, B>C	Lane 2, Integer bit 13
129	Lane 2, Wire state 5, A>B	Lane 2, Integer bit 14
130	Lane 2, Wire state 6, C>A	Lane 2, Integer bit 15
139	Lane 2, Wire state 6, B>C	Lane 2, “is_packet_data”
140	Lane 2, Wire state 6, A>B	
141	Lane 2, Wire state 7, C>A	
142	Lane 2, Wire state 7, B>C	
151	Lane 2, Wire state 7, A>B	
152	Lane 3, LP A	Lane 3, LP A
153	Lane 3, LP B	Lane 3, LP B
154	Lane 3, LP C	Lane 3, LP C
163	Lane 3, Wire state 1, C>A	Lane 3, Integer bit 0
164	Lane 3, Wire state 1, B>C	Lane 3, Integer bit 1
165	Lane 3, Wire state 1, A>B	Lane 3, Integer bit 2
166	Lane 3, Wire state 2, C>A	Lane 3, Integer bit 3
175	Lane 3, Wire state 2, B>C	Lane 3, Integer bit 4
176	Lane 3, Wire state 2, A>B	Lane 3, Integer bit 5
177	Lane 3, Wire state 3, C>A	Lane 3, Integer bit 6
178	Lane 3, Wire state 3, B>C	Lane 3, Integer bit 7
187	Lane 3, Wire state 3, A>B	Lane 3, Integer bit 8
188	Lane 3, Wire state 4, C>A	Lane 3, Integer bit 9
189	Lane 3, Wire state 4, B>C	Lane 3, Integer bit 10
190	Lane 3, Wire state 4, A>B	Lane 3, Integer bit 11
199	Lane 3, Wire state 5, C>A	Lane 3, Integer bit 12
200	Lane 3, Wire state 5, B>C	Lane 3, Integer bit 13

201	Lane 3, Wire state 5, A>B	Lane 3, Integer bit 14
202	Lane 3, Wire state 6, C>A	Lane 3, Integer bit 15
211	Lane 3, Wire state 6, B>C	Lane 3, “is_packet_data”
212	Lane 3, Wire state 6, A>B	
213	Lane 3, Wire state 7, C>A	
223	Lane 3, Wire state 7, B>C	
224	Lane 3, Wire state 7, A>B	
225	Clock	

Specifications

TABLE 7: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol Support			
Physical layer interface	C-PHY		
MIPI protocol	CSI-2/DSI/DSI-2		
LP/HS Handling	Automatic		Tester automatically detects LP and HS data
Ports			
Number of Receiver Lanes	4		
Number of Dedicated Clock Outputs	2		Separate clock for providing reference to the DUT
Number of Dedicated Clock Inputs	1		Used as external Reference Clock input
Number of Trigger Input Pins	3		Armed in software to trigger the start of specific measurements
Number of Flag Output Pins	3		Armed in software to flag test completion or pass/fail criteria
Data Rates and Frequencies			
Minimum Data Rate	80	Msps	
Maximum Data Rate	3.125	Gsps	
Minimum External Input Clock Frequency	10	MHz	
Maximum External Input Clock Frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input) Note: internal clock termination is

			50 ohms to 1.275 V. AC coupling is acceptable.
Minimum Output Clock Frequency	10	MHz	
Maximum Output Clock Frequency	250	MHz	
Output Clock Frequency Resolution	1	kHz	
Supported External Input Clock I/O Standards			Support for LVDS, LVPECL, CML, HCSL, and CMOS. Note: output clock is DC coupled.
Minimum LP State Period	50	ns	

TABLE 8: RECEIVER CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Coupling			
Input Impedance	50 Hi-Z	Ω Ω	
HS Performance			
Minimum Detectable Differential Voltage	90	mV	Specified as 2 x 45 mV single-ended |VOD| described in C-PHY
Maximum Allowable Differential Voltage	500	mV	
Resolution Enhancement & Equalization			
Minimum DC Gain	0	dB	
Maximum DC Gain	8	dB	
DC Gain Control	Per-receiver		
Equalization Control	Per-receiver		
Timing Generator Performance			
Resolution at Maximum Data Rate	7.8125	mUI	
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	+/- 2	UI	
LP Voltage Threshold Controls			
Minimum Programmable Threshold Voltage	-100	mV	
Maximum Programmable Threshold Voltage	1500	mV	
Threshold Voltage Resolution	1		
Threshold Voltage Accuracy	Larger of 5.0 mV or 2.0 % of		

	programmed value		
Global Timing Parameters			
Minimum Pre-Begin Duration (termination forced)	28	Symbol	2.5 Gsps, 50 ns LP001 duration, 38 ns LP000 duration
Minimum Pre-Begin Duration (termination automatic)	28	Symbol	2.5 Gsps, 100 ns LP001 duration, 38 ns LP000 duration
Minimum LP001 Duration	50	ns	
Minimum LP000 Duration (T3-Prepare)	38	ns	

TABLE 9: CLOCKING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Internal Time Base			
Number of Internal Frequency References	1		
Frequency Resolution of Programmed Data Rate	1	Kbps	

TABLE 10: PATTERN HANDLING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Preset Patterns			
Standard Built-In Patterns	PRBS.5 PRBS.7 PRBS.9 PRBS.11 PRBS.13 PRBS.15 PRBS.18		

Pattern Choice per Receive Channel	PRBS.23 PRBS.31 Per-receiver		
User-programmable Pattern Memory			
Individual Expected Pattern	Per-lane		
Total Memory Space for Expected Patterns	4	GByte	
BERT Characteristics			
Maximum Packet Size	$2^{32} - 1$		
Maximum Number of Packets	$2^{32} - 1$		
Maximum Number of Repeats	$2^{32} - 1$		
Maximum Time Between SYNC Words in Burst Mode	1	ms	
Minimum Time Between SYNC Words in Burst Mode	20 x 7	UI	Separate from above 16 segments.
Capture Memory Depth	262,144	Wire States	Additional capture memory is under development.
Additional Pattern Characteristics			
C-PHY Decoder & Demapper	Per Lane		
Escape Mode Command Detection	Per Lane		

REVISION NUMBER	HISTORY	DATE
1.0	Import from internal documentation	November 10, 2014
1.1	Updated lane count, data rate	November 20, 2014
1.2	Modified description of termination system, updated reference clock and preamble specifications, included description for streaming applications and pinouts.	February 6, 2015
1.3	Updated document template	June 1, 2015
1.4	Modified product description and updated technical specifications	December 1, 2017
1.5	Updated copyright information	August 25, 2021
1.6	Updated template	October 6, 2021

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